Controlled Cracking for Large-Area Thin Film Exfoliation: Working Principles, Status, and Prospects

Yonghwan Lee[1,2], Hark Hoe Tan[1,3], Chennupati Jagadish[1,3] and Siva Krishna Karuturi[1,4]**

[1]Department of Electronic Materials Engineering, Research School of Physics, The Australian National University, Canberra, ACT 2601, Australia

[2]Convergence Materials Research Center, Gumi Electronics and Information Technology Research Institute, Cheomdangieop 1-ro 17, Sandong-myeon, Gumi 39171, Republic of Korea

[3]Australian Research Council Centre of Excellence for Transformative Meta-Optical Systems, Research School of Physics, The Australian National University, Canberra, ACT 2601, Australia

[4]Research School of Electrical, Energy, and Materials Engineering, The Australian National University, Canberra, ACT 2601, Australia

KEYWORDS: controlled cracking, fracture, thin films, layer-transfer technology, flexible optoelectronics

ABSTRACT

The production of flexible monocrystalline semiconductor thin films with less than a few tens of micrometers in thickness is currently receiving huge interest in various emerging applications such as mobile healthcare (mHealth), wearable devices, smart cities, and internet of things (IoT). However, conventional techniques fail to produce wafer-scale monocrystalline thin films without the use of sophisticated equipment. Recently, controlled cracking method has shown promise as a facile and scalable method to produce monocrystalline inorganic semiconductor thin films such as Si, Ge, III-V, and III-N materials. In this method, a crystalline semiconductor thin film can be exfoliated from its thick donor substrate via sub-surface crack propagation. The cracking based layer transfer approach does not require expensive processing equipment and enable the production of multiple thin films from the same donor substrate. In this focused review article, we present the working principles, recent progress, and future prospects of this emerging crack-assisted layer transfer technology. The unique advantages of this technology for the state-of-the-art flexible (opto)electronics are also highlighted. This article offers insights for the fabrication of large-scale flexible monocrystalline semiconductors, which is crucial for the development of next-generation (opto)electronics.

1. Introduction

Over the last several years, flexible (opto)electronic devices have been touted as a solution to fulfil emerging applications such as mobile healthcare (mHealth), wearable systems, smart cities, and internet of things (IoT).[1] However, the realization of flexible (opto)electronic devices involves significant paradigm shift from conventional thick semiconductor wafer-based technology to a thin film based one, which offers the required mechanical flexibility. Significant attention has been paid to organic materials that allow low temperature fabrication to achieve thin film flexible devices.[2] However, organic devices still suffer from several drawbacks such as insufficient electronic performance, thermal/chemical instability, and non-compatibility with the current complementary metal oxide semiconductor (CMOS) processes.

Different strategies have been applied to realize flexible (opto)electronic devices with high performance using monocrystalline inorganic semiconductors in the form of thin films. The mainstream approach consists of the fabrication of full device structure on conventional thick semiconductor wafers and separation of the top device layers from the thick wafers. Subsequently, the separated thin film devices can be integrated on flexible substrates such as plastic, paper, fabric, and thin metal film, which provide better flexibility than the conventional thick wafer based devices. This strategy, called layer transfer process, enables flexibility to these monocrystalline inorganic semiconductors and has found some success in the past decade.

The layer transfer methods developed on inorganic monocrystalline semiconductors for flexible and high performance (opto)electronic devices can be categorized into two types: chemical lift-off and laser lift-off. In chemical lift-off process, a lattice-matched sacrificial layer and the desired device layer are grown in sequence on a growth substrate via epitaxial growth technique.[3]

Subsequently, the sacrificial layer is selectively etched away by a wet-etching process to release the top device layer from the growth substrate. For instance, lattice-matched AlAs and GaAs can be sequentially grown on GaAs growth substrate via metal-organic vapor deposition (MOCVD) or molecular beam epitaxy (MBE). The intermediate AlAs layer (~10 nm) can be selectively removed by immersing in HF acid solution while maintaining the GaAs layer intact with negligible etch due to an extremely high etching selectivity of AlAs to GaAs (~10^6:1).[4] After fully removing the AlAs layer, the top GaAs layer can be released from the GaAs growth substrate. The chemical lift-off process has been shown on wafer-scale (2 inch) and successfully demonstrated for various (opto)electronic devices.[5-6] However, this approach is limited by the requirement of an expensive epitaxial growth equipment and low throughput with tedious wet-etching process in hazardous chemical solutions.

Laser lift-off process is another layer transfer technique demonstrated for separating epitaxial GaN layer from its transparent growth substrate (*e.g.*, sapphire or SiC) by laser induced photothermal reaction.[7-8] To separate a GaN epilayer, an excimer laser is used to expose the GaN epilayer through the rear side of the transparent growth substrate. The GaN layer at the interface with the growth substrate absorbs the irradiated laser light and undergoes decomposition into Ga and N_2. As a result, the GaN layer can be delaminated from its growth substrate. The laser lift-off process shows relatively high throughput and has been demonstrated for light-emitting diodes (LED) within the industrial settings. However, this approach still requires expensive laser equipment and is limited only to specific material systems.

Recently, intended cracking on brittle semiconductor substrates has been introduced as a cost- and time-efficient approach for realizing flexible devices. Although uncontrolled cracking in brittle semiconductors can cause catastrophic failure during conventional semiconductor fabrication process, it has been shown that an exquisitely controlled cracking method could function as a wafer-scale and facile layer transfer technique. In particular, crack-assisted layer transfer technique has several advantages compared with the above-mentioned conventional lift-off methods. First, this approach is applicable to a variety of brittle semiconductor substrates (*e.g.*, Si, Ge, III-V, and III-N). Second, crack-assisted layer transfer process can exfoliate semiconductor thin films with various material structures (*e.g.*, bulk substrate, atomic 2D layer, and nanowire). Finally, the crack depth, which determines the thickness of an exfoliated semiconductor film, can be easily controlled by simply tuning the process parameters. Finally, this facile wafer-scale process enables high throughput without the need for sophisticated equipment.

Herein, we provide a focused review of the recent advancements of crack-assisted layer transfer technology. This review is divided into four main categories: i) working principles of crack-assisted layer transfer technology, ii) application of this technology to various semiconductor structures including bulk substrates, 2D materials, and nanowires, iii) engineering the interfacial fracture toughness, and iv) applications of the transferred films. We also discuss current limitations of this technique and opportunities it provides for future advancement. Finally, we summarize the current challenges and future research directions for crack-assisted layer transfer method, with an emphasis on both lab-scale demonstrations and large-scale implementation.

2. Working Principles of the Crack-Assisted Layer Transfer Technology

2.1 Fundamentals of Spalling Mode Fracture

Cracking in a material can be defined as the physical breaking of adjacent atomic bonding resulting in the formation of a new surface. Cracking occurs when the energy release rate G, or stress intensity factor K, induced by an applied mechanical force exceeds the ability of a material containing a crack to resist fracture, known as toughness G_c, or fracture toughness K_c.[9] In a thin film/substrate double-layered system, the thin film generates a residual stress its deposition on the substrate. If the crack growth criterion ($G > G_c$ or $K > K_c$) is met due to the residual stress generated in the thin film, it makes the crack grow in the thin film, substrate, or at the film-substrate interface. The most commonly observed cracking patterns in thin film/substrate systems include thin film cracking, delamination, buckling, and substrate spalling.[10-11] These cracking patterns are determined by the sign of the residual stress, ductility, elastic moduli, and adhesion force between the thin film and substrate. Among them, spalling mode fracture which is the desired phenomenon to exfoliate a thin film from its substrate occurs when the following three requirements are satisfied: tensile stressed thin film, sufficient adhesive bonding force between the thin film and the substrate, and brittle substrate.

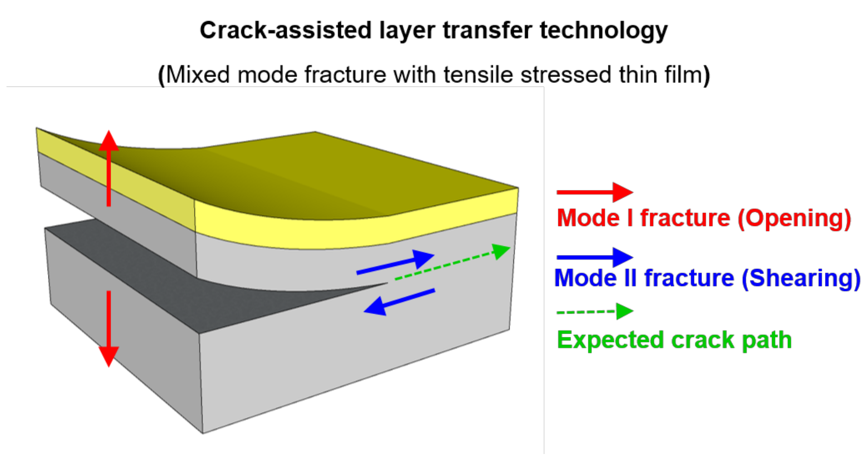

Figure 1. Spalling mode fracture for crack-assisted layer transfer technology. Schematic illustration of spalling mode fracture of brittle bulk substrates with a tensile stressed thin film. The stress at crack tip exists as two different stress components: opening stress (red solid line) and shearing stress (blue solid line).

Although the cracking phenomenon has been considered as a significant issue in conventional semiconductor fabrication process, the spalling mode fracture has recently been adopted as a facile layer transfer technology. The driving force of the spalling mode fracture is the tensile stress generated by a stressor layer deposited on top of a substrate. The stress originated from the stressor layer can be divided into two stress components with different directions near the crack tip: (i) tensile stress acting perpendicular to the crack plane and (ii) shear stress acting along the crack plane and normal to the crack front. In fracture mechanics, the fracture with tensile stress component is defined as mode I fracture (opening mode) while the fracture with shear stress component is defined as mode II fracture (shearing mode). Figure 1 illustrates these fracture modes. The crack growth occurs through mode I fracture. As discussed above, the tensile stress from the stressor layer induces a concentrated stress field near the crack tip, which can grow when G induced by the stress components exceeds G_c of the substrate. G of the bilayer system is proportional to the product of the stressor layer thickness, h and square of the tensile stress, σ of the stressor layer:[12]

$$G \propto h\sigma^2 \tag{1}$$

The crack growth location is determined by the mode II fracture. The shear stress induced by the stressor layer exists in the substrate in out-of-plane direction. The position where the shear component is minimized is called the neutral axis.[13] The crack growth direction tends to follow the trajectory of the neutral axis, which is determined by the elastic and dimensional parameters of the stressor layer and substrate (*e.g.*, thickness and modulus).[12, 14] By propagating the crack to the opposite edge position of the initial crack as shown in Figure 1, the top surface layer can be exfoliated from the substrate. The crack depth can be calculated as a function of the elastic and dimensional parameters using theoretical models reported in the literature.[12, 15]

2.2. Tensile Stressed Stressor Layer

As mentioned earlier, the stressor layer plays an important role in determining the crack growth and depth during spalling mode fracture. In addition, it can be useful as a handling layer to prevent the undesired breaking of the fragile thin film after the transfer process. It can also function as a bottom metal contact layer in a vertical device structure if the stressor layer is a metallic layer. For these reasons, the selection of the appropriate stressor layer material is vital in spalling. The following are the important requirements of a stressor layer: (i) high fracture toughness, (ii) facile controllability of stress level, (iii) strong adhesion with target substrates, and (iv) cost-effectiveness.

Ni has been shown to be an appropriate candidate material for stressor layer due to its high fracture toughness (145-222 MPa√m) and facile controllability of stress level deposited via sputtering or electrodeposition.[16] The stress in the Ni thin film deposited by sputtering process can be modified by controlling the Ar working pressure.[17] For instance, deposition at low Ar pressure induces compressive stress in the Ni film due to atomic peening effect, while tensile stress is induced at high Ar pressure. By adjusting the sputtering pressure from a few mTorr to tens of mTorr, the stress could be tuned between 300 and 700 MPa.[18] Ni stressor layer can also be deposited by electrodeposition method which is both cost-effective and high throughput compared with the sputtering technique. In addition, nanocrystalline Ni stressor layer deposited by electrodeposition process has a higher mechanical hardness than micro-crystalline Ni.[19] The residual stress of Ni stressor layer deposited by electrodeposition process is highly affected by the chemical composition in the electrolyte and the deposition current density. For instance, Luo *et al*. showed that the intrinsic stress in electrodeposited Ni films can be changed from compressive stress at low deposition current density (< 15mA/cm^2) to tensile stress at higher current density.[20] The presence of phosphorus ions in the electrolyte solution can also enhance the tensile stress of the Ni film.[21] Tensile stress in electrodeposited Ni film was increased from 112 to 290 MPa as the phosphorus ion concentration was increased from 0 to 0.01 M. However, the tensile stress of the Ni film decreased when the phosphorus ion concentration was increased above 0.015 M due to the generation of micro-cracks in the film.

As mentioned above, the stressor layer should form sufficient adhesion with the donor substrate. Physical vapor deposition (PVD) techniques such as thermal or e-beam evaporators are frequently used to deposit Ti thin film on donor substrates which provides strong adhesion for the subsequent thick stressor layer formation. However, the Ti layer deposition via the vacuum processing is regarded as a factor for increased process costs. Yang *et al*. demonstrated a solution-processed nanohole structure on donor substrate and autocatalytic electroless deposition of Ni seed layer to enhance the adhesion of electrodeposited Ni stressor layer on Si donor substrate without using any vacuum processing.[22] These approaches that do not rely on the usage of costly and time consuming equipment are crucial to realize cost-effective crack-assisted layer transfer technology for industrial implementation.

For photovoltaic applications, stressor layer deposition was investigated on Si target substrates with Al and Ag paste by screen-printing method.[23-24] The screen printing method provides an advantage of compatibility with conventional photovoltaic device fabrication. However, a high temperature (>700 °C) annealing process was needed to generate sufficient thermal misfit stress for crack growth in the Si substrate. The high temperature annealing process on metal stressor layer/Si substrate induces undesired metal impurity diffusion into the Si substrate and unintended thin oxide layer formation at metal stressor layer/Si interface that has to be removed to obtain high performance photovoltaic devices. In addition, the fracture at temperatures more than the brittle to ductile temperature (BDTT, 545°C for bulk Si) induces nucleation of a huge amount of dislocations at/near the crack tip.[25]

To avoid the above-mentioned disadvantages, thermosetting polymer based thin film can be used as a stressor layer.[26-28] The polymer layer can be easily deposited by drop-casting or spin coating on a target substrate. In addition, the large difference in thermal expansion coefficients of the polymer layer and semiconductor allows a significant reduction in the annealing temperature to below 150 °C to induce sufficient thermal misfit stress for crack growth. Martini *et al*. showed the polymer based layer has a strong interface adhesion force with a Si substrate, and a 400 µm-thick polymer layer enables spalling mode fracture to produce ~100 µm-thick Si.[26] However, a high variation of exfoliated Si thickness due to the lack of uniformity of the polymer based stressor layer thickness remains a problem to be addressed.

2.3. Crack Propagation

After the deposition of a tensile stressed stressor layer on a semiconductor target substrate, the crack growth criterion ($G > G_c$) has to be satisfied for spalling mode fracture. One of the simplest ways to realize spalling mode fracture is through the deposition of a stressor layer above the critical thickness where G is greater than G_c (see equation 1).[21-22] Another approach to increase tensile stress in the stressor layer is by using thermal misfit stress. As discussed earlier, annealing the stressor layer/substrate system can induce thermal misfit stress due to the difference in thermal expansion coefficients of the stressor layer and substrate. For instance, a metal stressor layer such as Ni has a higher thermal expansion coefficient compared to the semiconductor substrate (*e.g.*, 13 ppm/°C for Ni and 2.6 ppm/°C for Si),[29] and a thermal misfit stress can be generated during the cooling step in the annealing process. Laser ablation method can also be used for the formation of a lateral notch working as an initial crack at the substrate edge to determine the crack propagation direction.[30-31]

In 2012, Bedell *et al*. reported a novel spalling strategy, called controlled spalling process.[32] This approach shows that an external force can be used as the driving force for crack propagation in the spalling mode fracture. Figure 2a schematically illustrates the controlled spalling process. It starts with the deposition of a Ni stressor layer on a target substrate, and the thickness and residual stress of the Ni stressor layer are well controlled to sub-spontaneous spalling regime (blue dot of Figure 2b). Subsequently, a flexible tape is bonded to one edge of the Ni stressor layer. An external force is applied by the way of pulling the flexible tape up, inducing crack initiation at the edge of the Ni stressor layer and sub-surface crack propagation across to the opposite edge position of the initial crack to fully exfoliate the top semiconductor layer as a thin film without destruction of nanometer-scale CMOS device (Figure2 c-d). This approach provides controllability of the crack initiation position, crack propagation direction, and a facile crack propagation through the application of an external force. In addition, this process can be conducted at room temperature without the need for any sophisticated crack initiation equipment such as laser ablation.

3. Crack-Assisted Layer Transfer of Various Semiconductors.

3.1. Bulk Semiconductor Substrates: Si, Ge, III-V, and III-N

A strong advantage of crack-assisted layer transfer technology is its wide applicability to numerous semiconductors (*e.g.*, Si, Ge, III-V, and III-N) as well as various material structures (*e.g.*, bulk substrates, 2D materials, and nanowires). A critical factor that determines the feasibility of crack-assisted layer transfer technology on a target semiconductor substrate is its fracture toughness, which governs the crack growth criteria. Depending on the fracture toughness, the stress level and thickness of the stressor layer have to be carefully optimized. Table 1 shows a summary of the fracture toughness values of various key semiconductor materials.

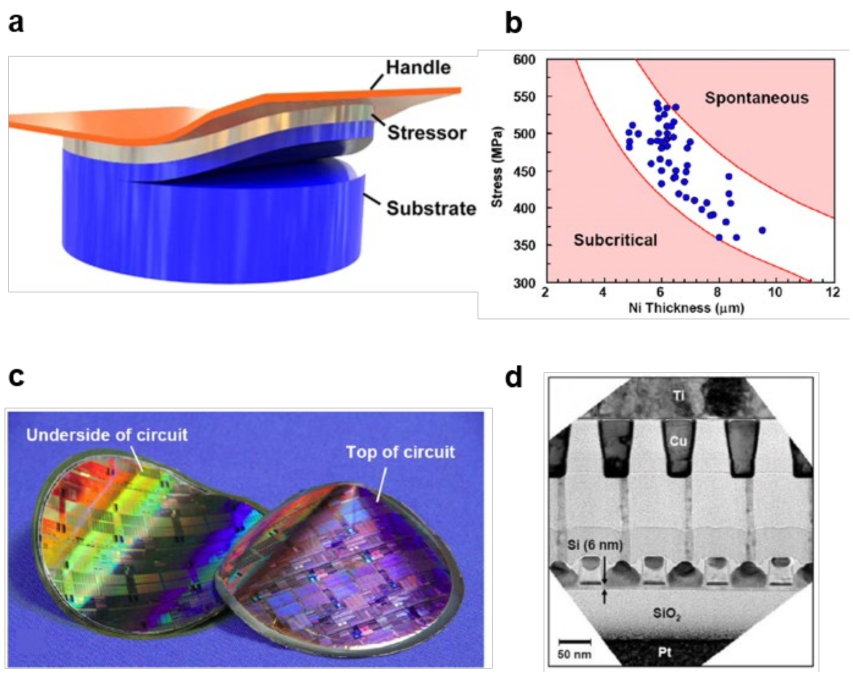

Figure 2. Spalling mode fracture activated by an external force. (a) Schematic illustration of the procedure for controlled spalling process. (b) Process window for spalling process of (100) Ge bulk substrate using tensile stressed Ni based stressor layer. (c) Wafer-scale (100 mm diameter) flexible Si based CMOS circuits produced via controlled spalling process. (d) Cross-sectional

transmission electron microscope (X-TEM) image of the flexible Si based CMOS circuit with the stressor layer. Reprinted with permission from ref.[18]. Copyright 2013, IOP Publishing Ltd.

Table 1. Fracture toughness K_{IC} of various brittle semiconductor materials

Material	Surface orientation	Fracture toughness K_{IC} (MPa√m)	Crystal structure	Measurement method	Ref.
Si	(100)	0.91	Diamond	Indentation (Vickers tip)	33
Si	(110)	0.94	Diamond	Indentation (Vickers tip)	33
Si	(111)	0.83	Diamond	Indentation (Vickers tip)	33
Ge	(111)	0.61	Diamond	Indentation (Vickers tip)	33
GaAs	(100)	0.43	Zinc-blended	Micro-indentation (Vickers tip)	33-34
GaAs	(110)	0.31	Zinc-blended	Micro-indentation (Vickers tip)	34
GaAs	(111)	0.45	Zinc-blended	Micro-indentation (Vickers tip)	34
InP	(100)	0.42-0.51	Zinc-blended	Indentation (Vickers tip)	33
GaN	m-plane	1.55	Wurtzite	Nano-indentation (Berovich tip)	35
GaN	a-plane	1.59	Wurtzite	Nano-indentation (Berovich tip)	35
GaN	c-plane	2.12	Wurtzite	Nano-indentation (Berovich tip)	35
SiC	N/A	2.5-6.4	N/A	Micro-indentation (Vickers tip)	36
α-Al2O3	c-plane	1.63	Hexagonal	Nano-indentation (Vickers tip)	37

Si is the most extensively used semiconductor material in the electronics and photovoltaics industries. Many approaches have been demonstrated to obtain wafer-scale (4 inch) crystalline Si based flexible electronic and photovoltaic devices. Figure 3a shows a sub-50 µm-thick crystalline Si thin film exfoliated from a 500 µm-thick Si donor substrate (Figure 3b) with a smooth fracture surface (Figure 3c).[38] Free-standing Si thin film is mechanically weak, however, the Si thin film/metal stressor bi-layer system produced by crack-assisted layer transfer process is mechanically robust. In addition, the crack-assisted layer transfer process does not lead to any material loss while the commercial wafer sawing technology (*i.e.*, multi-wire sawing method) results in a significant material loss (*e.g.*, >40% loss for 180 μm-thick Si wafer), called kerf-loss.[39] The dramatically reduced kerf-loss is also a considerable benefit in crack-assisted layer transfer, especially for photovoltaic industry where cost is an important issue. The production of multiple Si thin films via consecutive crack-assisted layer transfers has also been experimentally demonstrated. Figure 3d shows the sequentially produced Si thin films from a single Si donor substrate via crack-assisted layer transfer process. Although the surface roughness gradually increased from 312 to 459 nm after the third production, the values are still very low compared with the one fabricated by conventional wafer sawing technology. As mentioned earlier, crack-assisted layer transfer process enables thickness control of the exfoliated semiconductors via a simple adjustment of stressor layer thickness. Figure 3e shows the exfoliated Si thin films with different thicknesses from 5.6 to 45 μm produced by varying the Ni stressor layer thickness. Thickness of the exfoliated films has to be carefully optimized towards device applications since different semiconductors present different optical absorption depth based on their bandgap properties and absorption coefficients (see Figure 3f).

Ge has been frequently used as a growth substrate for compound semiconductors such as GaAs and InGaP due to its identical lattice constant and relatively low-cost. For crack-assisted layer transfer of compound semiconductors, Ge is often used as the medium for crack propagation to separate the epitaxially grown III-V device layers on Ge growth substrates. Shahrjerid *et al*. demonstrated flexible InGaP/(In)GaAs tandem junction solar cell using epitaxial growth followed by the controlled spalling process.[40] The spalled InGaP/(In)GaAs device layer analyzed using TEM showed no visible crystalline defects. The final tandem solar cell exhibited a power conversion efficiency of 28.1% with lightweight and high flexibility.

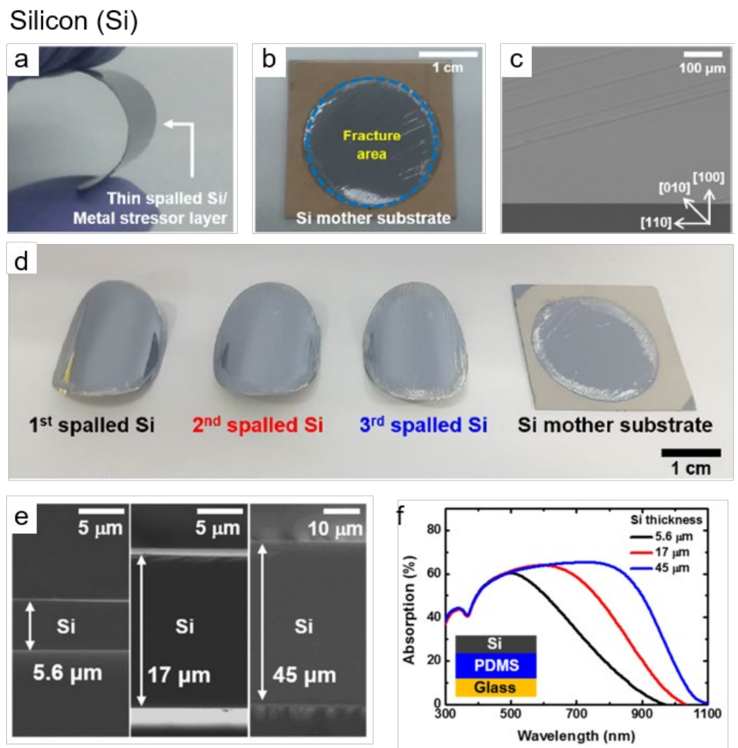

Figure 3. Crack-assisted layer transfer of bulk semiconductor substrates. (a) Spalled 1 inch diameter Si thin film (< 50 μm) with a stressor layer and (b) the left-over (100) orientation Si donor substrate. (c) Tilted-view scanning electron microscopy (SEM) image of the fracture surface of the Si donor substrate in (b). (d) Photograph of the multiple spalled Si/stressor layers obtained via consecutive crack-assisted layer transfers. (e) Cross-sectional SEM images of the spalled Si thin film with various thicknesses after stressor layer removal. The Si thickness (5.6 – 45 μm) was controlled by modification of the stressor layer thickness (10 – 25 μm). (f) Absorption property of

the spalled Si thin film as a function of its thickness. Reprinted with permission from ref.[38]. Copyright 2018, American Chemical Society.

InP is one of the promising candidates among III-V compound semiconductors for optoelectronic applications due to its direct bandgap, high electron mobility (5400 $cm^2/V{\cdot}s$), and low surface recombination velocity (10^4 cm/s for n-type, 10^5 cm/s for p-type).[41-42] Recently, we have shown crack-assisted InP layer transfer on zinc-blende InP substrate. The fracture surface morphology of InP is found to be highly dependent on the crystal orientation of InP donor substrate (see Figure 4).[43] It is well known that {110} plane is a preferred cleavage plane in zinc-blende III-V semiconductors due to its low fracture toughness compared to other prime planes.[44] Therefore, the crack tends to follow the {110} planes and it yields an extremely smooth surface on the fracture surface of (110) InP while a triangle shaped periodic grating structure is obtained on (100) InP (see Figure 4a-d). It is noted that the surface roughness of the exfoliated (110) InP thin film was found to be ~100 pm, which is extremely low, surpassing mirror-polished InP reference surface (~550 pm) achieved using a costly chemical mechanical polishing process. It is noteworthy that the extremely low surface roughness of the exfoliated (110) InP thin film can be beneficial for lateral wafer bonding process to produce heterojunction devices (*e.g.*, III-V on Si). We also showed controllability of the magnitude of the periodic grating structure by modification of the stressor layer thickness (see Figure 4f). The triangular grating structure shows a much reduced optical reflection in the visible wavelength range (300 – 900 nm, Figure 4g). This approach shows the feasibility for the formation of a periodic grating structure on exfoliated semiconductor thin film without the need of any additional etching process, which is a unique advantage of the crack-assisted layer transfer process compared to other layer transfer methods. The characterized material properties such as minority carrier lifetime show almost identical values compared to the reference substrate. It is noteworthy that this method enables the fabrication of micro-structures without any defect formation which is an issue in conventional micro/nano structure fabrication methods such as wet/dry etching process.

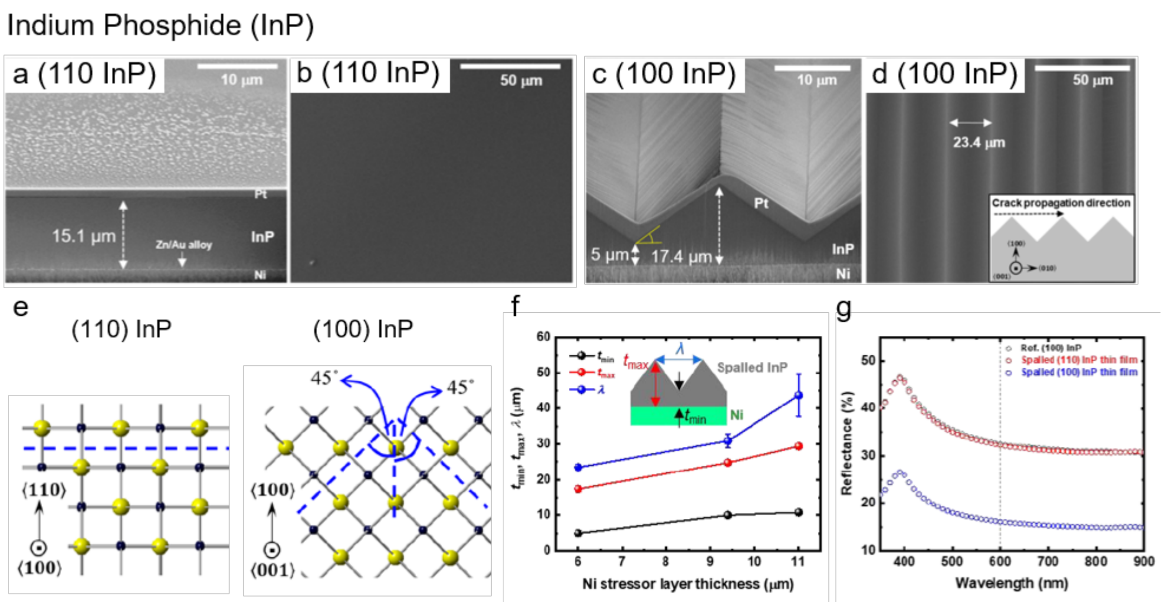

Figure 4. Periodic grating structure formation via crack-assisted layer transfer technology. Cross-sectional and top-view SEM images of the spalled InP thin film produced from (a-b) (110) and (c-d) (100) InP donor substrates. (e) Schematic illustration of the atomic arrangement of monocrystalline zinc-blende InP donor substrate with (110) and (100) orientation. (f) The magnitude of the periodic grating structure of spalled InP film with (100) orientation as a function of the stressor layer thickness. (g) optical reflection of the spalled (110) and (100) InP thin film with flat surface and grating structure as shown in (a-d), respectively. Reprinted with permission from ref.[43]. Copyright 2020, American Chemical Society.

GaAs is a mainstream III-V semiconductor having a direct bandgap of 1.42 eV, making it the highest efficiency single-junction photovoltaic device. Zinc-blende GaAs also shows a similar fracture tendency of InP yielding smooth surface for (110) orientation GaAs and periodic triangular grating structure for (100) orientation GaAs.[32, 45] Lee *et al*. showed that fracture morphology can be useful for photoelectrochemical hydrogen evolution which benefits from the triangular grating structure for reduced optical reflection and enhanced catalytic surface area.[38] In addition, the sub-20 μm-thick GaAs thin film photocathode, which was fabricated by the crack-assisted exfoliation from (100) orientation GaAs substrate, showed a photocurrent density of 22.4 mA/cm^2, which is identical to that of 350 μm-thick GaAs photocathode despite a dramatically reduced thickness.

GaN is a wide bandgap (3.4 eV) semiconductor widely used in LEDs, power electronics and photoelectrodes. It has a wurtzite crystal structure and strong ionic bond in contrast with the covalent bonding present in GaAs and InP. The strong ionic bonding makes GaN more tolerant to structural defects and high stability in acidic solutions.[46] Bedell *et al*. demonstrated 2-inch GaN thin film with ~20 μm thickness from [0001] oriented GaN substrate via controlled spalling process.[47] The fracture surface morphology of GaN shows an amplitude variation within a few micrometers over a length scale of several millimeters. Due to the m- and a-plane being the more appropriate cleavage planes than the [0001] plane, we anticipate that there is room to improve surface roughness on the fracture surface by applying crack-assisted layer transfer on these desired cleavage planes.[48] The TEM analysis of the fracture surface of exfoliated GaN thin film and GaN substrate exhibits no observable dislocations on both the surfaces indicating that the material quality remains the same as the reference bulk GaN substrate. The GaN thin film transfer via crack-assisted layer transfer enables facile exfoliation and reduced surface defects compare to that obtained via laser-lift off and ion-cut process.[49-50] The GaN/sapphire substrate is also a commonly used device structure in LED applications. However, the high fracture toughness (1.63 MPa√m) of sapphire limits the use of crack-assisted layer transfer in this material.[37] An epitaxially grown thick GaN buffer layer under the desired device layer can be used as a medium for crack propagation to exfoliate GaN based device layers from sapphire substrates.[51]

3.2. 2D Materials

3.2.1. Graphene

Two-dimensional (2D) materials have attracted huge attention from the global research community since their discovery. They show outstanding properties such as extremely high conductivity and mechanical strength compared with conventional bulk materials. 2D materials have an atomic thickness of several angstroms and high strength along the in-plane direction while weak interaction in the out-of-plane direction. One of the key requirements for the realization of 2D materials for practical device applications is the transfer of 2D materials from growth templates to target substrates without undesired defects such as wrinkles and tearing. Atomic-scale crack-assisted layer transfer process has been utilized to exfoliate 2D material from the growth templates such as silicon carbide (SiC) and copper substrates.

Typically, the transfer of graphene from its growth template consists of the deposition of a handling layer, followed by exfoliation of the graphene layers by applying mechanical force which is similar to the above-mentioned spalling mode fracture in bulk substrates. In this process, the most important parameter for designing atomic-scale crack-assisted layer transfer is the interfacial adhesion energy (*e.g.*, interfaces of 2D/2D materials, 2D material/growth template, and 2D material/handling layer).

Unarunotai *et al*. showed a selective transfer of the uppermost graphene monolayer from a multilayer graphene film on a SiC substrate.[52] Palladium (Pd) and polyimide layers were sequentially deposited on a multilayered graphene/SiC substrate. Then, an external force was applied with the help of a thermal adhesive tape attached on polyimide layer to propagate an edge crack at the interface between the uppermost graphene layer and the remaining graphene layers bonded to it. The crack propagation occurs at graphene/graphene interface due to its low adhesion energy. This process enabled single graphene monolayer transfer up to six times, with an area yield of almost 100% in the first two or three exfoliations. However, the exfoliation of the graphene layer from the SiC substrate was found to be more difficult due to the high adhesive energy between graphene and SiC substrate. Kim *et al*. showed the exfoliation of one or two graphene monolayers directly from SiC substrate.[53] Due to a higher difference in the binding energies per atom between graphene and Ni (~140 meV) compared to the one between graphene and SiC (~106 meV), graphene layer can be exfoliated from the SiC substrate via crack-assisted layer transfer. In addition, the authors showed that the excess graphene, known as narrow stripes formed by graphene growth on SiC, can be selectively removed with a second exfoliation process with Au film having moderate adhesion energy (~60 meV) with graphene layer. As a result, pure single graphene layers can be realized by making use of the adhesion property based on carefully designed metal thin film/graphene and repeated crack-assisted layer transfer processes.

Another noteworthy approach to transfer graphene from the growth template is the electrochemical delamination (or bubbling peel-off) method.[54-55] Wang *et al*. showed graphene layer delamination from a copper growth template by bubbling induced crack formation/propagation at the interface of graphene and copper substrate. In this process, the polyimide film working as a handling layer was coated on the top surface of graphene. The copper foil used as a graphene growth template serves as a cathode in an electrochemical cell, and hydrogen bubbles were generated at the copper foil surface when an electrical voltage was applied using Pt as a counter electrode. The generated hydrogen bubbles at the copper foil surface induce the delamination of the graphene/polyimide layer from the copper surface.

3.2.2. Other 2D Materials

A more universal approach has been recently reported to exfoliate various 2D materials such as hexagonal boron nitride (h-BN), WS_2, WSe_2, MoS_2, and $MoSe_2$ at wafer-scale. Shim *et al*. demonstrated various 2D monolayer exfoliation from 2D multilayers grown on sapphire substrates (Figure 5).[56] In this process, Ni layer was deposited on the top surface of 2D multilayer on sapphire substrate followed by spalling mode fracture. Due to a lowest interface toughness of 2D layer/sapphire (0.26 J/m^2) compared to the Ni/2D layer (1.4 J/m^2) and 2D layer/2D layer (0.45 J/m^2), the edge crack propagates at the 2D layer/sapphire interface. Subsequently, another Ni layer was deposited on the exposed surface of the 2D multi-layer film, followed by an additional spalling mode fracture process. In the second spalling step, edge crack propagates at the 2D/2D layer interface (Figure 5b), and as a result, only a single 2D monolayer is exfoliated onto the deposited Ni layer. Figure 5c shows the transferred wafer-scale (5 cm diameter) WS_2 monolayer from the SiC growth substrate onto an oxidized Si wafer. This approach has also been demonstrated for the transfer of other 2D materials such as h-BN, WS_2, WSe_2, MoS_2, and $MoSe_2$ via an identical crack-assisted layer transfer process.

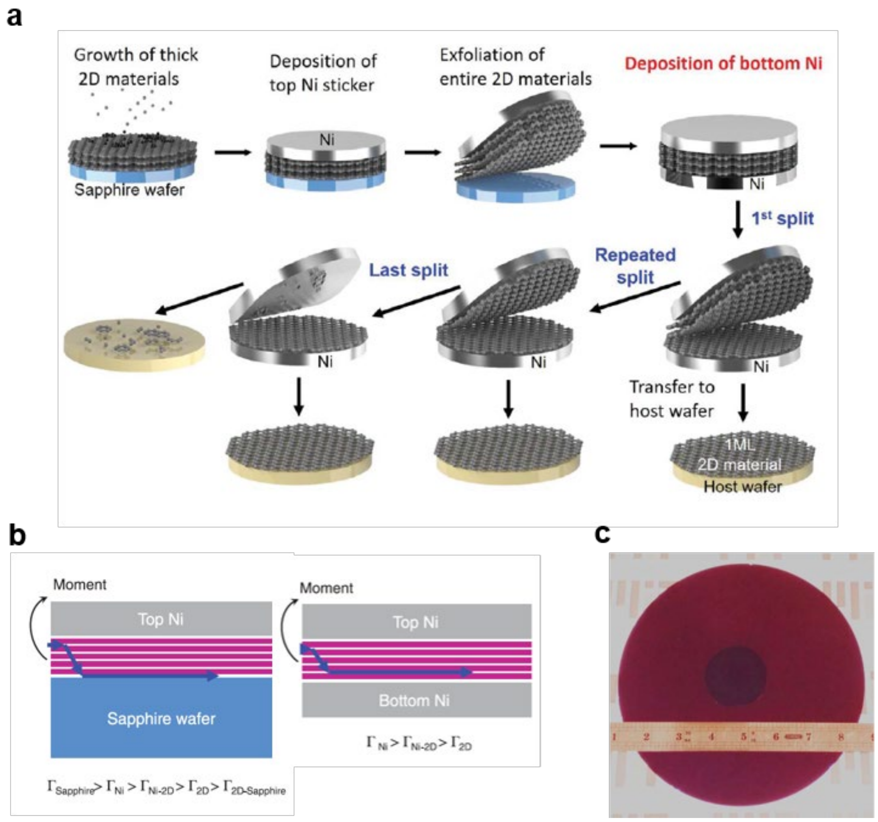

Figure 5. Crack-assisted atomic-scale 2D layer transfer. (a) Schematic illustration of crack-assisted 2D layer transfer from multiple graphene layers grown on sapphire template. (b) Schematic illustration of crack propagation mechanism for initial exfoliation of 2D materials from a sapphire growth template (left) and exfoliation of the bottom 2D material (right). (c) Optical image of the transferred WS_2 monolayer with 5 cm diameter on an oxidized Si wafer. Reprinted with permission from ref.[56]. Copyright 2018, American Association for the Advancement of Science (AAAS).

3.2.3. Nanowires

Semiconductor nanowires are attractive for their unique geometry-related optical and electrical properties. Generally, fracture toughness of nanowire semiconductor is higher than bulk substrates due to the reduced number of crack initiating defects in a given volume. For instance, Gordon *et al*. showed an enhancement of fracture toughness from 0.03 GPa in Si bulk substrate to 2-4 GPa in Si nanowires with a diameter between 100 – 700 nm.[57] In addition, the fracture toughness of Si nanowires was increased when the Si nanowire diameter was reduced in the diameter range of 300 – 940 nm.[58] Therefore, a higher pulling force has to be applied to exfoliate nanowire structured semiconductors compare to the bulk materials. In the crack-assisted nanowire transfer methods, however, nanowire structure gives more design freedom compared with bulk and 2D materials. For instance, the vertical surface of nanowires can be exposed providing opportunities for the formation of stress concentration structure, which can serve as the intended crack propagation position. Many research groups demonstrated Si nanowire transfer using polymer layer coating followed by a peel-off process. Plass *et al*. showed the Si nanowire transfer process from the (111) Si donor substrate.[59] A polymer layer was deposited and cured on the Si nanowire with a height of 100 μm. By pulling the cured polymer layer, the embedded Si nanowires were exfoliated from the Si substrate by crack initiation and propagation at the bottom side of the Si nanowires. In this process, the transfer yield of the Si nanowires is highly dependent on the adhesion force between the polymer layer and Si nanowires.[60]

Kim *et al*. developed a Si nanowire exfoliation method using an elastomeric substrate for Si nanoneedle templates.[61] Figure 6 shows the entire Si nanowire transfer process involving tapered undercut formation and elastomer swelling process. The authors showed Si nanowire formation with a tapered undercut at the bottom of the Si nanowire (Figure 6a). Subsequently, the pre-cured elastomer layer was bonded with the Si nanowires, and the top area of Si nanowires was embedded in the elastomer layer (Figure 6b). Immersion of the entire structure in a specific solution (*i.e.*, hexane and dichloromethane) makes the elastomer layer swell or expand. The elastomer layer swelling induces mechanical stress on the Si nanowire, which is concentrated mainly at the tapered undercut position (Figure 6c). Therefore, a crack is propagated at the tapered undercut position, and finally the Si nanowires can be exfoliated from the undercut position (Figure 6d and e). Si nanowire patch with a conformal elastomer substrate formed by this method is highly attractive for use in clinical applications.

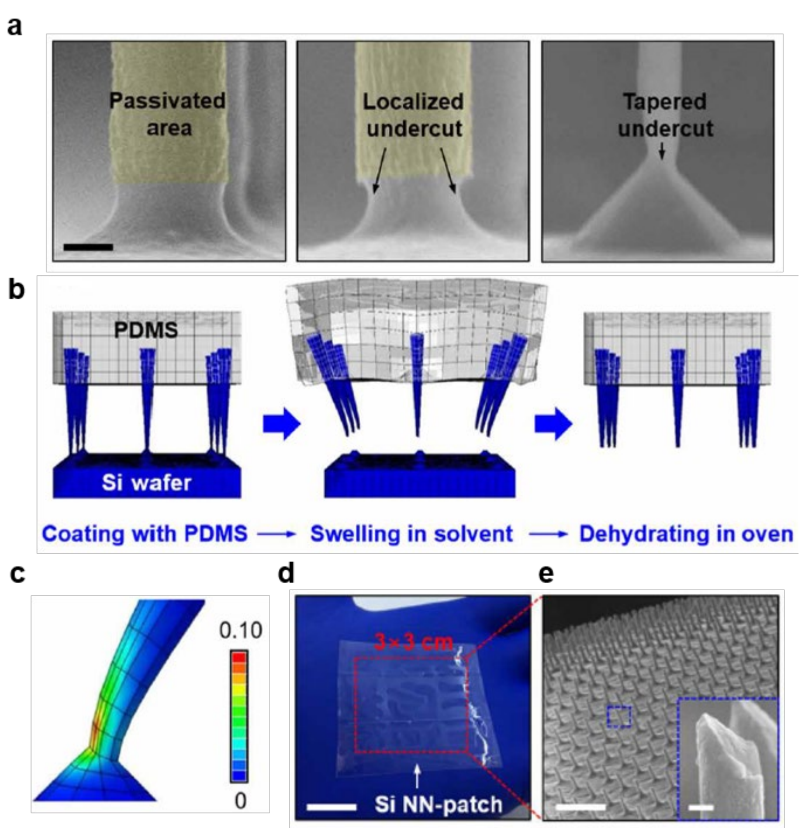

Figure 6. Crack-assisted nanowire transfer. (a) SEM images of Si micro/nanowire with a passivation layer, localized undercut, and tapered undercut (from left to right). The scale bar is 1

μm. (b) Schematic illustration of Si nanowire transfer with applied stress through PDMS swelling. (c) Finite element analysis results of principal strain distribution along a single Si nanowire during the swelling of PDMS. (d) Optical and (e) SEM images of an exfoliated Si nanowire with PDMS. Scale bar are 1.5 cm in (d) and 20 μm and 600 nm (inset) in (e). Reprinted with permission from ref.[61]. Copyright 2018, American Association for the Advancement of Science (AAAS).

Weisse *et al*. reported a Si nanowire transfer method with a porous sacrificial layer.[62] The authors showed that the formation of a sacrificial porous Si layer underneath the Si nanowire array by electro-assisted etching process, followed by a separation of the porous Si layer with Si nanowires from the donor Si substrate. The group also reported another Si nanowire transfer process, which shows controllable crack propagation position within Si nanowires.[63] The transfer process involves the formation of Si nanowires by Ag assisted electroless etching method. Next, a water soaking process is conducted to achieve a lateral direction etching of the Si nanowires to form a horizontal notch. Subsequently, an additional electroless vertical etching process, which is identical to the first step of forming nanowires, is carried out to form deep Si nanowires. Consequently, the entire process enables the formation of the Si nanowires embedded with a horizontal notch at the middle of the nanowire structure. When polymer deposition and peel-off process are conducted, the stress is concentrated at the lateral notch and therefore a crack expands in the lateral direction from the notch. This approach presents a facile strategy to determine the crack propagation position in Si nanowires, and external force for crack expansion can be dramatically reduced compared with the conventional approaches.

4. Crack-Assisted Layer Transfer with Interfacial Fracture Toughness Engineering

Although, crack-assisted layer transfer technology have seen many advances in the last decade, there still remains some limitations that need to be addressed. One important limitation of crack-assisted layer transfer is the undesired parasitic crack propagation, especially on bulk substrates, which leads to a relatively high surface roughness on the fracture surface compared to other layer transfer processes. For instance, Wallner line, which is created by the interaction between the crack propagation and the stress wave reflection at the crack front, is frequently observed in the fracture surface.[31] In addition, twist hackle pattern formed by the undesired mode III fracture due to edge boundary effect also appears in the edge area.[64] Therefore, further theoretical studies on parasitic crack propagation and development of practical approaches to eliminate parasitic cracks are needed. To solve this issue, various crack-assisted layer transfer methods have been reported that utilize interfacial fracture toughness engineering. The crack can be neatly extended to the intended location with minimized parasitic crack propagation by reducing the fracture toughness on a specific interface. Interfacial facture toughness engineering can be implemented in many different ways including changing the crystal structure, forming a mechanically weak structure beneath the top device layer, conducting a chemical reaction in a liquid solution, and utilizing remote epitaxy on slippery 2D materials.

4.1. Physical Lift-Off with a Modified Mo Layer

Figure 7a shows crack-assisted layer transfer via interfacial fracture toughness modification of Mo, referred to as Mo-based interfacial physical lift-off (IPLO) transfer method.[65] The sputter-deposited Mo layer shows that Mo crystal structure at the top surface can be transformed from an intrinsic body-centered cubic (BCC) to face-centered cubic (FCC) structure with high strain induced by an SiO_2 capping layer and additional heat treatment. Density functional theory (DFT) calculations show that the FCC structure is more stable than BCC structure under specific uniaxial tensile stress, and the interfacial fracture toughness at FCC/BCC has the lowest value of 1.56 J/m^2 while the fracture toughness of BCC and FCC structured are 2.37 and 2.44 J/m^2, respectively. Due to the lowest fracture toughness at the interface of FCC/BCC, the edge crack is propagated at the interface position when the physical lift-off process is conducted. The authors demonstrated flexible phase-change random access memory (f-PRAM) devices by pre-fabricated PRAM device layers on Mo and transfer onto flexible plastic films (polyethylene terephthalate) without significant degradation.

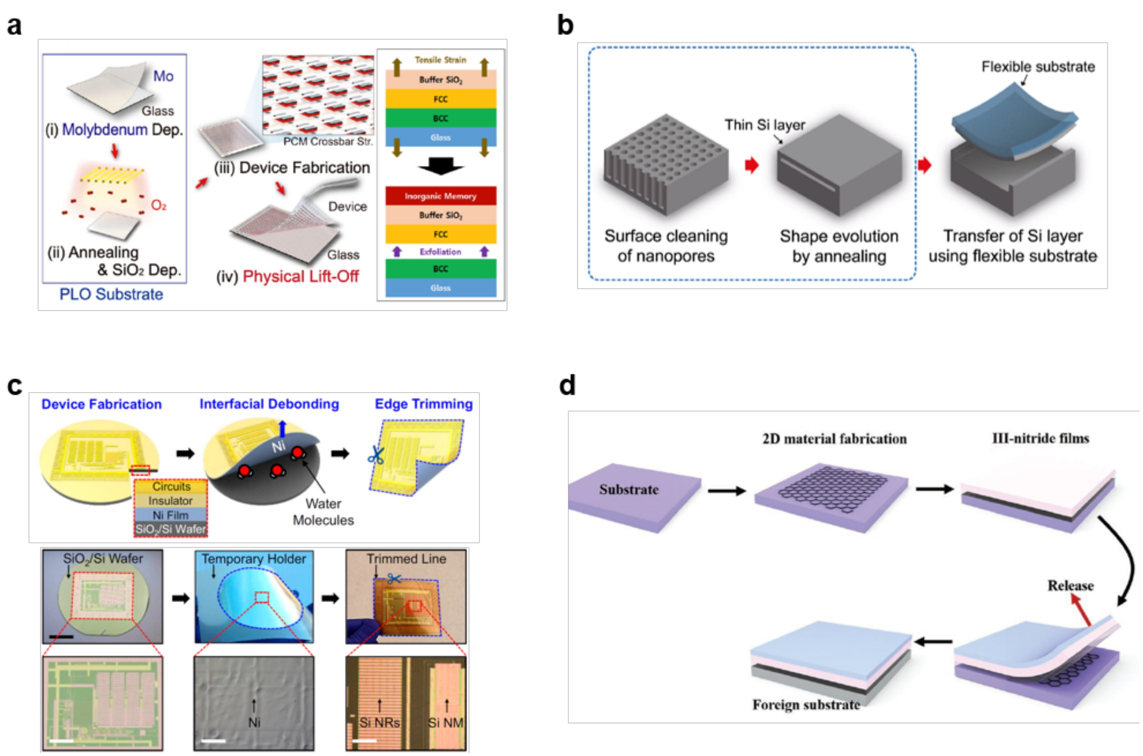

Figure 7. Crack-assisted layer transfer via interface fracture toughness engineering. (a) Schematic illustration of layer transfer via physical lift-off with a modified Mo layer. Reprinted with permission from ref.[7]. Copyright 2019, Elsevier. (b) Schematic illustration of layer transfer process based on a Si-on-Nothing (SON) structure. Reprinted with permission from ref.[66]. Copyright 2016, American Chemical Society. (c) Schematic illustrations of water-assisted thin film delamination process. Reprinted with permission from ref.[67]. Copyright 2018, National Academy of Sciences. (d) Schematic representation of the 2D material based layer transfer (2DLT) technique. Reprinted with permission from ref.[68]. Copyright 2019, John Wiley and Sons.

4.2. Layer Transfer using a Sacrificial Porous Layer

The formation of a mechanically weak layer such as a sacrificial porous layer on a donor substrate provides an appropriate approach compatible with the conventional semiconductor fabrication process. Figure 7b illustrates the layer transfer process involving crack propagation in the pre-defined sacrificial porous layer, called Si-on-Nothing (SON) technology.[66] In this approach, Si nanowires with a sufficiently high aspect ratio are first developed on a Si substrate. Subsequently, implementation of high temperature (~1100°C) annealing process in hydrogen atmosphere leads to reorganization of the Si nanowires, driven by surface energy minimization process, resulting in a thin crystalline Si layer (330 – 470 nm thickness) suspended on a void layer. The adhesive polymer layer is then bonded to the top Si layer, and the edge crack propagation occurs in the porous layer when mechanical peel-off process is initiated. Finally, the thin crystalline Si layer can be detached from the Si substrate. One of the strengths of this method is that it can utilize an epitaxial growth method, which typically requires high temperature process, to demonstrate monocrystalline semiconductor thin films and devices. The epitaxial Si (*i.e.*, epi-Si) growth on porous Si layer and separation of the epi-Si by cleaving the porous Si, referred to as Epitaxial Layer TRANsfer (ELTRAN), enables high-efficiency (>22%) photovoltaic devices at industrial scale.[69-70] For the high yield detachment of the epitaxial Si thin film from the donor substrate, the density and dimensions of the pillars in the sacrificial porous layer have to optimized.[71] Recently, Ge-on-nothing (GON) technology was also developed using the same strategy.[72] Smooth, uniform and defect-free Ge layers with ~300 nm thickness on voids were demonstrated by optimizing the initial pore geometry and suppressing the surface oxidation during the annealing process in hydrogen atmosphere. Due to an excellent surface uniformity (R_{rms} 5.7 nm) and high crystallinity of the suspended Ge layer, the epitaxially grown GaAs photovoltaic devices on the suspended Ge layer show almost identical performance compared to the one fabricated on reference Ge substrate. The authors showed the pre-fabricated GaAs photovoltaic device can be readily separated from its donor substrate by crack propagation on the Ge pillar from the edge using a UV adhesive and glass substrate as bonding material and handling substrate, respectively. This approach is highly interesting to significantly reduce the cost of the final device by reusing the expensive semiconductor substrate after the transfer process.

4.3. Water-Assisted Thin Film Delamination

Lee and coworkers reported a novel thin film transfer method by immersing metal thin film coated SiO_2/Si substrate in water solutions at room temperature.[73] When a Ni/SiO_2/Si substrate is immersed into water solution, the water molecules react with Ni-O-Si bonds formed at the Ni/SiO_2 interface, transforming it into Ni-O-H and Si-O-H bonds, respectively, on each side. The chemical reactions at the Ni/SiO_2 interface induce a reduction of the critical adhesion energy from 1.37 J/m^2 in air to 0.31 J/m^2 in water solution.[74] In addition, Ti and Cu thin films also show dramatically reduced critical adhesion energy in water solution. As a result, the crack can easily propagate at the Ni/SiO_2 interface in water solution than in atmosphere when the peel-off process is conducted. A theoretical study of the water-assisted thin film delamination showed that it is feasible to conduct wafer-scale layer transfer with almost 100% yield without any significant performance degradation of the exfoliated devices.[75] In the past decade, a range of devices including amorphous Si thin film solar cell,[73] nanowire electronic devices,[76] resistive random access memory (RRAM),[77] magnetic nano-devices,[78] solar absorbers for solar thermal energy conversion,[79] and super-capacitors[80] have been developed via water-assisted thin film delamination method. Wie *et al*. showed the integration of various nanomaterials (*e.g*., silver nanowire, crystalline Si nanomembranes, MoS_2) on Ni/SiO_2/Si substrate for the development of various functional devices, and separation of the fabricated device layer via water-assisted thin film delamination method.[67] The authors showed complex system-level demonstrations including a light emitting diode array controller with Si nanomembranes based metal-oxide-semiconductor field-effect transistors (MOSFETs), temperature sensors, and photodetectors. This approach not only shows the wafer-scale compatibility (4 inch), but also the ability to maintain the device performances intact after exfoliation. Similarly, graphene monolayer can be separated from the copper foil used as the growth substrate, by roll-to-roll mechanical delamination process in hot water (~50°C).[81] Recently, Magginetti *et al.* reported that CdS/CdTe thin films can also be readily lifted-off from SiO_2/Si substrates via water-assisted thin film delamination method due to the Te-rich layer at SiO_2 surface.[82] This approach makes it possible to use the conventional fabrication process such as high temperature annealing, which is otherwise not possible on flexible substrates such as plastic foil, by utilizing metal/SiO_2/Si substrate system. It also allows the transfer of fully fabricated device layers without needing any hazardous chemical etchants. Moreover, there is room for cost reduction by reusing the SiO_2/Si templates.

4.4. 2D Material-based Layer Transfer

Recently, a layer transfer technology utilizing remote epitaxy on a slippery graphene/growth template, called 2D material-based layer transfer (2DLT), has been developed (see Figure 7d).[83-84] The 2D material-based layer transfer technology consists of three main steps. First, remote epitaxial growth of a non-polar graphene layer is carried out on a crystalline growth substrate. This remote epitaxy method enables the growth of an epitaxial layer with identical crystal structure and orientation to that of the underlying growth substrate across the graphene layer. Second, a stressor layer is deposited on top of the as-grown epitaxial layer. Finally, the spalling mode fracture is applied to separate the epitaxial layer from the graphene/growth substrate. Due to the weak bonding between the epitaxial overlayer and slippery graphene, the crack readily propagates between the epitaxial layer and the graphene layer with the spalling mode fracture process. This method enables the transfer of epitaxial layer with high crystallinity, leaving the remaining surface of the graphene/growth substrate very clean without residues. Therefore the graphene/growth substrate can be re-used to produce another desired epitaxial layer without any additional treatment, which makes it a cost-effective approach. This approaches has been demonstrated on many single-crystalline materials from III-V semiconductors (*e.g.*, GaAs, InP, GaP, and GaN) to complex metal oxides (*e.g.*, $SrTiO_3$, $BaTiO_3$, $CoFe_2O_4$, $Y_3Fe_5O_{12}$, $Pb(Mg_{1/3}Nb_{2/3})O_3$, and $PbTiO_3$).[85-86] Furthermore, other 2D materials such as BN also can be used as interlayers for 2D material based transfer techniques.[84, 87]

5. Device Applications

Semiconductor thin films fabricated by crack-assisted layer technology can offer many advantages such as mechanical flexibility, lightweight, and low-cost. With these advantages, these semiconductor thin films have been applied in various (opto)electronic devices such as data processing or storage unit, energy harvesting devices, sensing units, 3D heterojunction device, and biomedical applications. Depending on the type of application, the requirements of crack-assisted layer transfer process also vary, which are described in detail as below.

5.1. Electronic devices

As mentioned above, semiconductor thin films produced by crack-assisted layer transfer process are sufficiently thin with high flexibility, which is a primary requirement for wearable applications. In addition, the stressor layer used for crack-assisted layer transfer process can be utilized as a mechanical backing layer. Therefore, the semiconductor thin film/stressor layer template presents an appropriate approach for flexible electronic devices. Crack-assisted layer transfer process has been demonstrated on conventional Si substrates, therefore the approach shows high compatibility with the existing CMOS technology and offers the potential as a cost-effective approach compared with the silicon on insulator (SOI) substrate-based layer transfer process. Zhai *et al*. demonstrated a wafer-scale flexible thin film transistor (*e.g*., p-MOSFETs and n-MOSFETs) fabricated by a standard 0.13 μm CMOS process from Si substrate using the crack-assisted layer transfer process (Figure 8a).[88] A flexible transistor circuit was demonstrated by fabricating a CMOS device layer on a conventional thick Si substrate followed by the exfoliation of the pre-fabricated device layer with a thicknesses of 25 -30 μm using the spalling process. This crack-assisted layer transfer process showed no significant degradation of transistor characteristics. For instance, the electron mobility in n-MOSFET before and after exfoliation was found to be 261 and 252 $cm^2/(Vs)$, respectively. The spalling process was successfully carried out on 8 inch wafer diameter, which is sufficient for industrial use, and the electrical performance of the exfoliated MOSFET device was similar compared with the one before the transfer process. Shahrjerdi *et al*. also showed an ultra-flexible Si integrated circuits by utilizing the spalling process and an ultrathin body Si on insulator (UTB-SOI) with a Si body thickness of 60 Å (Figure 8b).[40] In the spalling process, a ~10 μm-thick Si was exfoliated from the donor Si substrate, and the undesired Si was appropriately removed to maximize flexibility of the exfoliated electronic devices. As a result, ultra-thin Si device layers were demonstrated. This structure has a high potential for future applications with extreme mechanical bendability.

The flexible electronic devices fabricated by crack-assisted layer transfer process have been successfully demonstrated for micro-scale transistors without significant performance degradation. However, there are a few things to consider with crack-assisted layer transfer. A stressor layer is generally used for spalling mode fracture which induces mechanical strain in the exfoliated semiconductor thin film.[18] This phenomenon was even observed in the transferred semiconductor thin film on a foreign substrate even after the stressor layer has been removed.[40] Due to the mechanical strain in the stressor layer, the exfoliated thin film/stressor layer shows outward bending when an appropriate vacuum chuck or pressure-sensitive tape is not used.[18] The high curvature of the exfoliated semiconductor thin films with stressor layer limits minute alignment with micro/nano patterning for additional fabrication processes. Therefore, micro/nano patterning related processing has to be conducted before the crack-assisted layer transfer process. The mechanical strain also causes a crystal structure symmetry modification, induces changes to energy bands and carrier mobility.[89] These issues need to be carefully considered for use in various electronic devices.

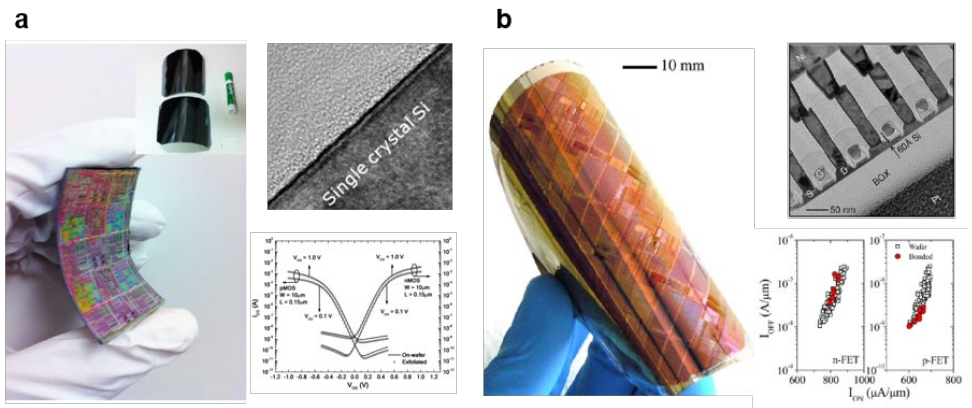

Figure 8. Representative flexible electronic devices. (a) Photographs of the flexible spalled Si with a CMOS unit (left). Cross-sectional TEM image of the exfoliated Si without significant damages (upper right). Measured MOSFET device characteristics before and after exfoliation (bottom right). Reprinted with permission from ref.[88]. Copyright 2012, American Chemical Society. (b) Photograph of the electronic device transferred to flexible plastic film via spalling process (left). Cross-sectional TEM image of spalled Si with nanoscale FET units (upper right). The n- and p-FET device performances before and after spalling process. Reprinted with permission from ref.[40]. Copyright 2013, American Chemical Society.

5.2. Photovoltaics

In the photovoltaic industry, Si is the most important material due to its good efficiency and cost-effectiveness. The cost of monocrystalline Si accounts for ~40% of the photovoltaic module system costs.[39] One of the main reasons for the high cost is the significant kerf-loss in the conventional wafering process, which is a wafer production process from Si ingots via slicing. For this reason, many attempts have been made to reduce the kerf-loss. The crack-assisted layer transfer method does not generate any material loss when exfoliating monocrystalline Si from the donor substrate, therefore this crack based wafering process provides a huge potential as to further reduce the cost of Si photovoltaics. Saha *et al*. demonstrated 25 μm-thick heterojunction Si solar cells with doped amorphous Si (a-Si) fabricated by the crack-assisted layer transfer process.[90] The bulk lifetime and implied open-circuit voltage of the spalled Si show similar values compared to a 500 μm-thick reference substrate despite the dramatically reduced thickness. The final heterojunction solar cell fabricated by spalled Si shows an open-circuit voltage, a short circuit current density, and a power conversion efficiency of 580 mV, 33.6 mA/cm^2, and 14.9%, respectively. Although the efficiency of the spalled Si based solar cell is relatively low compared to the industrial standard Si solar cell due to the non-optimized device fabrication, it shows the feasibility of obtaining moderate performance with a 25 μm-thick Si solar cell with high flexibility. It is noted that the crack-assisted layer transfer method may induce defects on the newly formed fracture surface of the spalled Si and donor substrate. Characterization of the fractured surface of the as-exfoliated Si via electron spin resonance (ESR) and photoluminescence (PL) imaging shows the defects cause significant reduction in the minority carrier lifetime.[28] The defects at the fracture surface can be appropriately removed by etching away a few micrometer thick Si from the fracture surface via wet-etching process.[64]

Another approach to demonstrate cost-effective heterojunction solar cells is through the utilization of 2D materials. Ahn *et al*. reported flexible graphene/Al_2O_3/Si heterojunction solar cells with 35 μm-thick Si.[91] It is noted that the reduced thickness results in insufficient light absorption at long wavelengths due to the indirect bandgap of Si. Appropriate light-trapping structures such as nano-scale inverted pyramids can enhance the optical path length and thus photon-to-current conversion efficiency can be enhanced.[92] In addition, the Si solar cell with reduced thickness can improve the open-circuit voltages with superior surface passivation.[93]

III-V semiconductors provide an excellent material platform to optimally convert sunlight to electricity. For instance, multi-junction solar cells based on III-V semiconductor show the highest efficiency among various material systems. However, the high cost of growth substrates, which accounts for more than 80% of the total cost of a GaAs solar cell, limits its practical application.[94] The crack-assisted layer transfer process can exfoliate the as-grown multi-junction solar cells from the costly growth substrates, and allows the reuse of the growth substrates after an appropriate post-treatment such as chemical-mechanical polishing, which offers a strong potential for cost-reduction of III-V based solar cells. Techno-economic analysis of III-V solar cells with the crack-assisted layer transfer process shows significant cost reduction of GaAs solar cells to around 1/10 from the conventional approaches.[94] For the crack-assisted layer transfer with III-V solar cells, the appropriate growth substrate, which is lattice-matched with the desired solar cell active layers (*e.g.*, GaAs, InGaP, and InGaAs), has to be considered. Sweet *et al*. showed the exfoliation of epitaxially grown single-junction GaAs solar cell from (100) orientation GaAs substrate by the crack-assisted layer transfer.[45] The GaAs solar cell showed a power conversion efficiency of 18.4%, without any significant performance degradation compared to reference solar cells. However, the grating structure formed on the fracture surface of the (100) orientation GaAs thin film and the donor substrate, has to be removed to allow additional epitaxial growth and exfoliation. This requires additional processing that results in an increased material-loss, which has to be minimized. This problem can be addressed by using Ge substrates for epitaxial growth and exfoliation with minimized additional processing and material-loss due to the relatively smooth fracture surface on Ge wafers after the crack-assisted layer transfer process. The epitaxially grown InGaP/(In)GaAs dual-junction solar cell showing an efficiency of ~28.1% was exfoliated from the Ge donor substrate without signification degradation in material properties (Figure 9).[95] This III-V solar cell exfoliated from rigid Ge donor substrate shows high flexibility as well as high specific power which is highly sought for air/space applications.

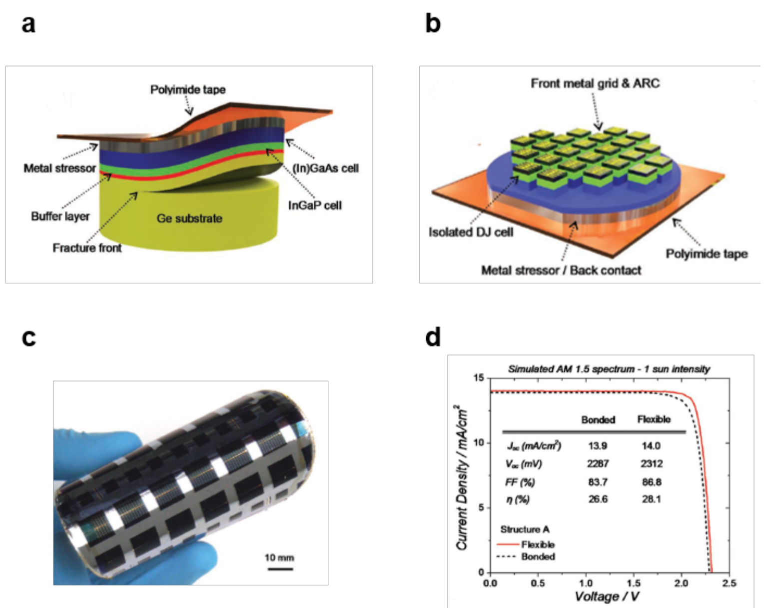

Figure 9. Representative flexible photovoltaic devices demonstrated by controlled cracking method. (a) Exfoliation of the epitaxially grown InGaP/(In)GaAs solar cell structure from a Ge donor substrate via controlled spalling process. (b) Schematic illustration of an InGaP/(In)GaAs solar cell arrays. (c) Photograph of the flexible the 100 mm diameter InGaP/(In)GaAs tandem solar cell arrays on a plastic carrier. (d) Light current-density vs voltage curve of the spalled InGaP/(In) GaAs tandem solar cell on a flexible plastic substrate (red solid line) and on a rigid Si wafer (black

dotted line) under AM 1.5G illumination. Reprinted with permission from ref.[96]. Copyright 2013, John Wiley and Sons.

5.3. Photoelectrochemical water splitting

Photoelectrochemical (PEC) water splitting enables direct splitting of water into H_2 and O_2, to produce a carbon-free energy fuel, using sunlight. Various semiconductor materials have been investigated as solar absorbers and monocrystalline semiconductors such as Si, III-V, and III-N, show high solar-to-hydrogen efficiencies compared to other amorphous materials. Similar to photovoltaic devices, the material cost is an important issue to address for industrial-scale manufacture of PEC water splitting devices. Therefore, crack-assisted layer transfer process has been used to demonstrate thin monocrystalline semiconductor based PEC devices without material loss as discussed above.

Lee *et al*. demonstrated spalled Si for photoelectrochemical cell applications.[38] Pt nanoparticle coated 16 μm-thick spalled Si photocathodes with np^+ rear junction shows a photocurrent density of 20.1 mA/cm^2 at 0 V (vs reversible hydrogen electrode, RHE) and an onset potential of 332 mV (vs RHE) in acid electrolyte. Although the crack-assisted layer transfer process produced high quality thin Si, the indirect bandgap of Si resulted in low optical absorption. The measured light absorption property of spalled Si rapidly decreased with reduced Si thickness at long wavelength (600 – 1000 nm). Therefore, an appropriate light-trapping structure has to be accompanied with the exfoliated Si thin film towards realizing high performance for sunlight absorption. III-V semiconductors such as GaAs and InP have direct bandgaps, therefore only a few micrometer thicknesses is enough to absorb solar irradiated light. In addition, the fracture plane in zinc-blende III-V semiconductors is confined on (100) plane, which has the lowest fracture toughness compared with the other primary planes. Therefore, micro-scale period grating structure can be readily formed on (100) orientation GaAs and InP substrate using the crack-assisted layer transfer process without the need for additional etching process. The grating structure on the fracture surface can reduce optical reflection as well as increasing the surface area, which can improve chemical reactions in water splitting photoelectrodes. Using this approach, a sub-20 μm-thick spalled p-GaAs photocathode was shown to have similar performance to that of the 350 μm-thick p-GaAs photocathode.[38] Zho *et al*. showed a new approach to demonstrate ultrathin $BiVO_4$ photoanode film with 80 nm thickness transferred from planar substrate to textured PDMS substrate via water-assisted thin film delamination method.[97] The authors demonstrated that the photo-current density of $BiVO_4$ photoanode can be enhanced by utilizing a patterned bottom substrate with an appropriate light-trapping structure compared to the planar substrate.

5.4. Light-emitting diode

Light-emitting diodes (LEDs) usually require multi-quantum-well (MQW) structure developed using epitaxial growth techniques for efficient light-emitting properties. There have been many attempts to exfoliate epitaxially grown MQW layers from the growth substrates using controlled crack propagation at the interface. The exfoliated MQW based LEDs can then be assembled into a vertical-type LED device structure with contact layers at the top and bottom position of the device, which help to achieve efficient heat dissipation. Bedell *et al*. demonstrated the exfoliation of a 3 μm-thick InGaN/GaN epitaxial MQW LED layer from a 50 mm diameter sapphire growth template using the crack-assisted layer transfer.[51] Due to the high fracture toughness of sapphire, epitaxially grown GaN buffer layer under the LED device layer was used as a medium for crack propagation. Subsequently, the exfoliated GaN LEDs were transferred to other inexpensive foreign substrates to demonstrate vertical-type LED. The demonstrated vertical LED presented a relatively high turn-on voltage (~200 mV) compared to the reference sample due to a non-optimized metallization process, however it shows the feasibility of wafer-scale demonstration of vertical-type LED via crack-assisted layer transfer technology. As mentioned earlier, 2D materials can also be used as a growth template and release layer. Chung *et al*. reported the growth of InGaN/GaN MQW LED structure on high-density ZnO nanowalls/graphene layer/substrate and its exfoliation from the graphene layer by crack propagation at the interface of graphene and substrate (Figure 10 a-b).[98] In addition, the graphene layer was also utilized as the bottom electrode. However, the slightly higher turn-on voltage due to unoptimized energy barriers at the junction of GaN/ZnO/graphene remains a challenge to be addressed. Similar to graphene, h-BN can be used as a release layer. In addition, the h-BN itself is a nitride semiconductor on which GaN based layers can be directly grown uniformly. Kobayahi *et al*. demonstrated the growth of GaN based LED layer on h-BN/sapphire substrate and exfoliation of the GaN based LED layer by crack propagation from the 3 nm-thick h-BN layer.[99] The authors proved that the crack-assisted layer transfer process does not result in any material quality degradation in the transferred GaN based LED, with an extremely low surface roughness of < 1 nm on the fractured surface, which is considerably lower than the one obtained by the conventional laser lift-off process. Recently, Jeong *et al*. demonstrated vertical-type micro-rod GaN LEDs which offers an ideal geometry for flexible devices via 2DLT technique (Figure 10c-e).[100] The exfoliated micro-rod GaN LEDs show superior mechanical stability on device damages such as partial edge cutting as shown in Figure 10e.

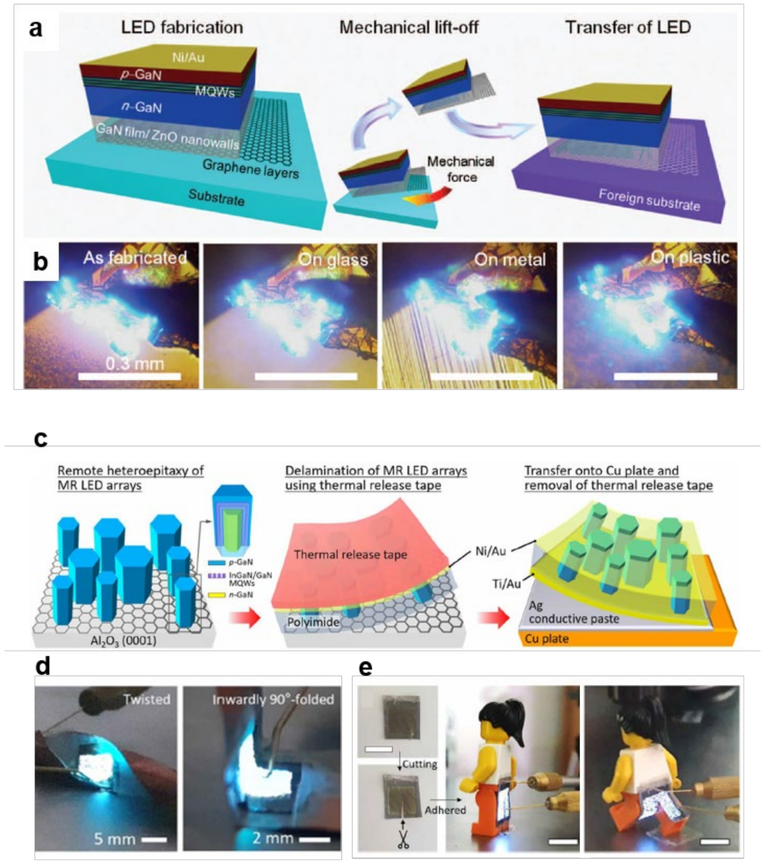

Figure 10. Representative flexible light-emitting diodes (LEDs) from the crack-assisted transfer process. (a) Schematic illustration of the crack-assisted transfer process for GaN multi-quantum-well (MQW) LEDs grown on graphene/sapphire substrate. (b) Photographs of light emission from the as-fabricated GaN MQW LED on the original graphene/sapphire substrate and after the transfer process on various foreign substrates such as metal, glass, and plastics. Reprinted with permission from ref.[98]. Copyright 2010, American Association for the Advancement of Science (AAAS). (c) Schematic illustration of the fabrication process for micro-rod LEDs grown on graphene/sapphire substrate. (d) Photographs of the micro-rod LEDs deformed in various shapes and (e) attached to a minifigure after partial cutting. Reprinted with permission from ref.[100]. Copyright 2020, American Association for the Advancement of Science (AAAS).

5.5. Sensors

Wearable tactile sensors can acquire human physiological and activity information and this data can be utilized in a wide range of applications such as healthcare monitoring, entertainment, and security. In a tactile sensor, single crystalline semiconductor materials such as Si show several advantages such as high sensitivity, low hysteresis, long-term stability, good uniformity, and compatibility with the conventional CMOS based readout circuitry.[101] Sakuma *et al*. showed a 40 μm-thick strain/force sensor using a bar-shaped spalled Si. The strain/force sensor exhibits a force sensitivity of around 0.6%/N under a perpendicular applied force in a three-point bending test.[102] Li *et al*. reported an advanced crack-assisted layer transfer, referred to as 3D spalling process, and the demonstration of a tactile sensor with a serpentine piezoresistor using an exfoliated Si thin film.[103] By utilizing patterning and modification of the stressor layer thickness, the spalling process exhibits 3D control over the shape and thickness of the exfoliated semiconductor thin films. The tactile sensor made using the exfoliated Si thin film exhibits satisfactory strain sensitivity by showing a gauge factor of 60 with various bending radii.

The spalled Si thin film template can also be used as light and temperature measurement sensors, which are essential for artificial skin applications. The light sensor configured into a Wheastone bridge network using the spalled Si thin film shows a decreased resistance with increasing illumination intensity due to an increase in carriers generated by the incident light.[103] The exfoliated Si thin film based temperature sensor exhibited a temperature coefficient of -0.44%/°C in the range of 34 to 50 °C which covers the temperature range of a human body (36.5 – 37.5°C).[102]

5.6. Optical filters

In 2011, Seo *et al*. reported the successful demonstration of multi-color generation with vertical Si nanowire array by utilizing their optical resonances.[104] The resonant wavelength of Si nanowire arrays can be tuned by controlling the geometrical parameters such as its size, shape, and period. Since then, optical filters based on Si nanowires have attracted huge interest in various optical applications such as image sensor devices. One of the dominant approaches involves the exfoliation of pre-fabricated Si nanowires on a Si donor substrate by making use of a transparent polymer substrate. Park *et al*. demonstrated that PDMS-embedded vertical Si nanowires as a color filter that shows tunability of optical reflection and transmission when the diameter of vertical Si nanowires is modified.[105] The authors showed the Si nanowire-based color filter with an image sensor can be efficiently used in a multi-spectral imaging system. PDMS embedded with a Si nanowire-based color filter can exhibit enhanced tunability of the generated color when additional bottom optical resonators such as amorphous Si/metal or metal/insulator/metal structure are incorporated.[106-107] Recently, Lee *et al*. demonstrated tunable multiple band optical filters by stacking multiple PDMS layers containing Si nanowires with different diameters. The multi-band optical filter shows efficient screening of the undesired wavelength for elaborate fluorescence tissue imaging.[108]

5.7. Biomedical applications

Nanowires have attracted huge interest in drug delivery applications, however, the rigid bulk materials beneath the nanowires limits their wider usage in biomedical applications, which require flexibility and stretchability. Nanowires transfer from a rigid donor substrate by the crack-assisted layer transfer process could solve this problem. Mumm *et al*. demonstrated a low-cost, disposable, and cell-culture compatible impalefection device with copper oxide (CuO) nanowires.[109] The detached CuO nanowires from a Cu substrate were transferred to transparent substrates such as glass. The fabricated CuO nanowires template was used to study cargo delivery and detailed cell-nanowire interfaction. Kim *et al*. showed the transfer of Si nano-needles structure using crack-assisted layer transfer with mechanical stress concentration at pre-defined fracture points.[61] Using the pre-defined fracture points, Si nanowires can be readily detached with uniform depth. The fabricated Si nano-needles transferred from rigid Si substrates to stretchable elastomer layers provide the ability to intimately contact the cells and living biological tissues, which is a useful function in intradermal and intramuscular delivery of biomolecules. The demonstrated Si nanoneedles embedded in an elastomer layer enables efficient injection of biomolecules as well as facile observation of cells during their interactions with Si nanoneedles. Recently, an identical Si needles patch has been developed with water-soluble medical films such as poly(vinyl alcohol) (PVA) instead of the PDMS layer (Figure 11). The bioresorbable materials based on Si nanoneedle patches show the advantages of unobtrusive topical delivery as well as facile removal of the used tools, thereby inducing minimal side effects.[110]

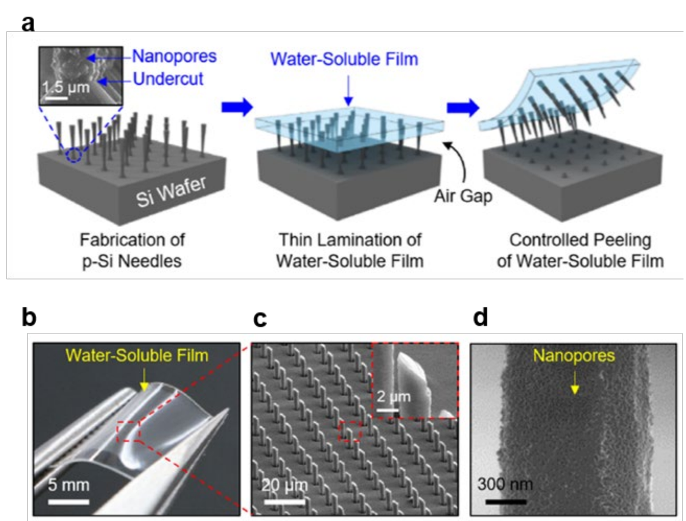

Figure 11. Representative flexible Si nanonedles with nanopores utilized for chemotherapy. (a) Schematic illustration of the fabrication process of Si nanoneedles on a water-soluble film. (b) Photograph and (c) SEM images of the transferred Si nanoneedles on water-soluble film. (d) SEM image of the side walls of silicon nanoneedles showing the nanopores. Reprinted with permission from ref.[110]. Copyright 2020, American Chemical Society.

Conclusions and Future Perspective

Remarkable advancements have been made in the development of various crack-assisted layer transfer technologies for numerous emerging applications such as mHealth, smart cities, IoT, and wearable (opto)electronic devices. In this review paper, we briefly explain the crack-assisted layer transfer process which provides a simple way to exfoliate thin crystalline semiconductors with various morphologies (*e.g.*, thin films, 2D layers, and nanowires) from their donor substrates by controlling the crack propagation direction. Crack-assisted layer transfer process does not require costly equipment and complex fabrication steps. In addition, it shows feasibility for wafer-scale (> 4 inch) exfoliation, compatibility with conventional CMOS technology, and universality on various brittle semiconductor materials.

There are many opportunities to broaden the application of crack-assisted layer transfer technique in (opto)electronic industry with a further scope for cleverly designed approaches. Further work is needed to realize industrial-scale demonstrations with high throughput. The stressor layer deposition on the target semiconductor substrate can be conducted by industrial-friendly approaches such as spin-coating, screen printing, and slot-die coating method. The adhesion force between the stressor layer and the target substrate should also be carefully controlled. Laser ablation method can be used to form the initial crack near the stressor layer. The controlled cracking process can be developed as an automated roll-to-roll transfer printing with the stressor layer deposited target substrate bonded with an adhesive tape which can be mechanically lifted-off by applying an external force for sub-surface crack propagation. Innovation in equipment design, process recipe, thin film handing, and system optimization is needed to industrialize this technology.

Despite the significant progress achieved in the field of crack-assisted layer transfer technology, many key challenges remain to be addressed. In the process of the sub-surface cracking, parasitic crack propagation is frequently observed which induces high surface roughness and undesired surface structure formation on the fractured surface. Further efforts should be made to minimize these undesired results. It also requires an in-depth study of the fracture surface morphology under different crack propagation conditions (*e.g.*, crack propagation velocity). For light emitting/absorbing device, surface texturing is one of the powerful approaches to enhance their performance. However, the surface structure formation on a semiconductor thin film may introduce stress concentration regions. This induces an undesired breaking of the semiconductor thin film causing a dramatic reduction of the device lifetime in flexible device applications. In addition, structural defects located at the edge of an exfoliated semiconductor thin film can also act as stress concentration points. Therefore, an appropriate design of the surface structure and minimization of edge defects are required to avoid these problems. While great attention has been paid to demonstrate ultrathin semiconductor thin films for device applications, stress induced effect on the electronic properties (*e.g.*, carrier mobility, energy bandgap, etc.) of the semiconductor thin film devices fabricated by crack-assisted transfer has yet to be studied in detail. The variation of the electronic properties of semiconductor thin films induced by external stress due to bending poses challenges to the utilization of complex and sensitive electronic devices such as state-of-art CMOS based circuits.

Although there remains many challenges yet to be addressed, the above considerations suggest that the field of crack-assisted layer transfer is highly promising with newly emerging fabrication methods in brittle semiconductor materials. We speculate that, eventually, widespread flexible (opto)electronic devices with high performance and reduced production costs will be realized, supported by continuous innovations in the crack-assisted layer transfer process in the near future.

AUTHOR INFORMATION

Corresponding Author

yhlee @geri.re.kr, siva.karuturi@anu.edu.au

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENT

We acknowledge the Australian Research Council (ARC) and the Australian Renewable Energy Agency (ARENA) for financial support. This work is conducted under the framework of the Research and Development Program of the Korea Institute of Energy Research (B7-2426).

REFERENCES

(1) Gupta, S.; Navaraj, W. T.; Lorenzelli, L.; Dahiya, R. Ultra-Thin Chips for High-Performance Flexible Electronics. *npj Flexible Electron.* **2018,** *2* (1), 1-17.

(2) Xu, H.; Yin, L.; Liu, C.; Sheng, X.; Zhao, N. Recent Advances in Biointegrated Optoelectronic Devices. *Adv. Mater.* **2018,** *30* (33), 1800156.

(3) Konagai, M.; Sugimoto, M.; Takahashi, K. High Efficiency GaAs Thin Film Solar Cells by Peeled Film Technology. *J. Cryst. Growth* **1978,** *45*, 277-280.

(4) Voncken, M.; Schermer, J.; Bauhuis, G.; Mulder, P.; Larsen, P. Multiple Release Layer Study of the Intrinsic Lateral Etch Rate of the Epitaxial Lift-Off Process. *Appl. Phys. A* **2004,** *79* (7), 1801-1807.

(5) Lee, K.; Zimmerman, J. D.; Hughes, T. W.; Forrest, S. R. Non-Destructive Wafer Recycling for Low-Cost Thin-Film Flexible Optoelectronics. *Adv. Funct. Mater.* **2014,** *24* (27), 4284-4291.

(6) Cheng, C.-W.; Shiu, K.-T.; Li, N.; Han, S.-J.; Shi, L.; Sadana, D. K. Epitaxial Lift-Off Process for Gallium Arsenide Substrate Reuse and Flexible Electronics. *Nat. Commun.* **2013,** *4* (1), 1-7.

(7) Park, J. H.; Lee, H. E.; Jeong, C. K.; Hong, S. K.; Park, K.-I.; Lee, K. J. Self-Powered Flexible Electronics beyond Thermal Limits. *Nano Energy* **2019,** *56*, 531-546.

(8) Bian, J.; Zhou, L.; Wan, X.; Zhu, C.; Yang, B.; Huang, Y. Laser Transfer, Printing, and Assembly Techniques for Flexible Electronics. *Adv. Electron. Mater.* **2019,** *5* (7), 1800900.

(9) Ashby, M. F.; Shercliff, H.; Cebon, D. *Materials: Engineering, Science, Processing and Design*; Elsevier: Cambrige, **2019**.

(10) Suo, Z. *Encyclopedia of Materials: Science and Technology;* Elsevier: Amsterdam, **2001**.

(11) Evans, A.; Drory, M.; Hu, M. The Cracking and Decohesion of Thin Films. *J. Mater. Res.* **1988,** 3 (5) 1043-1049.

(12) Suo, Z.; Hutchinson, J. W. Steady-State Cracking in Brittle Substrates Beneath Adherent Films. *Int. J. Solids Struct.* **1989,** *25* (11), 1337-1353.

(13) Thornton, J. A.; Hoffman, D. Stress-Related Effects in Thin Films. *Thin Solid Films* **1989,** *171* (1), 5-31.

(14) Sakuma, K. *Flexible, Wearable, and Stretchable Electronics*; CRC Press: Boca Raton, **2020**.

(15) Lee, Y. H. Fabrication and Characterization of Ultra-Thin Semiconductors for Solar Energy Conversion Devices using Spalling Process. Doctoral dissertation, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, **2018**; pp10-14.

(16) Hohenwarter, A.; Pippan, R. Fracture Toughness Evaluation of Ultrafine-Grained Nickel. *Scr. Mater.* **2011,** *64* (10), 982-985.
(17) Thornton, J. A.; Hoffman, D. W. Internal Stresses in Titanium, Nickel, Molybdenum, and Tantalum Films Deposited by Cylindrical Magnetron Sputtering. *J. Vac. Sci. Technol.* **1977,** *14* (1), 164-168.
(18) Bedell, S. W.; Fogel, K.; Lauro, P.; Shahrjerdi, D.; Ott, J. A.; Sadana, D. Layer Transfer by Controlled Spalling. *J. Phys. D: Appl. Phys.* **2013,** *46* (15), 152002.
(19) Giallonardo, J.; Erb, U.; Aust, K.; Palumbo, G. The Influence of Grain Size and Texture on the Young's Modulus of Nanocrystalline Nickel and Nickel–Iron Alloys. *Philos. Mag.* **2011,** *91* (36), 4594-4605.
(20) Luo, J.; Pritschow, M.; Flewitt, A.; Spearing, S.; Fleck, N.; Milne, W. Effects of Process Conditions on Properties of Electroplated Ni Thin Films for Microsystem Applications. *J. Electrochem. Soc.* **2006,** *153* (10), D155.
(21) Kwon, Y.; Yang, C.; Yoon, S.-H.; Um, H.-D.; Lee, J.-H.; Yoo, B. Spalling of a Thin Si Layer by Electrodeposit-Assisted Stripping. *Appl. Phys. Express* **2013,** *6* (11), 116502.
(22) Yang, C.; Moon, K.; Song, J.-W.; Kim, J.; Lee, J.-H.; Lim, J.-H.; Yoo, B. Spalling of Thin Si Layer via Electroless and Electrodeposit-Assisted Stripping (E2AS) with All-Wet Process for Fabrication of Low-Cost Flexible Single-Crystalline Si Solar Cell. *J. Electrochem. Soc.* **2018,** *165* (5), D243.
(23) Dross, F.; Robbelein, J.; Vandevelde, B.; Van Kerschaver, E.; Gordon, I.; Beaucarne, G.; Poortmans, J. Stress-Induced Large-Area Lift-Off of Crystalline Si Films. *Appl. Phys. A* **2007,** *89* (1), 149-152.
(24) Du, C.-H.; Chen, C.-H.; Wang, T.-Y.; Hsiao, J.-C.; Yeh, C.-M.; Chen, C.-H.; Yeh, J. A.; Yu, P. Fabricating 43-μm-Thick and 12% Efficient Heterojunction Silicon Solar Cells by using Kerfless Si (111) Substrates. *ECS J. Solid State Sci. Technol.* **2015,** *4* (8), P319.
(25) Masolin, A.; Bouchard, P.-O.; Martini, R.; Bernacki, M. Thermo-Mechanical and Fracture Properties in Single-Crystal Silicon. *J. Mater. Sci.* **2013,** *48* (3), 979-988.
(26) Martini, R.; Gonzalez, M.; Dross, F.; Masolin, A.; Vaes, J.; Frederickx, D.; Poortmans, J. Epoxy-Induced Spalling of Silicon. *Energy Procedia* **2012,** *27*, 567-572.
(27) Martini, R.; Granata, S.; Depauw, V.; Gonzalez, M.; Gordon, I.; Poortmans, J. Solar Cell

Processing of Foil Produced by Epoxy-Induced Spalling of Silicon. *Energy Procedia* **2014,** *55*, 879-884.

(28) Martini, R.; Kepa, J.; Debucquoy, M.; Depauw, V.; Gonzalez, M.; Gordon, I.; Stesmans, A.; Poortmans, J. Thin Silicon Foils Produced by Epoxy-Induced Spalling of Silicon for High Efficiency Solar Cells. *Appl. Phys. Lett.* **2014,** *105* (17), 173906.

(29) Dunn, B. D. *Materials and Processes: for Spacecraft and High Reliability Applications*; Springer: Switzerland, **2016**.

(30) Jeon, J.; Yu, S.; Yang, C.; Jin, S.; Roh, J.; Jung, J.; Yoo, B. Effect of the Laser-Scribing on Spalling of a Single Crystalline Si Using Electrodeposition Assisted Stripping (EAS) Process. *J. Nanosci. Nanotechnol.* **2016,** *16* (10), 10670-10674.

(31) Bellanger, P.; Slaoui, A.; Minj, A.; Martini, R.; Debucquoy, M.; Serra, J. M. First Solar Cells on Exfoliated Silicon Foils Obtained at Room Temperature by the SLIM-Cut Technique using an Epoxy layer. *IEEE J. Photovolt.* **2016,** *6* (5), 1115-1122.

(32) Bedell, S. W.; Shahrjerdi, D.; Hekmatshoar, B.; Fogel, K.; Lauro, P. A.; Ott, J. A.; Sosa, N.; Sadana, D. Kerf-Less Removal of Si, Ge, and III–V Layers by Controlled Spalling to Enable Low-Cost PV Technologies. *IEEE J. Photovolt.* **2012,** *2* (2), 141-147.

(33) Ericson, F.; Johansson, S.; Schweitz, J.-Å. Hardness and Fracture Toughness of Semiconducting Materials Studied by Indentation and Erosion Techniques. *Mater. Sci. Eng. A* **1988,** *105*, 131-141.

(34) Chen, C. *Fracture Mechanics Evaluation of GaAs: Final Report*; California Institute of Technology: CA, USA, **1984**.

(35) Cheng, Y.; Cai, D.; Wang, H.; Wu, J.; Liu, X.; Zhang, G.; Yu, T. Anisotropic Fracture Toughness of Bulk GaN. *Phys. Status Solidi B* **2018,** *255* (5), 1700515.

(36) Kaur, S.; Cutler, R. A.; Shetty, D. K. Short-Crack Fracture Toughness of Silicon Carbide. *J. Am. Ceram. Soc.* **2009,** *92* (1), 179-185.

(37) Wang, N.; Jiang, F.; Xu, X.; Lu, X. Effects of Crystal Orientation on the Crack Propagation of Sapphire by Sequential Indentation Testing. *Crystals* **2018,** *8* (1), 3.

(38) Lee, Y. H.; Kim, J.; Oh, J. Wafer-Scale Ultrathin, Single-Crystal Si and GaAs Photocathodes for Photoelectrochemical Hydrogen Production. *ACS Appl. Mater. Interfaces* **2018,** *10* (39), 33230-33237.

(39) Powell, D. M.; Winkler, M. T.; Choi, H.; Simmons, C. B.; Needleman, D. B.; Buonassisi, T.

Crystalline Silicon Photovoltaics: a Cost Analysis Framework for Determining Technology Pathways to Reach Baseload Electricity Costs. *Energy Environ. Sci.* **2012,** *5* (3), 5874-5883.
(40) Shahrjerdi, D.; Bedell, S. W. Extremely Flexible Nanoscale Ultrathin Body Silicon Integrated Circuits on Plastic. *Nano Lett.* **2013,** *13* (1), 315-320.
(41) Yao, T.; An, X.; Han, H.; Chen, J. Q.; Li, C. Photoelectrocatalytic Materials for Solar Water Splitting. *Adv. Energy Mater.* **2018,** *8* (21), 1800210.
(42) Hoffman, C.; Jarašiūnas, K.; Gerritsen, H.; Nurmikko, A. Measurement of Surface Recombination Velocity in Semiconductors by Diffraction from Picosecond Transient Free-Carrier Gratings. *Appl. Phys. Lett.* **1978,** *33* (6), 536-539.
(43) Lee, Y.; Yang, I.; Tan, H. H.; Jagadish, C.; Karuturi, S. K. Monocrystalline InP Thin Films with Tunable Surface Morphology and Energy Bandgap. *ACS Appl. Mater. Interfaces* **2020,** *12* (32), 36380-36388.
(44) Sadao, A. *Properties of Group-IV, III-V and II-VI Semiconductors*; John Wiley & Sons, Inc.: Hoboken, **2005**.
(45) Sweet, C. A.; Schulte, K. L.; Simon, J. D.; Steiner, M. A.; Jain, N.; Young, D. L.; Ptak, A. J.; Packard, C. E. Controlled Exfoliation of (100) GaAs-Based Devices by Spalling Fracture. *Appl. Phys. Lett.* **2016,** *108* (1), 011906.
(46) Tournet, J.; Lee, Y.; Karuturi, S. K.; Tan, H. H.; Jagadish, C. III–V Semiconductor Materials for Solar Hydrogen Production: Status and Prospects. *ACS Energy Lett.* **2020,** *5* (2), 611-622.
(47) Bedell, S.; Lauro, P.; Ott, J.; Fogel, K.; Sadana, D. Layer Transfer of Bulk Gallium Nitride by Controlled Spalling. *J. Appl. Phys.* **2017,** *122* (2), 025103.
(48) Stocker, D.; Schubert, E.; Grieshaber, W.; Boutros, K.; Redwing, J. Facet Roughness Analysis for InGaN/GaN Lasers with Cleaved Facets. *Appl. Phys. Lett.* **1998,** *73* (14), 1925-1927.
(49) Iida, D.; Kawai, S.; Ema, N.; Tsuchiya, T.; Iwaya, M.; Takeuchi, T.; Kamiyama, S.; Akasaki, I. Laser Lift-Off Technique for Freestanding GaN Substrate using an In Droplet Formed by Thermal Decomposition of GaInN and Its Application to Light-Emitting Diodes. *Appl. Phys. Lett.* **2014,** *105* (7), 072101.
(50) Chung, R. B.-K.; Kim, D.; Lim, S.-K.; Choi, J.-S.; Kim, K.-J.; Lee, B.-H.; Jung, K. S.; Kim-Lee, H.-J.; Lee, W. J.; Park, B. Layer-Transferred GaN Template by Ion Cut for Nitride-Based Light-Emitting Diodes. *Appl. Phys. Express* **2013,** *6* (11), 111005.
(51) Bedell, S. W.; Bayram, C.; Fogel, K.; Lauro, P.; Kiser, J.; Ott, J.; Zhu, Y.; Sadana, D. Vertical

Light-Emitting Diode Fabrication by Controlled Spalling. *Appl. Phys. Express* **2013,** *6* (11), 112301.
(52) Unarunotai, S.; Koepke, J. C.; Tsai, C.-L.; Du, F.; Chialvo, C. E.; Murata, Y.; Haasch, R.; Petrov, I.; Mason, N.; Shim, M. Layer-by-Layer Transfer of Multiple, Large Area Sheets of Graphene Grown in Multilayer Stacks on a Single SiC Wafer. *ACS Nano* **2010,** *4* (10), 5591-5598.
(53) Kim, J.; Park, H.; Hannon, J. B.; Bedell, S. W.; Fogel, K.; Sadana, D. K.; Dimitrakopoulos, C. Layer-Resolved Graphene Transfer via Engineered Strain Layers. *Science* **2013,** *342* (6160), 833-836.
(54) Wang, X.; Tao, L.; Hao, Y.; Liu, Z.; Chou, H.; Kholmanov, I.; Chen, S.; Tan, C.; Jayant, N.; Yu, Q. Direct Delamination of Graphene for High-Performance Plastic Electronics. *Small* **2014,** *10* (4), 694-698.
(55) Lee, J.; Kim, Y.; Shin, H.-J.; Lee, C.; Lee, D.; Lee, S.; Moon, C.-Y.; Lee, S. C.; Kim, S. J.; Ji, J. H. Crack-Release Transfer Method of Wafer-Scale Grown Graphene onto Large-Area Substrates. *ACS Appl. Mater. Interfaces* **2014,** *6* (15), 12588-12593.
(56) Shim, J.; Bae, S.-H.; Kong, W.; Lee, D.; Qiao, K.; Nezich, D.; Park, Y. J.; Zhao, R.; Sundaram, S.; Li, X. Controlled Crack Propagation for Atomic Precision Handling of Wafer-Scale Two-Dimensional Materials. *Science* **2018,** *362* (6415), 665-670.
(57) Gordon, M. J.; Baron, T.; Dhalluin, F.; Gentile, P.; Ferret, P. Size Effects in Mechanical Deformation and Fracture of Cantilevered Silicon Nanowires. *Nano Lett.* **2009,** *9* (2), 525-529.
(58) Östlund, F.; Rzepiejewska-Malyska, K.; Leifer, K.; Hale, L. M.; Tang, Y.; Ballarini, R.; Gerberich, W. W.; Michler, J. Brittle-to-Ductile Transition in Uniaxial Compression of Silicon Pillars at Room Temperature. *Adv. Funct. Mater.* **2009,** *19* (15), 2439-2444.
(59) Plass, K. E.; Filler, M. A.; Spurgeon, J. M.; Kayes, B. M.; Maldonado, S.; Brunschwig, B. S.; Atwater, H. A.; Lewis, N. S. Flexible Polymer-Embedded Si Wire Arrays. *Adv. Mater.* **2009,** *21* (3), 325-328.
(60) Park, H.; Seo, K.; Crozier, K. B. Adding Colors to Polydimethylsiloxane by Embedding Vertical Silicon Nanowires. *Appl. Phys. Lett.* **2012,** *101* (19), 193107.
(61) Kim, H.; Jang, H.; Kim, B.; Kim, M. K.; Wie, D. S.; Lee, H. S.; Kim, D. R.; Lee, C. H. Flexible Elastomer Patch with Vertical Silicon Nanoneedles for Intracellular and Intratissue Nanoinjection of Biomolecules. *Sci. Adv.* **2018,** *4* (11), eaau6972.
(62) Weisse, J. M.; Lee, C. H.; Kim, D. R.; Cai, L.; Rao, P. M.; Zheng, X. Electroassisted Transfer

of Vertical Silicon Wire Arrays using a Sacrificial Porous Silicon Layer. *Nano Lett.* **2013,** *13* (9), 4362-4368.
(63) Weisse, J. M.; Lee, C. H.; Kim, D. R.; Zheng, X. Fabrication of Flexible and Vertical Silicon Nanowire Electronics. *Nano Lett.* **2012,** *12* (6), 3339-3343.
(64) Lee, Y. H.; Cha, H.; Choi, S.; Chang, H. S.; Jang, B.; Oh, J. Characterization of Atomic-Layer-Deposited (ALD) Al2O3-Passivated Sub-50-μm-thick Kerf-Less Si Wafers by Controlled Spalling. *Electron. Mater. Lett.* **2018,** *14* (3), 363-369.
(65) Kim, D. H.; Lee, H. E.; You, B. K.; Cho, S. B.; Mishra, R.; Kang, I. S.; Lee, K. J. Flexible Crossbar-Structured Phase Change Memory Array via Mo-Based Interfacial Physical Lift-Off. *Adv. Funct. Mater.* **2019,** *29* (6), 1806338.
(66) Park, S.; Lee, Y. H.; Wi, J.-S.; Oh, J. A Semitransparent and Flexible Single Crystal Si Thin Film: Silicon on Nothing (SON) Revisited. *ACS Appl. Mater. Interfaces* **2016,** *8* (29), 18962-18968.
(67) Wie, D. S.; Zhang, Y.; Kim, M. K.; Kim, B.; Park, S.; Kim, Y.-J.; Irazoqui, P. P.; Zheng, X.; Xu, B.; Lee, C. H. Wafer-Recyclable, Environment-Friendly Transfer Printing for Large-Scale Thin-Film Nanoelectronics. *Proc. Natl. Acad. Sci.* **2018,** *115* (31), E7236-E7244.
(68) Yu, J.; Wang, L.; Hao, Z.; Luo, Y.; Sun, C.; Wang, J.; Han, Y.; Xiong, B.; Li, H. Van der Waals Epitaxy of III-Nitride Semiconductors Based on 2D Materials for Flexible Applications. *Adv. Mater.* **2020,** *32* (15), 1903407.
(69) Cariou, R.; Chen, W.; Cosme-Bolanos, I.; Maurice, J. L.; Foldyna, M.; Depauw, V.; Patriarche, G.; Gaucher, A.; Cattoni, A.; Massiot, I. Ultrathin PECVD Epitaxial Si Solar Cells on Glass via Low-Temperature Transfer Process. *Prog. Photovolt.* **2016,** *24* (8), 1075-1084.
(70) Hao, R.; Ravi, T.; Siva, V.; Vatus, J.; Kuzma-Filipek, I.; Duerinckx, F.; Recaman-Payo, M.; Aleman, M.; Cornagliotti, E.; Choulat, P. Kerfless Epitaxial Monocrystalline Si Wafers with Built-in Junction and from Reused Substrates for High-Efficiency PERx Cells. *IEEE J. Photovolt.* **2016,** *6* (6), 1451-1455.
(71) Radhakrishnan, H. S.; Martini, R.; Depauw, V.; Van Nieuwenhuysen, K.; Bearda, T.; Gordon, I.; Szlufcik, J.; Poortmans, J. Kerfless Layer-Transfer of Thin Epitaxial Silicon Foils using Novel Multiple Layer Porous Silicon Stacks with Near 100% Detachment Yield and Large Minority Carrier Diffusion Lengths. *Sol. Energy Mater. Sol. Cells* **2015,** *135*, 113-123.
(72) Park, S.; Simon, J.; Schulte, K. L.; Ptak, A. J.; Wi, J.-S.; Young, D. L.; Oh, J. Germanium-on-Nothing for Epitaxial Liftoff of GaAs Solar Cells. *Joule* **2019,** *3* (7), 1782-1793.

(73) Lee, C. H.; Kim, D. R.; Cho, I. S.; William, N.; Wang, Q.; Zheng, X. Peel-and-Stick: Fabricating Thin Film Solar Cell on Universal Substrates. *Sci. Rep.* **2012,** *2* (1), 1-4.

(74) Lee, C. H.; Kim, J.-H.; Zou, C.; Cho, I. S.; Weisse, J. M.; Nemeth, W.; Wang, Q.; Van Duin, A. C.; Kim, T.-S.; Zheng, X. Peel-and-Stick: Mechanism Study for Efficient Fabrication of Flexible/Transparent Thin-Film Electronics. *Sci. Rep.* **2013,** *3* (1), 1-6.

(75) Zhang, Y.; Kim, B.; Gao, Y.; Wie, D. S.; Lee, C. H.; Xu, B. Chemomechanics of Transfer Printing of Thin Films in a Liquid Environment. *Int. J. Solids Struct.* **2019,** *180*, 30-44.

(76) Lee, C. H.; Kim, Y. J.; Hong, Y. J.; Jeon, S. R.; Bae, S.; Hong, B. H.; Yi, G. C. Flexible Inorganic Nanostructure Light-Emitting Diodes Fabricated on Graphene Films. *Adv. Mater.* **2011,** *23* (40), 4614-4619.

(77) Choi, J. M.; Kim, M. S.; Seol, M. L.; Choi, Y. K. Transfer of Functional Memory Devices to Any Substrate. *Phys. Status Solidi* **2013,** *7* (5), 326-331.

(78) Donolato, M.; Tollan, C.; Porro, J. M.; Berger, A.; Vavassori, P. Flexible and Stretchable Polymers with Embedded Magnetic Nanostructures. *Advanced Materials* **2013,** *25* (4), 623-629.

(79) Li, P.; Liu, B.; Ni, Y.; Liew, K. K.; Sze, J.; Chen, S.; Shen, S. Large-Scale Nanophotonic Solar Selective Absorbers for High-Efficiency Solar Thermal Energy Conversion. *Adv. Mater.* **2015,** *27* (31), 4585-4591.

(80) Lim, C.; Shin, Y.; Hong, S.; Lee, S.; Kim, D. H. A Facile Fabrication and Transfer Method of Vertically Aligned Carbon Nanotubes on a Mo/Ni Bilayer for Wearable Energy Devices. *Adv. Mater. Interfaces* **2020,** *7* (8), 1902170.

(81) Chandrashekar, B. N.; Deng, B.; Smitha, A. S.; Chen, Y.; Tan, C.; Zhang, H.; Peng, H.; Liu, Z. Roll-to-Roll Green Transfer of CVD Graphene onto Plastic for a Transparent and Flexible Triboelectric Nanogenerator. *Adv. Mater.* **2015,** *27* (35), 5210-5216.

(82) Magginetti, D. J.; Aguiar, J. A.; Winger, J. R.; Scarpulla, M. A.; Pourshaban, E.; Yoon, H. P. Water-Assisted Liftoff of Polycrystalline CdS/CdTe Thin Films Using Heterogeneous Interfacial Engineering. *Adv. Mater. Interfaces* **2019,** *6* (14), 1900300.

(83) Kim, Y.; Cruz, S. S.; Lee, K.; Alawode, B. O.; Choi, C.; Song, Y.; Johnson, J. M.; Heidelberger, C.; Kong, W.; Choi, S. Remote Epitaxy Through Graphene Enables Two-Dimensional Material-based Layer Transfer. *Nature* **2017,** *544* (7650), 340-343.

(84) Kong, W.; Li, H.; Qiao, K.; Kim, Y.; Lee, K.; Nie, Y.; Lee, D.; Osadchy, T.; Molnar, R. J.; Gaskill, D. K. Polarity Governs Atomic Interaction Through Two-Dimensional Materials. *Nat.*

Mater. **2018,** *17* (11), 999-1004.

(85) Bae, S.-H.; Lu, K.; Han, Y.; Kim, S.; Qiao, K.; Choi, C.; Nie, Y.; Kim, H.; Kum, H. S.; Chen, P. Graphene-Assisted Spontaneous Relaxation Towards Dislocation-Free Heteroepitaxy. *Nat. Nanotechnol.* **2020,** *15* (4), 272-276.

(86) Kum, H. S.; Lee, H.; Kim, S.; Lindemann, S.; Kong, W.; Qiao, K.; Chen, P.; Irwin, J.; Lee, J. H.; Xie, S. Heterogeneous Integration of Single-Crystalline Complex-Oxide Membranes. *Nature* **2020,** *578* (7793), 75-81.

(87) Wang, D.; Lu, Y.; Meng, J.; Zhang, X.; Yin, Z.; Gao, M.; Wang, Y.; Cheng, L.; You, J.; Zhang, J. Remote Heteroepitaxy of Atomic Layered Hafnium Disulfide on Sapphire Through Hexagonal Boron Nitride. *Nanoscale* **2019,** *11* (19), 9310-9318.

(88) Zhai, Y.; Mathew, L.; Rao, R.; Xu, D.; Banerjee, S. K. High-Performance Flexible Thin-Film Transistors Exfoliated from Bulk Wafer. *Nano Lett.* **2012,** *12* (11), 5609-5615.

(89) Sun, Y.; Thompson, S.; Nishida, T. Physics of Strain Effects in Semiconductors and Metal-Oxide-Semiconductor Field-Effect Transistors. *J. Appl. Phys.* **2007,** *101* (10), 104503.

(90) Saha, S.; Hilali, M. M.; Onyegam, E. U.; Sarkar, D.; Jawarani, D.; Rao, R. A.; Mathew, L.; Smith, R. S.; Xu, D.; Das, U. K. Single Heterojunction Solar Cells on Exfoliated Flexible ~25 μm Thick Mono-Crystalline Silicon Substrates. *Appl. Phys. Lett.* **2013**, 102 (16), 163904.

(91) Ahn, J.; Chou, H.; Banerjee, S. K. Graphene-Al2O3-Silicon Heterojunction Solar Cells on Flexible Silicon Substrates. *J. Appl. Phys.* **2017,** *121* (16), 163105.

(92) Branham, M. S.; Hsu, W. C.; Yerci, S.; Loomis, J.; Boriskina, S. V.; Hoard, B. R.; Han, S. E.; Chen, G. 15.7% Efficient 10-μm-Thick Crystalline Silicon Solar Cells using Periodic Nanostructures. *Adv. Mater.* **2015,** *27* (13), 2182-2188.

(93) Jeong, S.; McGehee, M. D.; Cui, Y. All-Back-Contact Ultra-Thin Silicon Nanocone Solar Cells with 13.7% Power Conversion Efficiency. *Nat. Commun.* **2013,** *4* (1), 1-7.

(94) Ward, J. S.; Remo, T.; Horowitz, K.; Woodhouse, M.; Sopori, B.; VanSant, K.; Basore, P. Techno-Economic Analysis of Three Different Substrate Removal and Reuse Strategies for III-V Solar Cells. *Prog. Photovolt.* **2016,** *24* (9), 1284-1292.

(95) Shahrjerdi, D.; Bedell, S.; Ebert, C.; Bayram, C.; Hekmatshoar, B.; Fogel, K.; Lauro, P.; Gaynes, M.; Gokmen, T.; Ott, J. High-Efficiency Thin-Film InGaP/InGaAs/Ge Tandem Solar Cells Enabled by Controlled Spalling Technology. *Appl. Phys. Lett.* **2012,** *100* (5), 053901.

(96) Shahrjerdi, D.; Bedell, S. W.; Bayram, C.; Lubguban, C. C.; Fogel, K.; Lauro, P.; Ott, J. A.;

Hopstaken, M.; Gayness, M.; Sadana, D. Ultralight High-Efficiency Flexible InGaP/(In) GaAs Tandem Solar Cells on Plastic. *Adv. Energy Mater.* **2013,** *3* (5), 566-571.
(97) Zhao, J.; Guo, Y.; Cai, L.; Li, H.; Wang, K. X.; Cho, I. S.; Lee, C. H.; Fan, S.; Zheng, X. High-Performance Ultrathin BiVO4 Photoanode on Textured Polydimethylsiloxane Substrates for Solar Water Splitting. *ACS Energy Lett.* **2016,** *1* (1), 68-75.
(98) Chung, K.; Lee, C.-H.; Yi, G.-C. Transferable GaN Layers Grown on ZnO-Coated Graphene Layers for Optoelectronic Devices. *Science* **2010,** *330* (6004), 655-657.
(99) Kobayashi, Y.; Kumakura, K.; Akasaka, T.; Makimoto, T. Layered Boron Nitride as a Release Layer for Mechanical Transfer of GaN-Based Devices. *Nature* **2012,** *484* (7393), 223-227.
(100) Jeong, J.; Wang, Q.; Cha, J.; Jin, D. K.; Shin, D. H.; Kwon, S.; Kang, B. K.; Jang, J. H.; Yang, W. S.; Choi, Y. S. Remote Heteroepitaxy of GaN Microrod Heterostructures for Deformable Light-Emitting Diodes and Wafer Recycle. *Sci. Adv.* **2020,** *6* (23), eaaz5180.
(101) Park, M.; Bok, B.-G.; Ahn, J.-H.; Kim, M.-S. Recent Advances in Tactile Sensing Technology. *Micromachines* **2018,** *9* (7), 321.
(102) Sakuma, K.; Hu, H.; Liu, X. H.; Ni, J.; Bedell, S. W.; Webb, B.; Wright, S. L.; Lauro, P.; Latzko, K.; Agno, M. CMOS-Compatible Wearable Sensors Fabricated Using Controlled Spalling. *IEEE Sens. J.* **2019,** *19* (18), 7868-7874.
(103) Li, N.; Bedell, S.; Hu, H.; Han, S. J.; Liu, X. H.; Saenger, K.; Sadana, D. Single Crystal Flexible Electronics Enabled by 3D Spalling. *Adv. Mater.* **2017,** *29* (18), 1606638.
(104) Seo, K.; Wober, M.; Steinvurzel, P.; Schonbrun, E.; Dan, Y.; Ellenbogen, T.; Crozier, K. B. Multicolored Vertical Silicon Nanowires. *Nano Lett.* **2011,** *11* (4), 1851-1856.
(105) Park, H.; Crozier, K. B. Multispectral Imaging with Vertical Silicon Nanowires. *Sci. Rep.* **2013,** *3*, 2460.
(106) Song, H. S.; Lee, G. J.; Yoo, D. E.; Kim, Y. J.; Yoo, Y. J.; Lee, D.-W.; Siva, V.; Kang, I.-S.; Song, Y. M. Reflective Color Filter with Precise Control of the Color Coordinate Achieved by Stacking Silicon Nanowire Arrays onto Ultrathin Optical Coatings. *Sci. Rep.* **2019,** *9* (1), 1-10.
(107) Kim, Y. J.; Yoo, Y. J.; Lee, G. J.; Yoo, D. E.; Lee, D. W.; Siva, V.; Song, H.; Kang, I. S.; Song, Y. M. Enlarged Color Gamut Representation Enabled by Transferable Silicon Nanowire Arrays on Metal–Insulator–Metal Films. *ACS Appl. Mater. Interfaces* **2019,** *11* (12), 11849-11856.
(108) Lee, G. J.; Kim, Y. J.; Song, H. S.; Yoo, D. E.; Lee, D.-W.; Kang, I.-S.; Song, Y. M. The Facile Implementation of Soft/Tunable Multiband Optical Filters by Stacking Vertical Silicon

Nanowire Arrays for Smart Sensing. *Adv. Intell. Syst.* **2019,** *1* (6), 1900072.

(109) Mumm, F.; Beckwith, K. M.; Bonde, S.; Martinez, K. L.; Sikorski, P. A Transparent Nanowire-Based Cell Impalement Device Suitable for Detailed Cell–Nanowire Interaction Studies. *Small* **2013,** *9* (2), 263-272.

(110) Kim, H.; Lee, H. S.; Jeon, Y.; Park, W.; Zhang, Y.; Kim, B.; Jang, H.; Xu, B.; Yeo, Y.; Kim, D. R. Bioresorbable, Miniaturized Porous Silicon Needles on Flexible Water-Soluble Backing for Unobtrusive, Sustained Delivery of Chemotherapy. *ACS Nano* **2020,** *14* (6), 7227-7236.

Abstract Graphic