FABRICATION OF SOLAR CELLS USING THE EPILIFT TECHNIQUE

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ABSTRACT

The Epilift technique allows the growth and detachment of good quality, single crystal silicon films on silicon substrates. Since the substrates only act as a growth template, they can be re-used, offering the potential for substantial cost reductions. However, the processing of solar cells on Epilift layers introduces significant challenges as a result of the fact that the layers are thin and perforated. We have obtained good results by performing most of the processing prior to detachment of the layer from the substrate. An interdigitated rear contact design created by laser patterning allows the specific features of epilift layers to be optimally exploited. Individual $1cm^2$ cells with a SiO_2 antireflection coating have displayed efficiencies in excess of 13%, while a $50cm^2$ mini-module has displayed an efficiency of 10.9%.

1. INTRODUCTION

Decreasing material cost is the primary driver for reducing the costs of silicon photovoltaics. The cost of silicon comprises 30-50% of the costs of conventional wafer based modules. Despite this cost barrier silicon's excellent efficiency, stability, material abundance and low toxicity have enabled its domination of the PV market even though a variety of thin-film technologies have been developed. However, the cost of the silicon remains a barrier to major breakthroughs in the cost of silicon photovoltaics.

Thin silicon photovoltaics is an attractive option to reduce silicon costs. The epilift technique used to grow the thin silicon layers in this paper is one of a range of lift-off techniques that has been developed in the last decade [1-3]. In these techniques, a high quality, single crystal silicon film is grown on a suitably prepared silicon substrate. The epitaxial silicon film is subsequently detached from the substrate and the substrate is re-used. Since the substrate can be re-used many times and the amount of silicon used for the growth of the epilayer is much less than is consumed in a typical silicon wafer, significant reductions in silicon cost can be achieved. A more detailed account of the epilift growth technique is described elsewhere at this conference [4].

This paper describes the processing of cells on the epilift substrates and key performance results.

2. EPITAXIAL GROWTH

Epitaxial layers for solar cells were grown on 100mm diameter, 0.015 ohm-cm, B doped Cz (111) wafers. A 100nm thick layer of SiO_2 was grown on the substrates and patterned using photolithography. The pattern created is shown in figure 1. It consists of two orthogonal sets of seeding lines, spaced 160 µm apart. At regular intervals of several millimetres, larger 'islands' of substrate are also exposed. Indium was used as the solvent for epitaxial growth, resulting in p type epitaxial layers typically 50µm thick. An epitaxial layer is shown in figure 2. Following growth, the oxide is removed and the wafers are immersed in a dopant selective silicon etchant, such as 1:3:8 hydrofluoric:nitric:acetic acid. This solution etches through the narrow attachment regions. The epilayer remains attached to the substrate at the silicon 'islands'.

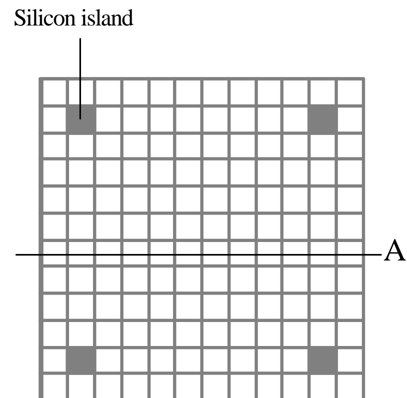

Figure 1. .The line seed pattern used for epitaxial growth. White areas are covered with SiO_2, in the grey areas the substrate is exposed. An array of silicon 'islands' is used to keep the epilayer attached to the substrate during processing.

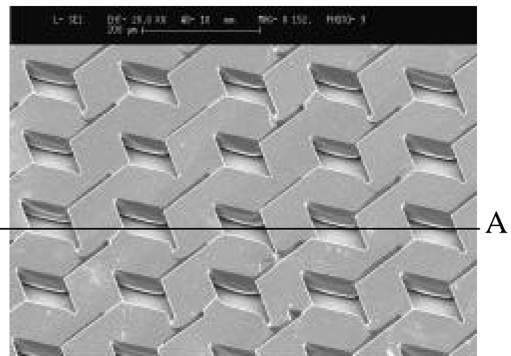

Figure 2. Epitaxial layer grown by LPE on a 111 oriented substrate. The layer grows out over the masking oxide layer, increasing the fractional coverage of silicon.

3. CELL DESIGN AND PROCESSING

Cell processing is carried out with the epilayer still attached to the substrate, to provide mechanical strength.

The epitaxial layer is rough compared even to a textured wafer. The epitaxial layer has holes that allow access to both sides of the layer. Steps in the layer can also be seen in figure 2. These are caused by the slight

misorientation of the substrate relative to <111>. This helps to allow uniform nucleation of growth but introduces challenges for cell processing.

3.1 Patterning

Original attempts to process the epitaxial layer were made using photolithography. Thick layers of relatively viscous resist were used to provide coverage of the rough surface. Significant problems were encountered, however, with the side of the layer adjacent to the substrate. Resist coverage was poor and masking layers which should have been retained were removed by wet chemical etching leading to shunting of most cells.

Some relief was provided with a change to dry chemical etching. Reactive ion etching (RIE) was used to etch masking oxides through the photoresist mask. Since RIE is directional, the rear surface of the epitaxial layer was not etched and remained defect free. This immediately improved the cell processing results and cells were manufactured with only moderate shunts. However, coverage of the steps and hole edges was unreliable and still lead to some unwanted defects and shunting.

Laser patterning was then tried as an alternative to photolithography. This was first developed for buried contact solar cells at UNSW [5] and is used for patterning commercial conventional wafer cells. This patterning technique has a number of advantages for epilift layer processing including:

1. Tolerance of surface roughness
2. Directionality (patterned only top surface)
3. Increased process flexibility

Patterning was undertaken on an IR Q-switched laser micromachining station with frequency doubling. Wafers were moved under a pulsed beam on a programmable X-Y stage.

Laser patterning required ablation of the silicon and the overlying masking layer. It was essential that the depth of the laser cut was less than the epitaxial layer thickness to avoid punching through the epitaxial layer . It was also desirable to minimise the cut width to keep the contact area small.

The fundamental frequency (1052nm) infrared cutting was originally examined. This light is relatively weakly absorbed in silicon and is therefore absorbed below the surface. This lead to wide deep cuts (>25μm). Decreased power lead to melting of the silicon without ablation. Alkaline etches were used to remove the molten silicon but much of the masking layer remained intact, interfering with subsequent processing.

The frequency doubled green (526nm) laser light provided superior results. The green spot size was smaller and light was absorbed closer to the surface reducing the power required for ablation. Cuts could be made which were less than 20 microns wide and 10 microns deep after clean up etch. The cut was sufficiently deep to allow continuous lines across the epitaxial steps.

3.2 Cell design

Only one side of the epitaxial layer is accessible before the layer is detached. Therefore both contacts to the cell must be on the top surface. This naturally leads to an interdigitated cell design with n-type and p-type contacts interleaved. Both laser patterned contacts need to be diffused since the silicon is ablated from the hole and the substrate is insufficiently doped for ohmic contact.

The contact grid has to be cut aligned to the grid opening for the epitaxial growth or contacts are broken by the holes in the layer. The two contacts were placed on different lines of the epitaxial layer mesh. This requires that the spacing of the grid lines is equal to a multiple of the pitch of the epitaxial layer (typically 160 microns).

The remainder of the surface was diffused n-type to act as a double sided collecting junction. This is oxide diffused to provide excellent surface passivation. The top and bottom of the epitaxial layer are joined through the holes. This leads naturally to a structure similar to the emitter wrap through cell [6]. Figure 3 is a schematic of the cell design through cross section 'A' in figures 1 and 2.

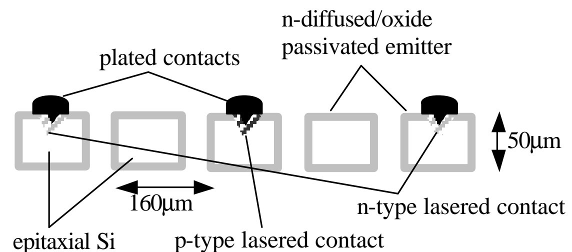

Figure 3. Schematic of the cell design. The lightly diffused emitter wraps to both sides of the cell and is passivated with oxide. The lasered contacts are aligned to the mesh and are heavily diffused and plated.

An outline of the cell process is as follows. Initially, the epilayer is cut into individual 1x1cm^2 areas, which will form individual cells. This process can be carried out with a laser or a dicing saw. A light phosphorous diffusion is performed in a diffusion furnace with a $POCl_3$ bubbler to form the emitter. This covers all surfaces of the epilayer since the gas can penetrate to the rear via the holes in the silicon mesh. A thick layer of SiO_2 is then grown. This acts as a masking layer for the diffusions and is retained as the final passivating oxide.

The Q-switched laser operating in the green (523nm) is then used to create shallow grooves for the n contact, followed by a damage etch. The grooves are aligned to the silicon mesh. The grooves are diffused with phosphorus and a thin oxide is grown on top to mask against the boron diffusion. The same laser processing is used to create shallow grooves for the p contact, aligned to lines in the mesh between the n-type contacts (see figure 4 schematic). The second set of grooves is diffused with boron.

The thin oxide grown on the n-type grooves and the boron glass is removed. Both sets of grooves are then metallised. The cells form an interdigitated grid.

Cells can be detached from the module mechanically or by laser cutting. Mechanical separation involves attaching the cells to a temporary superstrate and pulling the cells from the substrate. The epitaxial layer breaks around the attachment island. This causes only localised damage to the cell. Alternatively, a laser can be used to dice around the edge of the attachment island. This leads to controlled damage to the cell in the form of a well defined hole. There is no significant decrease in cell performance due to damage from the detachment.

3.4 Cell Performance

The laser processing enabled 1cm^2 cell efficiencies as high as 13% (in-house). Individual cells displayed voltages as high as 620mV and fill factors up to 70%. A major limitation on the device performance was the light doping of the thin substrate. This was most clear in the fill factors of the cells that were limited by series resistance losses due to the lateral flow of holes in the epitaxial substrate. Cells typically had contact line spacings of 640μm (i.e. every second mesh line has an n-type or p-type contact line). Increased spacings led to decreases in fill factor. 960 micron spacing decreased fill factors to less than 60%. Resistivity of the epitaxial material could be improved in future with the addition of Ga to the melt to increase doping. This is expected to improve both fill factor and voltage provided the Ga does not degrade the bulk lifetime.

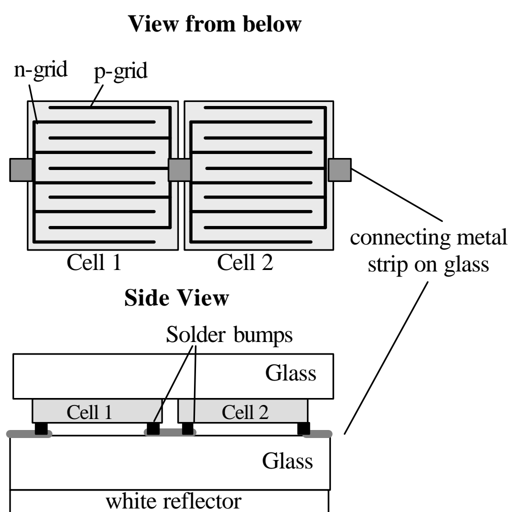

Figure 4. Series connection of cells using solder bumps on glass. Cell contacts are on the rear of the cell, minimising shading**.**

Internal collection efficiencies from the cell should be near ideal. Cells are thin with collecting junctions on both surfaces. The quality of detached layers was good with lifetimes over several microseconds up to 10μs, so diffusion lengths exceed the device thickness. Despite the near <111> front surface, reflection and transmission measurements indicated enhanced absorption due to light trapping equivalent to a path length enhancement by a factor of four. Cells are exposed to illumination from the rear, eliminating shading from the contacts.

Cell performance of isolated cells is limited by the holes in the epitaxial silicon mesh. Approximately 20% of the mesh area is not covered with silicon. Light directed onto these areas is not absorbed in the silicon. Cell performance can be recovered by reflecting this light back onto the cell. A specular mirror is not sufficient for this task since light perpendicular to the mesh is simply reflected back via the same path. However, a diffuse reflector enables the majority (>80%) of the light that passes through the holes to be absorbed by the silicon since the cells are bifacial (though less efficient on the contact side). Cell currents with a rear reflector were as high as 31mA. A textured specular reflector may be able to produce even better results but would require alignment for best performance. Significant further improvements to current could be achieved through the use of a better AR coating.

4. CELL MOUNTING

Since both cell contacts are on the same side, monolithic connection can be realised. Cells were connected into a mini-module using the 'flip-chip' approach. The desired cell interconnection pattern was fabricated on glass by thermal evaporation of silver. The tracks were laid out to form the necessary series and parallel connections. Pads were patterned to correspond to the location of the contact pads on the cell. The pads were then screen printed with solder paste.

Cells were placed in a jig to position them accurately. The glass was then brought in contact with the cells and the assembly was heated to re-flow the solder (figure 4). Figure 5 is an example of an array of 45 1cm^2 cells that were connected together to form 9 parallel strings of 5 series connected cells each, to make a 50cm2 mini-module (10% of the area is gaps between cells). These cells came from one epitaxial layer on a 100mm substrate. The glass is then turned over so that the contact grids are on the rear (not illuminated) side. This helps minimise shading losses.

As described in section 3.4, a significant fraction of the cell surface is transparent due to the presence of holes. In addition, there are gaps between the cells. In order to recover most of this light, a white reflective paint is placed on the rear of the glass.

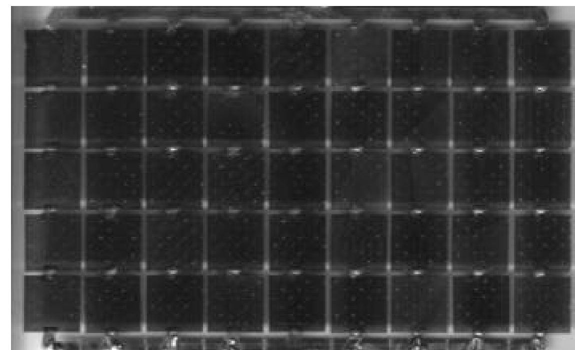

Figure 5. Series connection of cells using solder bumps on glass. Cell contacts are on the rear of the cell, minimising shading. The bright spots on the cells are damage from the mechanical detachment where the layer was attached to the substrate.

The 50cm^2 mini-module had an efficiency (in-house) of 10.9% with V_{oc} = 2.91V, I_{sc} = 298mA and FF = 63%. (Figure 6). Cell currents (33.0mA) were greater than for individual cells due to the recovery of the light striking between cells. The fill factor is low primarily because of the series resistance of the cells, not mismatch or module resistance losses.

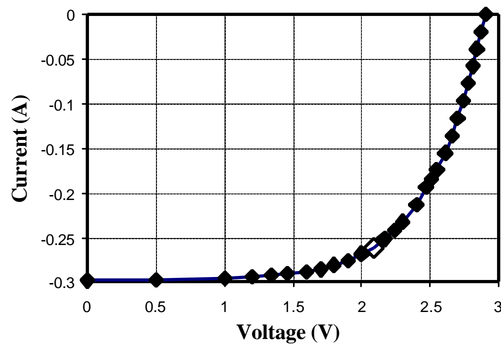

Figure 6. IV curve for a 50cm^2 9x5 mini-module of epilift cells. The module efficiency was 10.9% (in-house).

5. CONCLUSIONS

The Epilift technique has been used to grow monocrystalline silicon layers which have been processed into cells and detached from the substrate template. The surface morphology of the layers led to the use of laser patterning to define the cell contacts. Cells were designed with a structure similar to the emitter wrap through cell design which, combined with the layer quality, enabled good carrier collection efficiencies

Good cell efficiencies up to 13% and voltages of 620mV have been demonstrated on individual cells and a 50cm^2 minimodule displayed an efficiency of 10.9%. Cells were primarily limited by poor fill factors. Further efficiency improvements could be expected through the use of gallium to produce more heavily doped epitaxial layers.

Acknowledgments

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