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I–V curve hysteresis induced by gate-free charging of GaAs nanowires' surface oxide

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The control of nanowire-based device performance requires knowledge about the transport of charge carriers and its limiting factors. We present the experimental and modeled results of a study of electrical properties of GaAs nanowires (NWs), considering their native oxide cover. Measurements of individual vertical NWs were performed by conductive atomic force microscopy (C-AFM). Experimental C-AFM observations with numerical simulations revealed the complex resistive behavior of NWs. A hysteresis of current-voltage characteristics of the p-doped NWs as-grown on substrates with different types of doping was registered. The emergence of hysteresis was explained by the trapping of majority carriers in the surface oxide layer near the reverse-biased barriers under the source-drain current. It was found that the accumulation of charge increases the current for highly doped p^+-NWs on n^+-substrates, while for moderately doped p-NWs on p^+-substrates, charge accumulation decreases the current due to blocking of the conductive channel of NWs. *Published by AIP Publishing*. https://doi.org/10.1063/1.5005125

GaAs nanowire (NW)-based electronic devices have been undergoing rapid development in the last decade. Efficient photodiodes and laser structures have been created, and significant progress has been achieved in increasing the efficiency of solar cells based on GaAs NWs.[1–3]

Considering the large surface-to-volume ratio in NWs, surface effects can dominate the electrical properties of NW-based devices. A substantial disadvantage of GaAs is the high density of the surface states, which gives rise to a depletion layer near the surface.[4] In addition, a native oxide on the GaAs surface, consisting of GaO_x, AsO_x, and As,[5] contains charge-capturing traps. The charging-discharging of these traps is relatively slow, with characteristic durations of seconds.[6] The width of the surface depletion region can either decrease or increase depending on the sign of a trapped charge.[7]

Slow charging of the NW's surface oxide affects the current flowing through the NW in the time scale up to hundreds of seconds. Yang *et al.* have reported that negative photoconductance in InAs NWs can be induced by charge trapping in the surface oxide.[8] In Ref. 9, these effects were studied in horizontal Ge NWs with a native oxide surface, contacted at both ends (drain and source). The charging of the surface was performed by applying a bias voltage to the substrate (gate). It should be noted that charging of the surface of a NW can also occur when the voltage is applied solely between the drain and the source. The effect of charge accumulation on the surface of horizontal GaAs NWs was observed recently by Kelvin probe force microscopy (KPFM) in the area near the Schottky junction by applying a reverse voltage.[10] The accumulation of majority carriers occurred at the border of the depletion region of a reverse-biased barrier and the characteristic durations of charge accumulation/distribution were tens of seconds. The impact of these effects on current-voltage characteristics (I–V curves) has not been studied yet. It is known that surface charges can lead to a considerable change in the Schottky barrier height.[11] This effect is reinforced in NWs due to their high surface-to-volume ratio.[12] In this respect, it seems remarkable that we have observed a pronounced hysteresis in measurements of I–V curves on individual vertical NWs. Moreover, we have observed and provide explanation for both the increase and decrease in current due to the accumulation of charges in the surface oxide, which is directly dependent on the doping level of individual NWs.

The aim of this study was to investigate charge accumulation on the surface of as-grown NWs and its specific influence on the hysteresis of their I–V curves. The measurements were performed with an atomic force microscope (AFM). It is worth noting that the measurements were done accurately on single NWs [see the scheme in Fig. 1(a)] instead of typical measurements carried out on NW ensembles or horizontally fixed NWs, where the supporting substrate may perturb the charge carriers inside the NWs.[13]

Two types of Zn-doped NWs were used in the experiments: (1) p^+-GaAs NWs (with carrier concentration, $N_a \sim 5 \times 10^{18}\,cm^{-3}$) on an n^+-GaAs substrate ($N_d \sim 5 \times 10^{18}\,cm^{-3}$) and (2) p-GaAs NWs ($N_a \sim 1 \times 10^{18}\,cm^{-3}$) on a p^+-GaAs substrate ($N_a \sim 5 \times 10^{18}\,cm^{-3}$). GaAs NWs were grown on a GaAs (111)B substrate with a metalorganic vapor phase epitaxy (MOVPE) system using nominally 100 nm Au nanoparticles as the seeds in the vapor-liquid-solid method. The length of the NWs was controlled to be $\sim$1.1 μm, and the diameter was in the range of 100–150 nm. More details on the growth technique are presented in Ref. 14. Figure 1(b)

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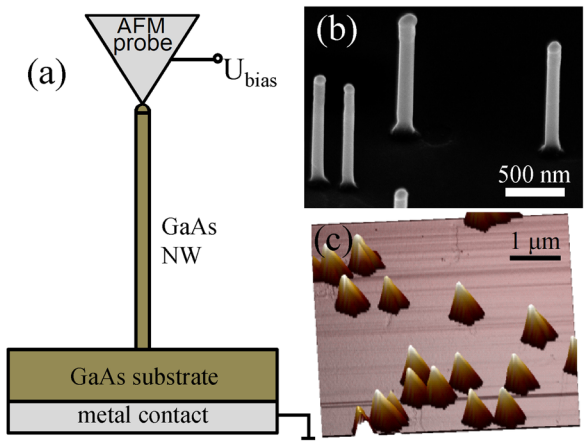


FIG. 1. (a) Sketch of the AFM experimental configuration. (b) Representative SEM image of vertical p^+-GaAs NWs on an n^+-GaAs substrate. (c) AFM 3D topography image of vertical NWs.

depicts a scanning electron microscopy (SEM) image of the vertical NWs, and Fig. 1(c) shows a 3D topography AFM image of an array of NWs. The pyramidal shape of the NWs in the AFM images results from the convolution effect of the pyramidal shape of the AFM probe tips onto tall cylindrical NWs.

The measurements of the current-voltage characteristics of individual GaAs NWs as-grown on a GaAs substrate were performed by accurate positioning of the AFM probe onto their upper ends [Fig. 1(a)]. The accurate positioning ensured a stable and reliable electrical contact without deformation of the NWs.[15,16] This is why the I–V curves were taken in the Ramp contact regime at predefined locations to establish a persistent electrical contact. In order to achieve such a delicate stable contact, we used the PeakForce Tapping™ mode that allowed controlling the maximum force of the impact made on the upper part of the NW by the AFM probe, i.e., the force of pressing onto the Au catalyst cap.

One electrical contact was established via an AFM tip connected to the Au cap of the NW, while the second contact was as-grown at the bottom of the wide substrate (fixed on a steel wafer with silver conductive paste). The NW-substrate bottom electrical contact was assumed to be low-resistant and have a negligible impact on the obtained I–V curves. Since the surface area of the bottom contact was large and the substrate was thick and highly doped, the entire bottom contact was considered to be Ohmic.[17] The I–V curves were measured on the NWs with a Multimode 8 AFM (BRUKER Inc.) in ambient conditions. We used PFTuna (BRUKER Inc.) probes with Pt/Ir-coated conductive tips and a nominal tip radius of 25 nm.

Numerical calculations of potential distribution and charge transport processes in NWs were performed by using the device simulation tool ATLAS by Silvaco.[18] The proposed model was calculated in 2D with cylindrical symmetry. The model replicates cylindrical GaAs with a diameter of 100 nm. The actual parameters of the NWs were utilized for lengths, shapes, position of contacts, and doping levels in the following simulations. More details are presented in the supplementary material (Fig. S1, supplementary material). The Schottky barrier height for all types of metallic contacts was 0.55 eV.[19] The NWs were positioned on the GaAs-substrate with a modeled thickness of 200 nm, indicating the bottom Ohmic electric contact. The upper contact was of the Schottky type. Thermionic emission, recombination, and tunneling across the Schottky barrier at the metal-nanowire interface were included as possible transport mechanisms in our simulations.[20] The thermionic emission current was calculated by taking into account surface recombination velocity, field-dependent barrier lowering, static dipole effects, and band-to-band recombination.[21] Tunneling for electrons and holes was calculated by a built-in universal Schottky tunneling model.[22] In addition, donor and acceptor midgap surface states with a density of $D_{it} = 3 \times 10^{12}\,cm^{-2}$ (Ref. 23) and a cross section of $\sigma = 10^{-14}$ cm^2 were included in the model. The charge accumulation effect on the I–V curves was modeled by adding fixed surface charges (Q_f) into the surface of the NW.

Let us consider the reasons for charge accumulation in the surface native oxide at the border of a depletion region of a reverse-biased barrier. The distribution of electrical potential within the oxide of p^+-GaAs NWs under a reverse-bias in the range of 3–10 V was modeled near the Schottky barrier. From the profiles in Fig. 2(a), it becomes evident that most of the voltage drops in close proximity to the Schottky barrier. Therefore, the electric potential in the oxide is distributed nonlinearly between two electrodes. However, the studied system should seek to minimize its energy represented by the linear distribution of the potential in the oxide [seen as dotted lines in Fig. 2(a)]. In Ref. 24, external voltage was applied between electrodes mounted on a SiO_2 layer.

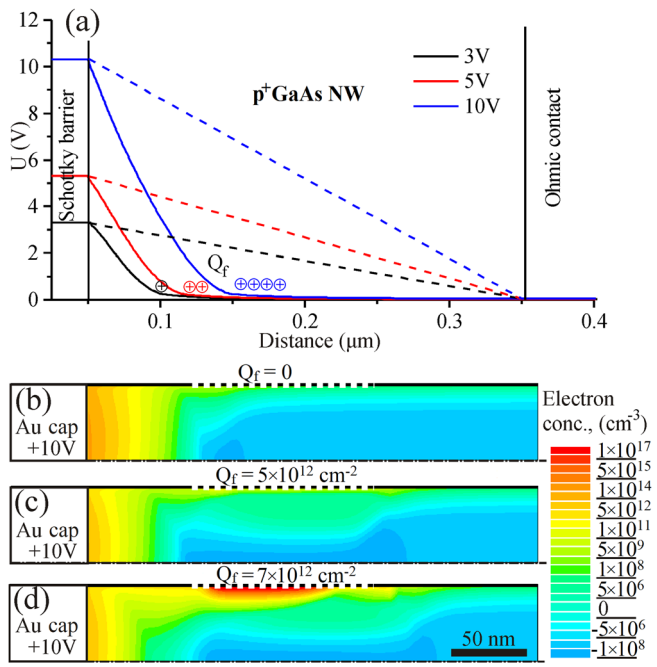


FIG. 2. (a) Distribution of electric potential in the surface oxide of a GaAs NW under a reverse bias in the range of 3–10 V applied to the Schottky barrier at the border between the Au cap and the NW. Q_f indicates the location of the charge accumulated in the surface oxide. The dashed lines indicate the linear potential distribution. (b)–(d) Semi-cross-sectional maps of the distribution of electron density under different Q_f values in surface oxide layers near the surface charge region of the Schottky barrier under +10 V applied to the Au cap.

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The authors noticed that potential distribution was transformed from non-linear to linear by charge redistribution in the SiO_2 layer with time. We have previously observed exactly such behavior of potential on an individual horizontal NW by KPFM.[10] Figs. S2 and S3 in the supplementary material can be accessed for further details. In order to reach the linearity of distribution of potential in the oxide layer, exactly positive charge carriers should be accumulated in the p-doped NW. Likewise, the surface oxide of an n-doped NW would accumulate negative charge, i.e., corresponding majority carriers. Moreover, an enlarged reverse bias would result in a higher amount of trapped charges.

Several physical phenomena are expected to occur due to the accumulation of charge carriers on the surface of the NW near the Schottky junction: (1) change in the width of the conduction channel of the NW and tunneling probability due to a field effect; (2) change in the height of the Schottky barrier due to an image force; and (3) change in the recombination current.[25] In particular, the accumulation of a positive charge on the walls of the p^+-NW should reduce the current according to the phenomenon (1) mentioned above.[26] According to the abovementioned effects (2) and (3), the accumulation of a positive charge should intensify the current.

Figures 2(b)–2(d) present modeled semi-cross sections of p^+-GaAs NWs near the Schottky barrier under a reverse bias of 10 V. Each semi-cross section shows the distribution of the concentration of electrons under the specific density of the surface charge Q_f near the surface charge region of the Schottky barrier. It is visible that the diameter of the conduction channel shrinks under the amplified surface charge [from $Q_f = 0$ in Fig. 2(b) to $Q_f = 5 \times 10^{12}\,cm^{-2}$ in Fig. 2(c)] due to the field effect. A further increase in the surface charge to $Q_f = 7 \times 10^{12}\,cm^{-2}$ [Fig. 2(d)] leads to the emergence of an inversed region near the surface of the NW. However, the conduction channel in the NW is still open in such conditions. The emergence of a highly doped n^+-inversion region leads to the increase in a recombination current. Thus, the conductance of the NW in the case shown in Fig. 2(d) is higher than in the case in Fig. 2(c). This means that a NW must be highly doped and with a non-depleted core for the generation of a considerable recombination current. In low-doped NWs, the surface charge also can lead to the emergence of an n^+-region, but the depletion of a NW would lead to an insignificant concentration of holes and a negligible recombination current.

It can thus be deduced that the accumulation of majority carriers on the surface of a NW near the energy barriers will lead to a decrease in the conductance of low-doped NWs. On the other hand, the increase in conductivity in highly doped NWs is possible due to the reinforcement of the recombination current.

Comparison between the modeled results (Fig. 2) and experimental findings (Fig. 3) strengthens the proposed hypothesis. Figure 3 shows the I–V curves of vertical p^+-GaAs NWs grown on the n^+-GaAs substrate registered in the contact between the NW and the conductive AFM probe. These I–V curves were recorded with varying voltages from 0 V to +7 V and back and later from 0 V to −7 V and back. The sweeping rates were 4 V/s [Fig. 3(a)] and 1 V/s [Fig. 3(b)]. Comparison of these I–V curves reveals a clear hysteresis associated with

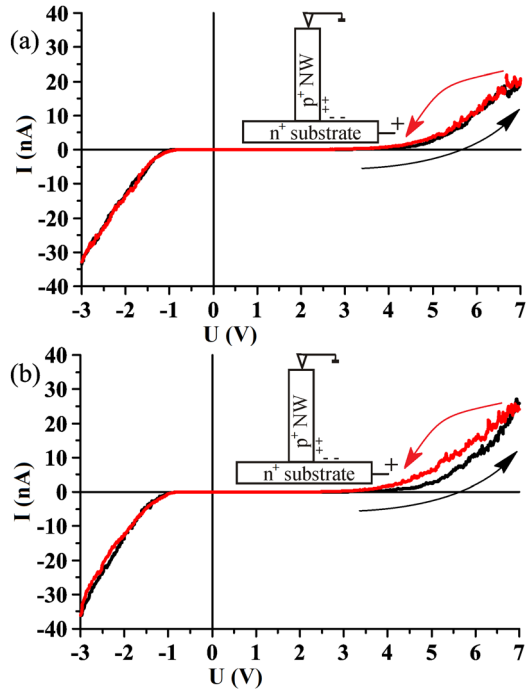


FIG. 3. I–V curves of vertical p^+-GaAs NWs grown on an n^+-GaAs substrate. The black and red curves denote measurements corresponding to an increase or a decrease in the voltage. The bias sweeping rates were (a) 4 V/s and (b) 1 V/s. The inset shows the experimental arrangement.

the accumulation and dissipation of electric charge near the Schottky barrier area and characteristic durations of these processes in the order of seconds. At least five far-standing NWs were studied in each sample, and hystereses were observed in all of them.

Figure 4 shows the I–V curves of vertical p-GaAs NWs grown on a p^+-GaAs substrate registered when contacting the NW by a conductive AFM probe. These I–V curves were recorded with varying voltages from 0 V to +10 V and back and later from 0 V to −10 V and back, with a sweeping rate of 4 V/s under laser illumination. Comparison of these I–V curves reveals a hysteresis inverted with respect to the hysteresis shown in Fig. 3.

A pronounced hysteresis can be noticed for the NWs on both substrates (Figs. 3 and 4). The current increases with the reduction of voltage in Fig. 3, while the current drops down in Fig. 4 in the same regime. It is important to note that the characteristic lifetimes of charges establishing

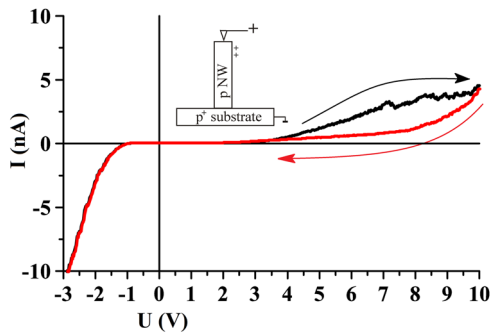


FIG. 4. I–V curves of vertical p-GaAs NWs grown on a p^+-GaAs substrate. The black and red curves denote measurements corresponding to an increase or a decrease in the voltage. The bias sweeping rate was 4 V/s. The inset shows the experimental arrangement.

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hysteresis are in the order of seconds. Therefore, we suppose that the existence of hysteresis is associated with the accumulation of charge exactly in the surface oxide of GaAs NWs.[6] This conclusion is reinforced by the fact that increasing the duration of the recording of I–V curves leads to intensified hystereses. Moreover, it is confirmed by the absence of hysteresis observed by us during the recording of I–V curves on passivated NWs because the surface oxide in them is replaced by passivating shell layers.[14]

It is vital to consider that the charge accumulation occurs in regions with the highest voltage drop. For example, in the reverse-bias case, it is the Schottky barrier or the p-n junction area. Concerning the I–V curves measured on the vertical p^+-GaAs NW grown on the n^+-GaAs substrate (Fig. 3), their shape was determined by the reverse current through the p-n junction when a positive voltage is applied. For a negative voltage, the shape was determined by the reverse current through the Schottky barrier. The hysteresis was almost absent for negative voltages below –1.5 V due to the breakdown of the Schottky barrier and resulting downfall of the resistance. Therefore, the voltage drop at the barrier diminished, and charge accumulation did not occur on the surface of the NWs. For a positive voltage, the major part of the voltage drop occurred in the p-n junction, wherein the charge accumulation occurred on the NW walls and on the surface of the substrate near the contact. However, since the surface accumulates majority carriers, the surface of the p^+-NW accumulates holes, while the surface of the n^+-substrate accumulates electrons.

Figure 5(a) depicts the semi-cross section of a cylindrically symmetric model of the NW with a length of 1 μm and a radius of 50 nm (the horizontal and vertical scales are different). This figure presents the distribution of current density in a p^+-NW on the n^+-substrate at the application of the +7 V bias to the substrate. It is evident that the current density along the surface descents. This is due to surface band bending, which has been taken into account in our model by using a specific surface. Additionally, specific locations where the fixed charge Q_f was installed are marked in Fig. 5(a): Q_{f1} for the case of the p^+-NW on the n^+-substrate and Q_{f2} for the case of p-NW on the p^+-substrate.

The I–V curve of the p^+-NW on the n^+-substrate was simulated to validate our model for the case depicted in Fig. 3(a) with minimal hysteresis and accordingly with the negligible amount of accumulated charge. The simulated and experimental current-voltage characteristics are compared in Fig. 5(b). The coincidence of simulated and experimental I–V curves indicates the correctness of our model and the chosen parameters D_{it}, σ, and Q_f. Figure 5(c) shows the simulated current-voltage characteristics with different densities of a fixed charge in the areas depicted in Fig. 5(a) as Q_{f1}. The charge density was equal in the areas where positive and negative charges were installed. The location where the charge was set was somewhat distant from the location of the

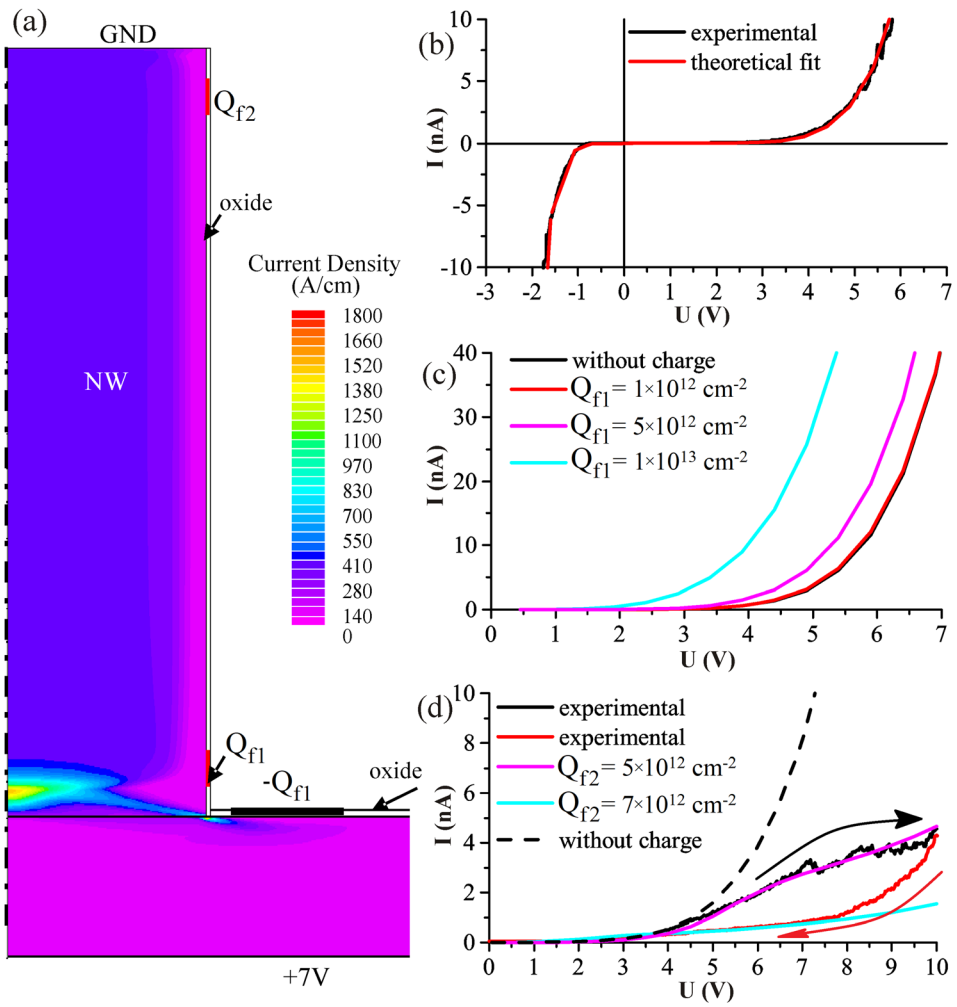


FIG. 5. (a) Semi-cross section of vertical p^+-NWs on the n^+-GaAs substrate with simulated distribution of the current density under the bias voltage of +7 V. Q_{f1} and Q_{f2} are the positions of fixed charge densities. (b) Experimental and simulated I–V curves of p^+-NWs on the n^+-GaAs substrate. (c) Simulated I–V curves of p^+-NWs on the n^+-GaAs substrate with a different fixed charge density Q_{f1}. (d) Experimental and simulated I–V curves of the p-NW on the p^+-GaAs substrate with a different fixed charge density Q_{f2}.

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barrier. This distance (to which these locations are remote from the boundary) was determined by the width of barrier field penetration. From Fig. 5(c), it follows that an increase in the fixed charge density on the surface from $10^{12}\,cm^{-2}$ to $10^{13}\,cm^{-2}$ results in intensification of the reverse current through the p-n junction. This corresponds well to our experimental results [Fig. 3(b)]. The increase in the reverse current through the p-n junction seems associated with the increase in the recombination current.

In the case of p-NWs on the p^+-substrate (Fig. 4), the breakdown of the Schottky barrier of the NW occurs at 3–4 V and hysteresis becomes visible. The segment of the I–V curves corresponding to the breakdown of the p-NW Schottky barrier was found in regions with opposite signs of voltage (Figs. 3 and 4).

A positive fixed charge Q_{f2} was installed near the Schottky barrier between the NW and the Au cap [see Fig. 5(a)] for the numerical simulation of the I–V curves shown in Fig. 4. Figure 5(d) shows experimentally obtained current-voltage characteristics and those simulated for the different Q_{f2} surface charge density. This figure illustrates that increasing the positive surface charge density leads to a decrease in the reverse current through the Schottky barrier. This decrease was associated with the blocking of the conduction channel in the NW. It is worth noting that the simulated I–V curves agree only qualitatively with the experiment. This is because a fixed amount of charge was set to a fixed position in our simulations. However, an increase in voltage at the beginning of the I–V curve recording should move the position of the accumulated charge [see Fig. 2(a)].

To summarize, hystereses of I–V curves of vertical GaAs NWs emerge during their recording by conductive AFM. Characteristic durations of the recorded hystereses are in the order of seconds. This phenomenon is explained by the trapping of majority carriers in the native oxide on the surface of NWs. A positive charge is accumulated inside the surface layer of the oxidized p-GaAs NWs in close proximity to the Schottky barrier and p-n junction under reverse bias. In highly doped NWs, charge accumulation leads to an increase in current due to the intensification of recombination. In moderately doped NWs, the accumulated charge blocks the conductive channel and the current is decreased. This effect has a significant impact on the conductivity of NWs, which should be considered when designing device structures based on semiconductor NWs.

See supplementary material for details of our numerical model and KPFM results for horizontal NWs.

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[1]X. Dai, S. Zhang, Z. L. Wang, G. Adamo, H. Liu, Y. Z. Huang, C. Couteau, and C. Soci, Nano Lett. **14**, 2688 (2014).
[2]B. Hua, J. Motohisa, Y. Kobayashi, S. Hara, and T. Fukui, Nano Lett. **9**, 112 (2009).
[3]D. van Dam, N. J. J. van Hoof, Y. Cui, P. J. van Veldhoven, E. P. A. M. Bakkers, J. Gómez Rivas, and J. E. M. Haverkort, ACS Nano **10**, 11414 (2016).
[4]A. C. E. Chia and R. R. LaPierre, J. Appl. Phys. **112**, 063705 (2012).
[5]P. A. Alekseev, M. S. Dunaevskiy, D. A. Kirilenko, A. N. Smirnov, V. Y. Davydov, and V. L. Berkovits, J. Appl. Phys. **121**, 074302 (2017).
[6]M. Passlack, M. Hong, and J. P. Mannaerts, Appl. Phys. Lett. **68**, 1099 (1996).
[7]V. Schmidt, S. Senz, and U. Gosele, Appl. Phys. A **86**, 187 (2007).
[8]Y. Yang, X. Peng, H.-S. Kim, T. Kim, S. Jeon, H. K. Kang, W. Choi, J. Song, Y.-J. Doh, and D. Yu, Nano Lett. **15**, 5875 (2015).
[9]T. Hanrath and B. A. Korgel, J. Phys. Chem. B **109**, 5518 (2005).
[10]M. S. Dunaevskii, P. A. Alekseev, M. I. Lepsa, D. Grützmacher, and A. N. Titkov, Tech. Phys. Lett. **39**, 209 (2013).
[11]A. M. Cowley and S. M. Sze, J. Appl. Phys. **36**, 3212 (1965).
[12]Z. Zhang, K. Yao, Y. Liu, C. Jin, X. Liang, Q. Chen, and L.-M. Peng, Adv. Funct. Mater. **17**, 2478 (2007).
[13]M. Triplett, Y. Yang, F. Léonard, A. A. Talin, M. S. Islam, and D. Yu, Nano Lett. **15**, 523 (2015).
[14]P. Geydt, P. A. Alekseev, M. S. Dunaevskiy, T. Haggrén, J.-P. Kakko, E. Lähderanta, and H. Lipsanen, Lith. J. Phys. **56**, 92 (2016).
[15]A. A. Talin, F. Léonard, B. S. Swartzentruber, X. Wang, and S. D. Hersee, Phys. Rev. Lett. **101**, 076802 (2008).
[16]P. A. Alekseev, M. S. Dunaevskiy, V. P. Ulin, T. V. Lvova, D. O. Filatov, A. V. Nezhdanov, A. I. Mashin, and V. L. Berkovits, Nano Lett. **15**, 63 (2015).
[17]A. A. Talin, F. Léonard, A. M. Katzenmeyer, B. S. Swartzentruber, S. T. Picraux, M. E. Toimil-Molares, J. G. Cederberg, X. Wang, S. D. Hersee, and A. Rishinaramangalum, Semicond. Sci. Technol. **25**, 024015 (2010).
[18]Silvaco Inc., *ATLAS Users Manual* (Silvaco Inc., 2015).
[19]S. M. Sze, *Physics of Semiconductor Devices* (John Wiley & Sons, New York, 1981).
[20]A. M. Lord, T. G. Maffeis, O. Kryvchenkova, R. J. Cobley, K. Kalna, D. M. Kepaptsoglou, Q. M. Ramasse, A. S. Walton, M. B. Ward, J. Köble, and S. P. Wilks, Nano Lett. **15**, 4248 (2015).
[21]G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, IEEE Trans. Electron Devices **39**, 331 (1992).
[22]K. Matsuzawa, K. Uchida, and A. Nishiyama, IEEE Trans. Electron Devices **47**, 103 (2000).
[23]A. C. E. Chia, M. Tirado, Y. Li, S. Zhao, Z. Mi, D. Comedi, and R. R. LaPierre, J. Appl. Phys. **111**, 094319 (2012).
[24]S. G. J. Mathijssen, M. Kemerink, A. Sharma, M. Cölle, P. A. Bobbert, R. A. J. Janssen, and D. M. de Leeuw, Adv. Mater. **20**, 975 (2008).
[25]F. Léonard, A. A. Talin, B. S. Swartzentruber, and S. T. Picraux, Phys. Rev. Lett. **102**, 106805 (2009).
[26]Y. Cui, X. Duan, J. Hu, and C. M. Lieber, J. Phys. Chem. B **104**, 5213 (2000).

05 August 2026 03:57:42