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Gettering of transition metals in high-performance multicrystalline silicon by silicon nitride films and phosphorus diffusion

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ABSTRACT

High-performance multicrystalline silicon (HP mc-Si) from directional solidification has become the mainstream industrial material for fabricating mc-Si based solar cells for photovoltaic applications. Transition metal impurities are inherently contained in HP mc-Si during ingot growth, and they are one of the major efficiency-limiting drawbacks. In this work, we investigate the gettering of transition metals (Cu, Ni, Fe, and Cr) in HP mc-Si wafers along an industrial-standard p-type HP mc-Si ingot, via examining the metal concentration and distribution in the near-surface gettering layers using secondary ion mass spectrometry. We applied both conventional phosphorus diffusion gettering and the recently developed silicon nitride (from plasma-enhanced chemical vapour deposition) gettering techniques. Both techniques are shown to remove significant quantities of metals from the silicon wafer bulk to the surface gettering layers. Improvements in the bulk minority carrier lifetimes throughout the ingot height are also observed by lifetime measurements and spatially-resolved photoluminescence imaging. The gettered Cu and Ni concentrations, as well as the as-grown dissolved Fe concentrations in the silicon wafer bulk, along the HP mc-Si ingot height are shown to follow a similar concentration profile as the metals in conventional mc-Si ingots.

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I. INTRODUCTION

Multicrystalline silicon (mc-Si) from directional solidification is a low-cost silicon material that currently accounts for the majority of the silicon solar panels produced worldwide.[1] The mc-Si material is inherently rich in crystal defects and impurities, which introduce recombination centers in the silicon wafer bulk that limit the conversion efficiency of the solar cells made from these materials.

In recent years, the impact of the crystal defects has been significantly reduced, thanks to the development of the so-called high-performance (HP) mc-Si ingot growth technique, which minimises the propagation of the detrimental dislocation clusters in mc-Si through careful grain size control.[2] Over the last couple of decades, the mc-Si materials are also becoming increasingly cleaner from impurities, particularly metallic impurities, due to better contamination control in the crucible, crucible lining and feedstock, as well as benefiting from an improved understanding of the impurity contamination sources in mc-Si ingot growth processes.[3–7] As a combined result, the current state-of-the-art industrial HP mc-Si materials are of much better quality than those used 5-10 years ago. This is reflected in the higher and more tightly distributed solar cell efficiencies made from such materials.[1,2]

Several groups have reported on the responses of HP mc-Si wafers to the gettering and hydrogenation steps used in solar cell fabrication, mainly from the perspectives of observing changes in the bulk carrier lifetime and recombination activity of the crystal defects.[8–12] Stokkan *et al.* characterised the total metal concentrations in a number of laboratory-scale HP mc-Si ingots via Neutral Activation Analysis (NAA).[3] The same group also used secondary ion mass spectrometry (SIMS) to assess the metal concentrations in dislocation clusters, although

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only Ni could be identified above the detection limit (DL).[11] The concentration and distribution of dissolved, interstitial Fe (Fe_i) in laboratory-scale HP mc-Si ingots were reported in Refs. 13 and 14.

This work will focus on the gettering of metallic impurities in HP mc-Si. In particular, we will examine the concentration and distribution of some of the 3d transition metals that are gettered along a typical industrial-standard p-type HP mc-Si ingot. SIMS is used to measure Cu, Ni, Fe, and Cr depth profiles in surface gettering layers, where the gettered metals are concentrated by a few orders of magnitude compared to the silicon wafer bulk, allowing SIMS measurements above the detection limit. This is similar to the approach used by Bentzen *et al.* for conventional mc-Si wafers.[15] Intra-grain regions of the HP mc-Si wafers will be examined, as a recent study on laboratory-scale HP mc-Si shows that the intra-grain metal concentrations agree better with the average concentrations in cm-sized mc-Si blocks.[3] In addition, probing the intra-grain regions minimises the impact of internal gettering (i.e., gettering by grain boundaries and dislocation clusters) on the measurements that focus on the external gettering by surface layers. Cu, Ni, Fe, and Cr are the most commonly found and detrimental metallic impurities in mc-Si.[3–5,16–18] Although Cu and Ni are known to be more harmful as precipitates, particularly in mc-Si due to the abundant crystal defects that result in the formation of nano- or micro-precipitates,[19] gettering of the dissolved Cu and Ni atoms at elevated temperatures is certainly beneficial for reducing the subsequent precipitate concentrations during the cooldown.

The surface gettering layers used in this work include a conventional phosphorus diffusion gettering (PDG) layer[20] and the recently reported silicon nitride (SiN_x) thin films from plasma-enhanced chemical vapour deposition (PECVD).[21] Both the PECVD SiN_x and atomic layer deposited aluminum oxide dielectric thin films were recently found to have gettering effects for Fe, yet very little is known about the underlying gettering mechanisms.[21–24] Gettering is known to occur via Fe segregation from the silicon wafer bulk to the surface dielectric films at elevated temperatures (examined up to 900 °C).[21,23,24] So far, the gettering effect has only been studied for Fe in intentionally contaminated float-zone silicon (FZ-Si) wafers. The gettering capacity of PECVD SiN_x films for other metallic impurities, and its application on mc-Si wafers, will be assessed in this work.

Changes in the silicon wafer bulk before and after gettering are monitored by effective minority carrier lifetime[25] and spatially-resolved photoluminescence imaging.[26] Apart from SIMS which measures the total metal concentrations regardless of the chemical state, the dissolved, interstitial Fe concentrations in the silicon wafer bulk are also measured by a lifetime-based Fe-B pair dissociation technique.[27–29] The simulation of diffusion-limited gettering of metals is presented and discussed.

II. EXPERIMENTAL DETAILS

The multicrystalline silicon wafers used in this work came from a state-of-the-art industrial G6-scale HP mc-Si ingot, manufactured at Jinko Solar, China. The ingot was p-type boron-doped, and the brick studied was from the center of the ingot away from the crucible walls. The wafers came from four different height positions along the HP mc-Si brick: near-bottom (15% of the ingot height from the bottom), middle (48%), near-top (90%), and top red-zone regions. The boron dopant concentrations were 8.7×10^{15}, 9.4×10^{15}, 1.2×10^{16}, and 1.3×10^{16} cm^{-3}, respectively.

Two sister wafers from each ingot height were used in this experiment. The 156 mm × 156 mm wafers were cut into 9 pieces for ease of handling. The wafers were 185 ± 10 μm thick after saw damage etching in an HNO_3-HF solution. Two pieces of the sister wafers from each ingot height were then cleaned and coated with PECVD SiN_x films on both sides. The PECVD process conditions and film properties can be found in Ref. 21. The deposition process is known to cause some impurity gettering effects,[21,30] as the wafers were held at elevated temperatures (in this case, the sample holder temperature was ~250 °C for a total of 1 h) where some metals are sufficiently mobile to reach the wafer surfaces. The SiN_x coated samples were then annealed at 700 °C for 90 min in N_2 in a quartz tube furnace. The temperature and time were chosen such that Cr, which has the slowest diffusivity out of the four metals, has sufficient time to reach the surface SiN_x layers.[18] One set of the sister wafers from each ingot height was then characterised by SIMS for the metal concentrations in the annealed SiN_x films and the near-surface silicon regions. The other set of wafers underwent chemical etching to remove the annealed SiN_x films (the passivation effect of which was degraded after annealing), and a few μm of the silicon wafer surfaces, before being cleaned and re-coated with fresh SiN_x films on both sides to allow bulk lifetime measurements.

An additional two sister wafer pieces from the same red-zone mc-Si wafers were subjected to phosphorus diffusion after saw damage etching and cleaning. Phosphorus diffusion was carried out in $POCl_3$ in a quartz tube furnace. The $POCl_3$ diffusion was at 810 °C for a total of 40 min (including deposition, drive-in, and oxidation), and the temperature ramp-up and ramp-down rate was at 10 °C/min from and to 700 °C. This resulted in a sheet resistance of 100 Ω/square for the phosphorus doped silicon surface layer, as measured by a four-point probe. The depth profile of the electrically active phosphorus concentration was measured by electrochemical capacitance-voltage (ECV) profiling, using a WEP Wafer Profile CVP21 instrument. After phosphorus diffusion, one of the sister wafers was characterised by SIMS, which had the phosphosilicate glass (PSG) retained on the wafer surfaces as a surface contamination barrier. The other sister wafer had the PSG and the phosphorus doped silicon layers chemically etched off, and the wafer was then cleaned and coated with PECVD SiN_x films on both sides to enable bulk lifetime measurements.

Electronic-grade FZ-Si wafers were included in all of the PECVD deposition processes in order to monitor the SiN_x surface passivation quality. The FZ-Si wafers were p-type boron-doped with a dopant concentration of 1.5×10^{16} cm^{-3}

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and were 200 μm thick after etching. Effective surface recombination velocity (SRV) of the as-deposited SiN_x films was estimated from the carrier lifetime measurements of the FZ-Si control samples, assuming a bulk lifetime that is only limited by Auger and radiative recombination.[31,32] The extracted SRV was then used to estimate the surface-limited carrier lifetimes ($\tau_{surface}$) for the mc-Si wafers with SiN_x films. However, as recently pointed out by Grant *et al.*, high purity FZ-Si wafers could contain bulk defects that become recombination active upon thermal processing.[33] The extracted $\tau_{surface}$ therefore represents a *lower limit* of the surface-limited lifetimes. This probably explains why the middle HP mc-Si sample after gettering has a higher lifetime than the lower limit of the surface lifetime in Sec. III A.

Photoconductance lifetime measurements[25] and photoluminescence (PL) imaging[26] were applied to characterise the bulk of the HP mc-Si wafers before and after gettering. The tools used were a WCT-120 Sinton lifetime tester and a BTimaging LIS-R1 PL imager. The calibration method described in Ref. 34 was employed to convert the spatially resolved PL signals to excess minority carrier density images. The interstitial Fe concentration ($[Fe_i]$) in the silicon wafer bulk, before and after gettering, was also measured by these lifetime-based tools, based on the well-established technique of comparing the effective carrier lifetimes before and after Fe-B pair dissociation via illumination.[27–29] Error bars in the Fe_i concentrations arose from assuming a 5% uncertainty in the measured effective carrier lifetimes before and after pair dissociation. The $[Fe_i]$ detection limit for the given lower limit of $\tau_{surface}$ and a lifetime uncertainty of 5% is around $3 \times 10^9\ cm^{-3}$.

SIMS depth profiling was used to measure the Cu, Ni, Fe, and Cr concentrations in the near-surface regions, in the SiN_x/Si and PSG/P-doped Si/Si samples. The SIMS measurements were conducted by EAG Laboratories. The Si and P raw ion counts were monitored in order to identify the boundaries of the different surface layers. The nominal depth resolution was ∼2 nm/step, although the actual resolution was much larger as the sputtered ions become intermixed during the depth profiling. The metal concentrations were quantified based on implanted calibration standards and relative sensitivity factors.

The SIMS depth profiles typically suffer from surface-related measurement artefacts and surface contamination, which manifest themselves as apparent sharp increases toward the wafer surfaces in the top tens of nm, as marked in the SIMS plots below. These regions are disregarded from the analysis. Integrating the SIMS metal profiles allows us to estimate the gettered metal concentrations. An example is shown in Fig. 1, where the shaded region is the area under the curve that the integration took place for the red data curve (Ni gettered to SiN_x in a top red-zone mc-Si wafer). As shown in Fig. 1, the near-surface region is excluded from the integration, and so is the possible smearing of the surface contamination/artefacts further into the depth profiles, as represented by the fitted curves. In this work, we estimated the smeared surface effect by fitting a power-law curve to the near-surface contamination/artefact region and then extrapolated it to deeper into the profile. A power-law curve was chosen as it seems to fit well with the SIMS profiles of the no-Fe control samples from our previous works.[21,23] The SIMS detection limit (DL) is also considered and subtracted from the data curve (if DL is higher than the fitted "artefact curve"), as shown by the shaded area in Fig. 1. The concentration estimation was integrated until the depth where the signal reaches the detection limit, as the metal-related signal is also smeared deeper into the bulk. The reported error bars in the gettered metal concentrations came from the uncertainty in SIMS calibration factors (provided by EAG Laboratories).

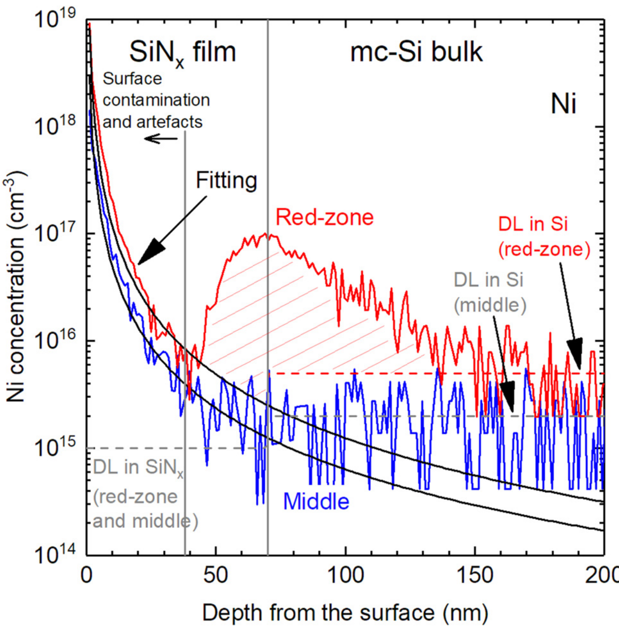

FIG. 1. SIMS Ni profiles in SiN_x/Si samples (SiN_x gettering 700 °C 90 min), where the substrate Si wafers came from the top red-zone and middle positions of an HP mc-Si ingot. The shaded region denotes the integration area for estimating the gettered Ni concentration of the top red-zone sample.

For samples with relatively low gettered metal concentrations, such as the blue data curve in Fig. 1 (Ni gettered to SiN_x in a middle mc-Si wafer), the uncertainty in estimating the surface smearing effect is too significant to allow an accurate extraction of the gettered metal concentration. These are therefore noted as "below SIMS limit" in Sec. III D.

SIMS was used to probe the intra-grain regions of the HP mc-Si wafers, at least 2 mm from any grain boundaries or dislocation clusters (except for the near-bottom wafer which has very small grains). As the wafer thickness (<200 μm) is much shorter than the distance to crystal defects, external gettering to the wafer surfaces (SiN_x or phosphorus diffused region) is the more dominant effect compared to internal gettering to crystal defects.

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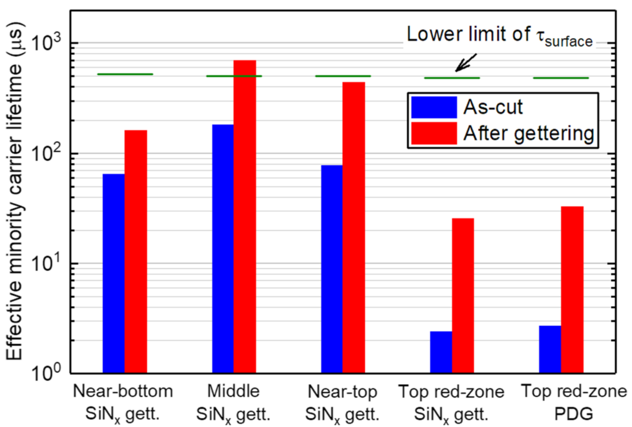

FIG. 2. Average effective minority carrier lifetime before and after gettering, by either annealing with SiN_x films at 700 °C for 90 min, or undergoing $POCl_3$ diffusion at 810 °C for 40 min (with a ramp-up and cooldown rate of 10 °C/min from and to 700 °C). All samples had as-deposited PECVD SiN_x films on both sides as surface passivation layers. The average lifetimes were from photoconductance measurements at an injection level of 10^{15} cm^{-3}, in the Fe-B dissociated (i.e., isolated Fe_i) state.

III. RESULTS AND DISCUSSION

A. Changes in HP mc-Si wafer bulk

As shown in Fig. 2, all of the tested HP mc-Si wafers along the ingot height experienced an increase in the effective carrier lifetime after gettering by either phosphorus diffusion or annealing with SiN_x films. As the FZ-Si controls were found to have largely consistent lifetimes for the different PECVD deposition runs, these changes in the effective lifetimes indicate lifetime improvements in the bulk of the HP mc-Si wafers. However, because of the moderate surface passivation quality, the effective lifetime of some of the HP mc-Si wafers, particularly the middle and near-top wafers, likely becomes almost entirely limited by the surface, making it difficult to accurately extract the lifetime increases in the mc-Si wafer bulk. Nevertheless, it appears that the near-bottom HP mc-Si wafer underwent the smallest lifetime improvement, likely due to its high density of recombination active grain boundaries. The microstructure of the HP mc-Si wafers from different ingot positions can be found in Ref. 8, which showed PL images of wafers from the same ingot and from very similar ingot positions.

The lifetime profile with respect to the ingot height is consistent with previous reports.[8,11] The top red-zone wafers demonstrate the lowest lifetimes both before and after gettering, as they are limited by impurities and defects in the silicon wafer bulk. For these red-zone wafers undergoing either SiN_x gettering or phosphorus diffusion gettering, similar bulk lifetime improvements are observed in Fig. 2.

An example of the PL images before and after gettering is shown in Fig. 3, for a top red-zone wafer undergoing SiN_x gettering. Under the same 808-nm laser excitation of 5×10^{16} cm^{-2} s^{-1} (equivalent to approximately 0.2 suns), the light-generated excess minority carrier density (Δn) is increased by one order of magnitude after gettering, from an average Δn of 2×10^{12} cm^{-3} in the as-cut state (with only saw damage etching and SiN_x coating), to 3×10^{13} cm^{-3} after SiN_x gettering and re-coating.

For all samples along the mc-Si ingot, hydrogenation of the crystal defects is not observed here after the 700 °C 90-min SiN_x annealing treatment. This is likely due to the extended annealing time that caused the onset of dehydrogenation in this case. The SiN_x film used in this work is

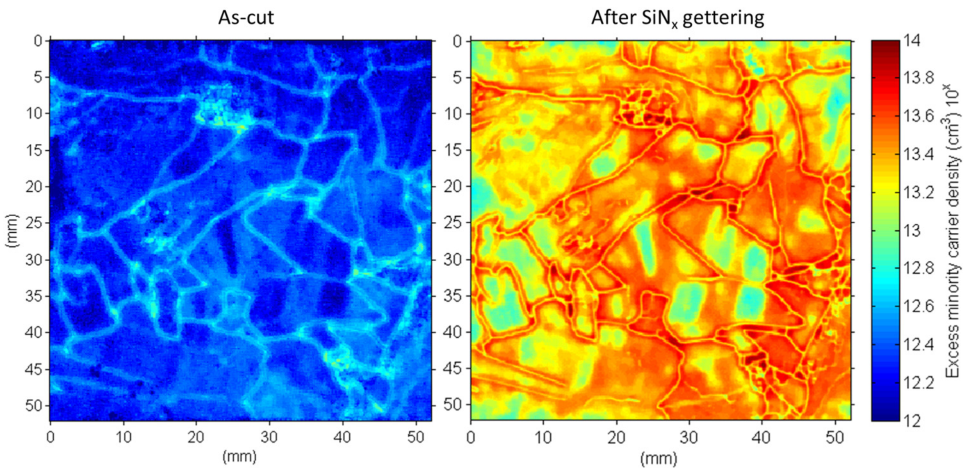

FIG. 3. PL images of the excess minority carrier density in a top red-zone wafer before and after SiN_x gettering (700 °C, 90 min). The wafer had fresh as-deposited PECVD SiN_x films on both sides as surface passivation layers. The PL images were taken under the same 808-nm laser excitation intensity of 5×10^{16} cm^{-2} s^{-1} (0.2 suns). Note that the color bar for carrier density is on a logarithmic scale.

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thermally unstable, and its dehydrogenation is also reflected in its much degraded surface passivation quality after annealing.[35] Our recent study on a range of PECVD SiN_x films indicates that both thermally stable and unstable films generate similar gettering effects for Fe.[22] The balance between hydrogenation and dehydrogenation relates to the SiN_x film properties,[35] which in turn determine whether or not the benefits of bulk hydrogenation and impurity gettering can be achieved in a single annealing step with the SiN_x films.

The dissolved, interstitial Fe (Fe_i) concentration in the silicon wafer bulk in the as-cut state was found to be reduced by at least an order of magnitude after gettering, regardless of the gettering method or the ingot height position. This is as expected from the known diffusivity of Fe in silicon,[36] the gettering effectiveness of phosphorus diffusion for Fe,[20,37] and that the SiN_x gettering of Fe was reported to be largely diffusion-limited below 700 °C.[21] The bulk Fe_i concentrations will be presented and discussed later in Sec. III D.

B. Metals gettered to the phosphorus diffused surface regions

The near-surface depth profiles of the metals, as well as the electrically active P dopant concentrations, are shown in Fig. 4 for the phosphorus diffused red-zone HP mc-Si wafer.

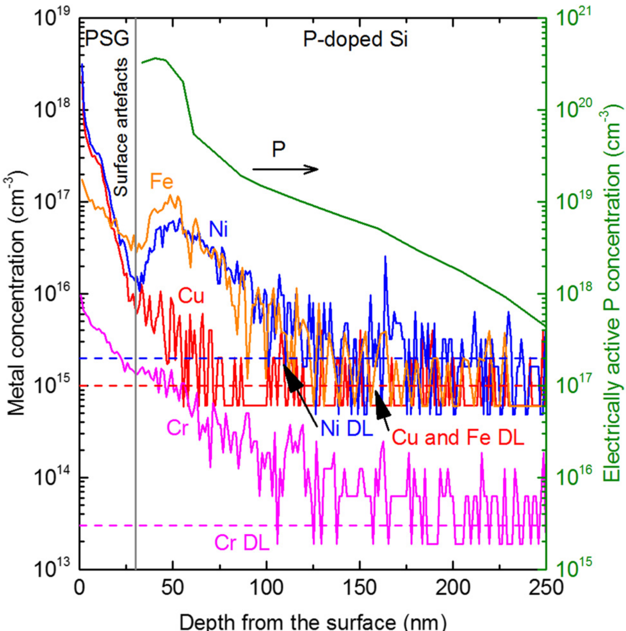

FIG. 4. SIMS depth profiles of the Cu, Ni, Fe, and Cr concentrations in a PSG/P-doped Si/Si sample. The Si substrate was an HP mc-Si wafer from the top red-zone region of the ingot. An 810 °C 40-min $POCl_3$ diffusion (10 °C/min from and to 700 °C) was carried out to getter the metals to the surface regions. The SIMS metal detection limits (DL) are included as dashed lines. An ECV depth profile of the electrically active phosphorus dopant concentration is shown as well.

Note that the apparent sharp increases toward the wafer surface in the PSG layer are likely caused by surface contamination and surface-related measurement artefacts.

The phosphorus diffusion condition used in this work represents a typical process used in cell fabrication. As shown in Fig. 4, the phosphorus diffusion results in all four metals, Cu, Ni, Fe, and Cr, being gettered to the P diffused silicon surface regions. The SIMS metal profiles coincide well with the ECV active P dopant profile, which indicates that the metals are preferentially segregated to the heavily P doped silicon, agreeing with the literature.[37,38]

C. Metals gettered to the SiN_x surface regions

Figure 5 presents the near-surface metal profiles of the HP mc-Si wafers which underwent SiN_x gettering. The SiN_x/Si interfaces were identified from monitoring the raw ion counts of the silicon matrix. Again, the sharply increasing metal profiles in the top 30–40 nm, which have similar slopes irrespective of the mc-Si wafer substrates, are due to surface contamination and surface-related measurement artefacts, as marked in the figure.

As shown in Fig. 5, all four metals, Cu, Ni, Fe, and Cr, can be measured above the respective detection limit, and some above the possible impact of surface artefacts, at the SiN_x/Si interfaces and/or within the bulk of the SiN_x films, particularly for the top red-zone wafer. This clearly demonstrates the gettering of these metals to the SiN_x surface regions.

For each metal, the concentration and shape of the profile in the SiN_x gettering layers exhibit variations along the HP mc-Si ingot height. For Cu [Fig. 5(a)], while the middle and near-top wafers demonstrate Cu accumulation only in the bulk of the SiN_x films, the near-bottom and top red-zone wafers show additional Cu accumulation at the SiN_x/Si interfaces. Ni [Fig. 5(b)] exhibits a clear trend in the concentration of the broad interface peak with respect to the ingot height—the Ni concentration is highest in the top red-zone wafer, followed by near-top, near-bottom, and middle wafers. In Fig. 5(c), the top red-zone wafer shows a prominent Fe peak near the SiN_x/Si interface, while the other three wafers display a much flatter profile in the bulk of the SiN_x films, some with a smaller amount of Fe near the interfaces as well. Figure 5(d) shows that in the near-bottom, middle, and near-top HP mc-Si wafers, a gradually decreasing profile of Cr can be found, which may be affected by the surface artefacts; whereas in the top red-zone wafer, Cr is mostly aggregated in the SiN_x film near the interface.

Note that the SIMS depth profiles are somewhat smeared by the intermixing of the sputtered ions during measurements, and therefore the metal profiles in Fig. 5 cannot be used to infer the exact width of the gettering regions or layers. The extent of the interface peaks into the silicon wafer substrate is also likely to be attributed by this ion smearing effect.

It is interesting to observe that some of the gettered metal profiles in Fig. 5 differ from the gettered Fe profiles reported in Ref. 21, where Fe, being the only intentional

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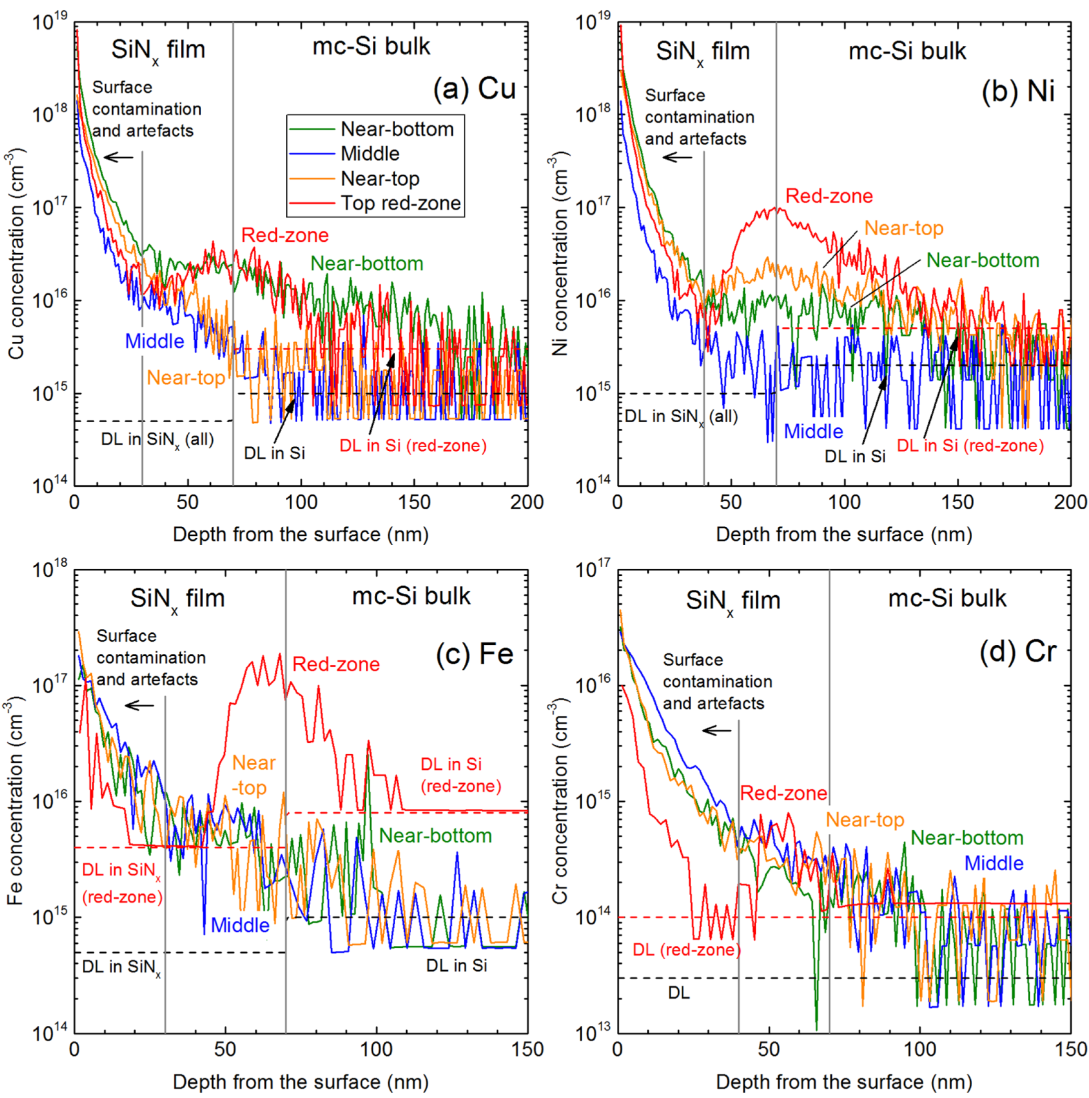

FIG. 5. SIMS depth profiles of the Cu, Ni, Fe, and Cr concentrations in SiN_x/Si samples. The Si wafer substrates were from near-bottom, middle, near-top, and top red-zone regions of an HP mc-Si brick. After coating with SiN_x films on both sides, the SiN_x/Si samples were annealed at 700 °C for 90 min to enable the gettering of metals to the surface regions. The SIMS metal detection limits (DL) are included as dashed lines.

contaminant in the silicon wafer bulk, was found to be mostly aggregated to the bulk of the SiN_x films, with a tail into the silicon wafer substrate which is possibly due to the ion smearing effect. However, some of the metal profiles in Fig. 5, particularly the ones with a high metal concentration from the top red-zone region, show obvious peaks at the SiN_x/Si interfaces. Interaction of multiple metals may have assisted in the preferential gettering at the interfaces, similar to the co-location of multiple metal clusters during ingot growth.[5,39] The different profiles may also be caused by the different amounts of metal impurities being gettered to the SiN_x surface regions. In Ref. 21, $9 \times 10^{12}\,cm^{-3}$ or $5 \times 10^{12}\,cm^{-3}$ Fe atoms were intentionally introduced into clean FZ-Si wafers, whereas the mc-Si wafers, particularly the top red-zone wafers, inherently contain much more impurities of higher concentrations (some of the gettered metal concentrations can be seen in Fig. 6). If there were limited gettering sites in the bulk of the SiN_x films and the defective SiN_x/Si interfaces could allow for more impurity accumulation, a high concentration of impurities may be found near the interface after the saturation in the films. This could also explain the flatter metal profiles in the mc-Si samples with lower metal

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concentrations (for example, the Ni, Cu, and Fe profiles of the wafers from near-bottom, near-top, and middle of the ingot), as shown in Fig. 5. Similar SIMS Fe profiles have also been reported in Ref. 40 for the conventional mc-Si wafers after low temperature anneals, where there is no interfacial Fe peak. Further work is required to examine these speculations.

D. Gettered metal concentrations

The concentration of metals being gettered from the silicon wafer bulk to the surface regions can be estimated from integrating the SIMS profiles, as detailed in Sec. II. The results are shown in Fig. 6. Those with relatively low concentrations, where the uncertainty in separating signal from surface artefact/contamination is large, are marked as "Below SIMS limit" in Fig. 6. The concentrations of these samples, however, are not necessarily below the lower end of the *y*-axis (10^{10} cm^{-3}) in Fig. 6. Note that gettering layers were in fact present on both sides of the wafer surfaces, and Fig. 6 presents the gettered metal concentrations in one side of the gettering layers.

Comparing two pieces of a top red-zone wafer undergoing either PDG or SiN_x gettering, it can be seen from Fig. 6 that similar concentrations of Ni and Fe were gettered. The gettered Cu and Cr concentrations, on the other hand, are below the SIMS uncertainty range in the phosphorus diffused sample. The difference in the two gettering layers could be simply caused by the large lateral inhomogeneity of the impurity distribution across a top red-zone mc-Si wafer. Nevertheless, the comparison in Fig. 6 confirms that the SiN_x surface regions can effectively getter metals in addition to Fe, similar to the conventional PDG.

Figure 6 also presents the concentration of metals being gettered to the SiN_x surface regions for wafers that are from different height positions of the HP mc-Si ingot. The as-cut bulk Fe_i concentrations in these wafers are also shown. The gettered Ni and Cu concentrations, as well as the as-cut bulk Fe_i, follow the general trend of the metal profiles in a directionally solidified conventional mc-Si ingot—that is, the metal concentration is high in the bottom due to solid-state in-diffusion from the crucible bottom, lowest in the middle, and becomes increasingly higher toward the ingot top because of the combined effect of impurity segregation (i.e., Scheil distribution) and solid-state back-diffusion from the highly contaminated ingot top.[4] As it is not possible to track the same grain throughout the ingot height, the comparison of the gettered metal concentrations along the ingot is affected, to some extent, by the lateral inhomogeneity across the examined mc-Si wafers.

Note that the *gettered* metal concentration reported here is a fraction, possibly a large fraction,[41] of the *total* metal concentration in silicon, as metal precipitates and compounds may not fully dissolve and diffuse to the gettering sites during the process. Nevertheless, the trend of the gettered metal concentrations and the as-cut bulk Fe_i concentrations suggests that the contamination sources and incorporation mechanisms likely remain unchanged for the HP mc-Si ingots. This agrees with the literature that the crucible and crucible coating, rather than the crystallisation technique, are identified as the most important contamination sources in directionally solidified mc-Si.[3,42,43]

Although the *gettered* metal concentrations should not be directly compared with the *total* metal concentrations reported in the literature,[3–5,41] a comparison can be made on the as-cut bulk Fe_i concentrations. The p-type HP mc-Si

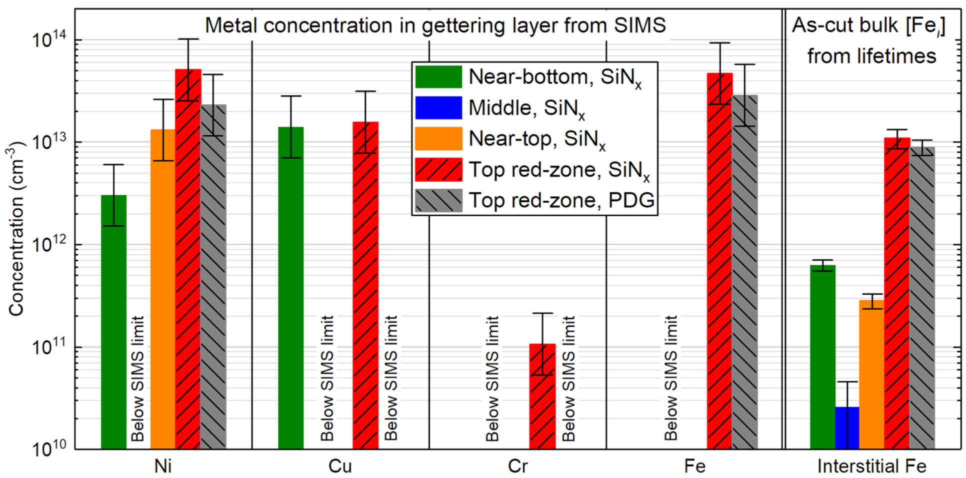

FIG. 6. Concentrations of Ni, Cu, Cr, and Fe that are gettered to the surface layer of either SiN_x (700 °C 90 min) or phosphorus diffused silicon ($POCl_3$ diffusion 810 °C 40 min), from integrating SIMS profiles. The interstitial Fe concentrations in the silicon wafer bulk in the as-cut state prior to gettering, as measured from carrier lifetimes, are also shown. The silicon wafers come different positions along an HP mc-Si ingot.

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wafers studied here are shown to have lower Fe_i concentrations throughout the ingot height as compared to the conventional mc-Si wafers in Refs. 4, 40, and 44. This is a good indication of the much-improved impurity control in this new generation mc-Si material.

For the top red-zone wafers which have unambiguous SIMS signals, Fig. 6 also shows that the concentrations of Fe being gettered to the surface regions (SiN_x or PDG) are higher than the corresponding as-cut bulk Fe_i concentrations prior to gettering. Although we cannot entirely rule out the contribution of other metal-related complexes and defects (which might exist in silicon according to the theoretical calculations[45,46]) to the gettered Fe concentrations, Fe precipitate dissolution and subsequent gettering seems to be the more likely explanation in mc-Si from numerous experimental reports.[12,47–50]

E. Modeling diffusion-limited gettering of metals

Figure 7 models the time and temperature required to getter 99% of the initially dissolved, mobile 3d transition metals in silicon, assuming a typical HP mc-Si solar cell thickness of 170 μm, and that both wafer surfaces act as infinite gettering sites.[51] That is, the gettering process is assumed to be only limited by the diffusion of metals in silicon. For Ni, Co, Mn, and Cr, the available diffusivity parameters were derived from data at temperatures above 900 °C[18] or 665 °C (Ni),[52] and hence the extrapolated diffusivities are used for modeling, as denoted by dashed lines in Fig. 7. The diffusivity parameters of Cu and Fe are from Refs. 19 and 36.

The diffusion-limited gettering assumption means that the simulation in Fig. 7 represents the *minimum* time required to getter 99% of the dissolved metal at a given temperature, as the gettering processes are in some cases also limited by the gettering reactions. For instance, the gettering kinetics of Fe by PECVD SiN_x films were found to be largely limited by the Fe diffusivity at temperatures below 700 °C, and at higher temperatures of 800 °C–900 °C, the kinetics become reaction-limited.[21] It is uncertain at this stage whether the SiN_x gettering of other metals, especially the fast-diffusing metals, follows similar diffusion-limited kinetics at moderate or low temperatures. The gettering reaction at PDG layers depends on the diffusion parameters, e.g., the dopant concentration, oxygen, vacancy injection, etc, and the gettering kinetics also change during the dynamic thermal diffusion processes.[37,38] Furthermore, in mc-Si materials, precipitate dissolution and metal interaction with crystal defects affect the final gettering effects as well.

Nevertheless, the simulation in Fig. 7 suggests that the fast-diffusing metals of Cu, Ni, and Co have the potential to be effectively gettered within seconds or tens of seconds at typical contact firing temperatures (700–850 °C), or even at lower temperatures if they were not yet precipitated. Mn, Fe, and Cr, on the other hand, require minutes to tens of minutes to reach the wafer surfaces at 700–900 °C. Although they could not be completely removed during typical contact firing, their diffusivities are probably not a limiting factor for gettering by phosphorus diffusions which typically last tens of minutes or even longer.

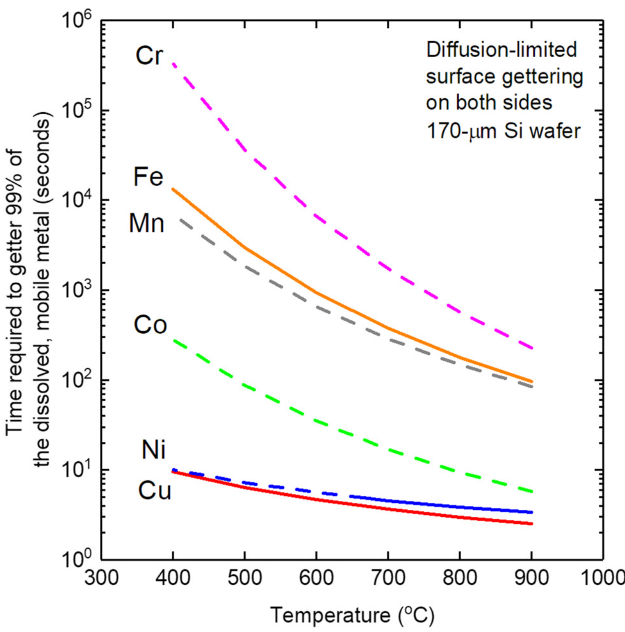

FIG. 7. Modeled time and temperature required to getter 99% of the dissolved, mobile metal concentrations in a 170-μm thick silicon wafer with infinite gettering sites on both wafer surfaces. The dashed lines were modeled based on the extrapolation of the available diffusivity parameters in the literature,[18,52] whereas the solid lines used the reported diffusivity parameters in Refs. 19, 36, and 52.

IV. CONCLUSION

In summary, this work investigates the concentration and distribution of metallic impurities (Cu, Ni, Fe, and Cr) in the near-surface gettering layers after either a typical phosphorus diffusion, or a PECVD SiN_x gettering process, for silicon wafers from different height positions along an industrial-standard p-type HP mc-Si ingot. Metals were found to be aggregated to the surface gettering layers, accompanied by lifetime enhancements in the bulk of the HP mc-Si wafers throughout the ingot height, which demonstrates the continued importance of gettering for this new generation mc-Si material. For the top red-zone HP mc-Si wafers compared in this work, the phosphorus diffused silicon regions and the SiN_x surface layers resulted in similar gettering effects, confirming that metals in addition to Fe could be effectively removed by the PECVD SiN_x films at elevated temperatures.

The gettered Cu and Ni concentrations and the as-cut bulk dissolved Fe concentrations along the HP mc-Si ingot height were revealed to follow a similar trend as the metals in the conventional mc-Si: that is, the metal concentration is high in the top and bottom, and lowest in the middle of the ingot, due to the combined effects of impurity segregation (i.e., Scheil distribution) and solid-state in-diffusions from the

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ingot top and bottom. This suggests that similar contamination sources are still present in this new generation mc-Si material, although the concentration has been substantially reduced.

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