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Xiaoming Yuan,[1,a)] Dong Pan,[2,3] Yijin Zhou,[1] Xutao Zhang,[4] Kun Peng,[5] Bijun Zhao,[6] Mingtang Deng,[7,a)] Jun He,[1,a)] Hark Hoe Tan,[6,8] and Chennupati Jagadish[6,8]

AFFILIATIONS

[1]Hunan Key Laboratory of Nanophotonics and Devices, School of Physics and Electronics, Central South University, 932 South Lushan Road, Changsha, Hunan 410083, People's Republic of China
[2]State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences, P.O. Box 912, Beijing 100083, China
[3]Beijing Academy of Quantum Information Sciences, Beijing 100193, People's Republic of China
[4]MOE Key Laboratory of Material Physics and Chemistry under Extraordinary Conditions and Shaanxi Key Laboratory of Optical Information Technology, School of Physical Science and Technology, Northwestern Polytechnical University, Xi'an 710129, People's Republic of China
[5]Department of Physics, University of Oxford, Clarendon Laboratory, Parks Road, Oxford OX1 3PU, United Kingdom
[6]Department of Electronic Materials Engineering, Research School of Physics, The Australian National University, Canberra, Australian Capital Territory 2601, Australia
[7]Institute for Quantum Information and State Key Laboratory of High Performance Computing, College of Computer Science and Technology, National University of Defense Technology, Changsha 410073, People's Republic of China
[8]ARC Centre of Excellence for Transformative Meta-Optical Systems, Research School of Physics, The Australian National University, Canberra, Australian Capital Territory 2601, Australia

[a)]**Authors to whom correspondence should be addressed:** xiaoming.yuan@csu.edu.cn; junhe@csu.edu.cn; and mtdeng@nudt.edu.cn

ABSTRACT

Selective area epitaxy (SAE) can be used to grow highly uniform III–V nanostructure arrays in a fully controllable way and is thus of great interest in both basic science and device applications. Here, an overview of this promising technique is presented, focusing on the growth fundamentals, formation of III–V nanowire arrays, monolithic integration of III–V nanowire arrays on silicon, the growth of nanowire heterostructures, and networks of various shapes. The applications of these III–V nanostructure arrays in photonics, electronics, optoelectronics, and quantum science are also reviewed. Finally, the current challenges and opportunities provided by SAE are discussed.

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I. INTRODUCTION

Bottom-up epitaxy of III–V semiconductor nanostructures is an excellent technique to produce a diverse range of "building blocks" for nanoscale electronic, photonic, and optoelectronic device applications.[1,2] Among the synthesis methods, selective area epitaxy (SAE) receives increasing interest thanks to its several distinct advantages. First, SAE is a scalable method to produce uniform nanowire arrays.[3,4] Second, the density, position, diameter, and pattern can be arbitrarily designed and controlled to form arrays of different nanostructures. Third, the localized nature of SAE could mitigate lattice and thermal mismatch–induced stress, thus reducing the dislocation density and wafer bowing effect. Finally, the dielectric mask layer and uniform property make SAE an ideal epitaxy approach for device fabrication. In addition to nanowires, SAE can be used to grow III–V semiconductor nanostructure arrays with different shapes and geometry, such as nanomembranes, nanorings, and in-plane nanowires, by creating the appropriate patterns on the dielectric mask.[5–9] This growth method has been used to synthesize nanowire networks for realizing topologically protected Majorana-based qubits.[10–13] SAE can also be extended to realize advanced integration of III–V nanostructures onto silicon substrates. Borg and IBM researchers developed a template-assisted selective epitaxy (TASE) method to grow III–V nanostructure arrays on silicon-on-insulator (SOI) substrates.[14–16] This method shows advantages both in reducing threading dislocations and fabricating complex III–V nanostructure arrays in both vertical and horizontal forms, which are very attractive for silicon photonics and electronics applications.[14,17–19] Moreover, metal catalysts can be introduced into the openings of the mask to bring more feasibility in controlling growth.[20] By this so-called selective area (SA) vapor-liquid-solid (VLS) approach, growth conditions can be easily tuned to form axial[21–23] and lateral[24,25] nanowire heterojunctions as well as nanowire networks,[26,27] which have been utilized for single-photon emission,[28,29] solar cell,[25] lasing,[30] and photodetection[31,32] applications. Advances in different research fields with nanostructures grown by SAE demonstrate that this technique is fast becoming the method of choice to create nanostructures and network arrays with high crystal quality and superior uniformity for photonic, electronic, optoelectronic,[33,34] and quantum science applications. Here, we review the recent development of III–V nanostructure arrays produced by SAE and suggest several possible future directions.

II. PRINCIPLE OF SELECTIVE AREA EPITAXY

SAE is a localized growth approach that can be realized in different epitaxial techniques, such as metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), and chemical beam epitaxy (CBE). By carefully adjusting the growth parameters, semiconductor layers only grow selectively on the exposed regions of the substrate, which is otherwise covered by a layer of dielectric mask. The general approach of SAE is illustrated in Fig. 1. First, a thin layer of dielectric mask is deposited on the substrate. After spin coating of a thin electron-resist layer, nanoscale hole patterns are written and transferred onto the mask layer, exposing the equivalent regions of substrate. Finally, these patterned substrates are loaded into the reactor for nanowire growth. Metal catalysts can be introduced into the openings to add another dimension of controllability during the growth of nanowires. In addition, various patterns such as slots or rings and networks of stripes can be patterned to create more interesting nanostructures.

A. Mask selection

The basic requirements for the mask materials are as follows. First and most important, the sticking coefficient of adatoms on the mask should be as low as possible to avoid parasitic growth. Consequently, nucleation and crystal growth only occur in the openings that expose the underlying substrate instead of the mask layer.[35] Second, the mask should be heat tolerant to withstand the high growth temperature. Third, the mask should be inert to the carrier gas and precursors. Finally, the mask layer should be compatible with the subsequent processing technique (e.g., dry or wet etching). Considering these requirements, SiN_x, SiO_x, and Al_2O_3 films are commonly used as masks. It is worth mentioning that the mask material can cause unintentional doping, as demonstrated during the GaN film growth where SiO*x* and tungsten masks lead to a high concentration of Si and oxygen doping, respectively.[36]

In addition to growth selectivity, the mask layer can act in other specific roles, such as a barrier layer to inhibit metal catalyst movement and agglomeration during VLS growth. This is very useful when the contact angle of the catalyst droplet is too small to favor vertical nanowire growth, as applied in the growth of stemless III-Sb nanowire arrays.[37–39] The mask layer can also be effective in prohibiting the propagation of threading dislocations and has been applied to reduce the defect density of III–V nanostructures grown on lattice-mismatched substrates.[40] Other mask materials are also being investigated to realize specific roles. For instance, HfO_2 mask can be used for the integration of a high-mobility InGaAs semiconductor array with high-k dielectric materials for 3D device architectures.[41] Metal mask layer is used for bottom electrode fabrication, such as the W mask in InAs nanowire array field effect transistors (FETs).[42] Oto *et al.*[43] demonstrated that Ti metal mask can reduce the diameter of GaN nanowires.

B. Pattern design

The openings on the mask shape can be prepared via several different patterning techniques. Deep ultraviolet (UV) lithography is mainly used in the industry, which is the technique of choice in a high-volume production environment. Electron beam lithography (EBL) is widely used in research thanks to its ability in producing complex patterns. However, the "serial" nature in the pattern writing process makes it impractical for wafer-scale patterning. Nanoimprint lithography technique, on the other hand, has the advantages for wafer-scale pattern preparation and with significantly less cost than EBL. However, its main limitations are wear and tear of the

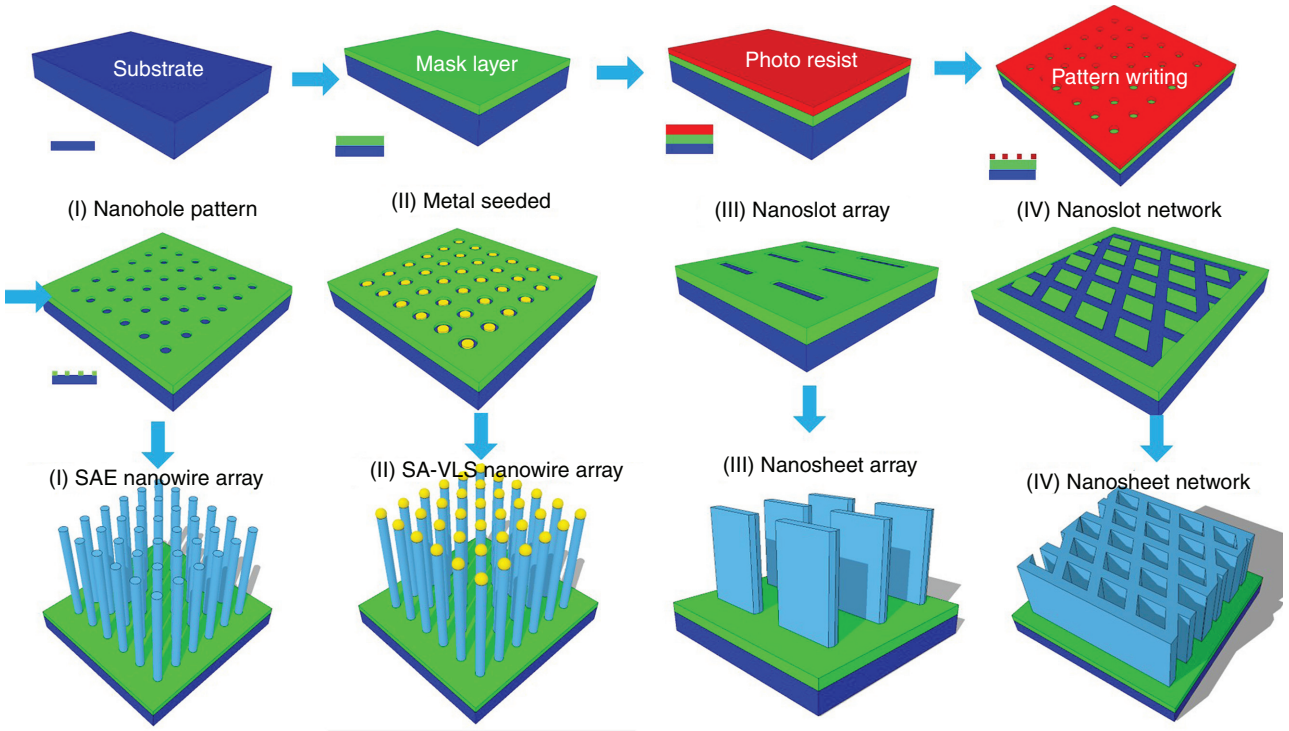

FIG. 1. Illustration of the SAE growth method from nanowire and nanosheet arrays to nanosheet networks.

nanoimprint stamp and less developed patterning process in terms of accuracy and reproducibility. All these techniques require the use of photoresist or electron resist that need further cleaning process. In comparison, focused ion beam directly writes the patterns on the mask without the use of resist.[44,45] However, it has limitations in both resolution and ion beam damage compared with EBL. Nanosphere lithography, which is a facile and low-cost technique, has been widely used for top-down fabrication processes and can be extended to patterning the wafers over large areas.[46,47] However, this method is limited in resolution or complex pattern formation.

C. Growth method

In general, SAE can be performed in MBE, MOCVD, and CBE. Solid-source MBE takes place under ultra-high vacuum, which has the advantage of minimal impurity incorporation. Moreover, the high vacuum maintains a clean nanostructure surface for subsequent processes, such as superconducting metal epitaxy for quantum science applications.[12,13] MBE can be combined with other advanced techniques (e.g., reflection high-energy electron diffraction, x-ray photoelectron spectroscopy) for *in situ* characterization. In addition, MBE is a good platform for studying the growth mechanism, as the reaction processes are simple and carried out in a clean environment. However, the low growth rate and the requirement of an ultra-high vacuum system restrict its use primarily for research or in very specialized applications. In comparison, MOCVD has the advantage of fast growth rates and compatibility with large-scale production. Moreover, fundamentally, the sticking coefficient of precursor adatoms in MOCVD is smaller than in MBE, making SAE easier.

D. Growth fundamentals

SAE relies on the interplay between the sticking coefficients and diffusion length of adatoms on the mask, which is tunable by adjusting the growth conditions such as V/III ratio and growth temperature. Thus, careful attention to the growth conditions is required to achieve selectivity between deposition at the openings and the mask. During the initial stage of growth, nucleation occurs in the openings followed by a gradual filling up of the openings. During this period, the growth direction and crystal phase are mainly determined by the crystal structure of the underlying substrate. Epitaxy then continues and extends outside the mask from the "seed" crystals formed in the openings. The shape and crystal structure are then largely determined by the spatial confinement of the patterns and the surface energies of the various facets. For a small opening, such as a nanohole, SAE is realized by nucleation and growth under the standard vapor-solid (VS) growth mode. A nucleation-based model shows that hexagonal nucleus along the ⟨111⟩ direction has the smallest Gibbs free energy,[48] thereby explaining the preferred growth direction. For III–V semiconductors, {111} planes are polar and can be divided into (111)B and (111)A.[38] During SAE, GaN and InP grow along the ⟨111⟩A polar direction, while other compounds grow along the ⟨111⟩B direction.[49] The nucleus determines the crystal structure and the growth direction.[50] For InP, thermodynamic calculations show that the nucleus with wurtzite (WZ)

phase along the ⟨111⟩A directions is the most energetically favorable, while the nucleus along other directions (e.g., ⟨111⟩B and ⟨100⟩) has a larger energy barrier and results in a zinc blende (ZB) stacking sequence.[51,52] The control of WZ vs ZB crystal phases can be tuned by using the appropriate growth conditions.[53] Normally, SAE of nanowires is limited by the mass flow, where the adatoms diffuse from the mask region and sidewalls to the growth front.[54] Since the adatom diffusion rate relies on the sticking coefficient on the mask, growth methods, growth conditions, and the designed pattern, the growth behavior could vary in different situations. For instance, shadowing effect, where the scattered adatoms from the mask are affected by the ordered nanowire array, leads to the transformation of the nanowire crystal phase from WZ to ZB with increasing pitch distance.[55] Both radial and axial growth happen simultaneously, and their growth rate is tunable by growth conditions, which are utilized to grow axial and lateral heterostructures. Sometimes, optimal filling-up and growth conditions do not overlap, which causes difficulties in growth, especially for the III-Sb nanostructures.[11]

For large-size openings, the traditional layer-by-layer growth mode may not be valid, and the growth largely relies on the geometry and direction of the openings and the crystal structure of the underlying substrate. Multinucleation events could occur that might lead to antiphase domain formation[56] or not a fully flat surface.[48,57] The shape of III–V nanostructure is mostly determined by minimization of the total surface energy. Wulff construction can be applied to predict the shape of the nanostructure. Since SAE is normally performed at nonequilibrium conditions, Sun *et al.*[58] and Leung *et al.*[59] developed a kinetic Wulff plot to explain the morphology evolution of GaN on substrates by using the measured facet growth rate to replace the surface energy. Taking the dynamics (e.g., deposition, diffusion, incorporation, and desorption rate) into consideration, phase-field simulation is also used to model the shape evolution and applied to explain the 3D morphology of GaN on the ring-shaped pattern[60] as well as the evolution of GaAs nanomembranes.[61]

The well-accepted VS growth mechanism during SAE can be switched to the well-developed VLS mode when the growth condition is favorable for self-catalyzed growth, such as low V/III ratios,[62] small nanowire diameters,[63] and the intentional use of metal-seeded SAE.[64]

III. SAE OF VERTICAL NANOWIRES

In Sec. IIIA–D, we review the growth of vertical nanowires, including SAE, SA-VLS, formation of heterostructures, and growth on Si substrates.

A. III–V nanowires

The family of III–V semiconductors contains a variety of materials with different properties and surface energies. Consequently, the progress of SA-grown III-V nanowires differs from one compound to another. Direct growth of III-V binary and ternary compound nanowire arrays via SAE is summarized in Fig. 2.

III-N nanowire arrays, especially for a GaN-based materials system, is well developed thanks to its great potential in optoelectronic applications. Due to the large lattice and thermal mismatch between GaN and the substrate (sapphire or silicon), suppressing the defect density in GaN film is quite challenging. However, taking advantages of the nanowire size and geometry, under the right conditions, dislocation-type defects can be pinned at the interface, and dislocation threading along the nanowire can be avoided. In 2013, Mandl *et al.*[65] reviewed the progress of GaN nanowire arrays. The growth direction of GaN nanowires can be tuned to along either a Ga-polar [0001] or an N-polar [000-1] direction via pregrowth treatment or growth condition adjustment.[66] SAE of GaN nanowires was first reported by Hersee *et al.*[67] via a pulsed growth mode. Group III and V precursors were alternately injected into the reactor in a similar fashion as atomic layer deposition. They found that continuous growth mode leads to lateral 2D growth at a high V/III ratio. A continuous mode was thus proposed by Choi *et al.*[68] using ultra-low precursor flow rate and low V/III ratio conditions, resulting in nanowires as small as 50 nm in diameter. However, this method required high precision in mask preparation because the nanowire morphology was largely affected by the size of the openings, and larger diameter openings (400 nm) led to lateral expansion.[68] A method combining the advantages of pulsed and continuous mode was proposed by Lin *et al.*,[69] where only NH_3 was pulsed during the growth. This approach was simpler than the standard pulsed mode and more tolerant to the mask opening size. The nanowires show better optical properties, with strong suppression of yellow luminescence. Kamimura *et al.*[70] reported the growth of N-polar InN nanowires using molybdenum mask on sapphire (0001) substrates by plasma-assisted MBE. They found that higher InN selectivity could be achieved under In-rich conditions thanks to improved indium adatom diffusion length. Zeghouane *et al.*[71] reported highly uniform InN nanowire arrays grown on Ga-polar GaN/sapphire using hydride vapor-phase epitaxy, as shown in Fig. 2(b). They found that growth conditions (temperature and NH_3 partial pressure) and duration of growth could change the nanowire morphology from a pointed top (r-plane and m-plane sidewall) to a flat top (c-plane and a/m-plane) due to the effect of both mass transport and surface kinetics.[71]

SAE of III-P nanowire arrays is quite specific in terms of polarity preference and crystal phase purification. InP nanowire array was pioneered by Mohan *et al.*[4] along the ⟨111⟩A polar direction. Gao *et al.*[53] optimized the growth conditions to achieve a pure WZ phase from the first epitaxial layer demonstrated under lower V/III ratio and higher temperature [see Fig. 2(d)]. The pure crystal quality largely enhanced its internal quantum efficiency (IQE) and showed great potential in lasing applications. Recently, Staudinger *et al.*[56] achieved WZ InP pillar with area over 100 μm^2 via a careful pattern design and intentional lateral overgrowth. In comparison, advances in the SAE of GaP nanowire array are quite limited. Only recently in 2019, the first SAE of GaP was report in Choi *et al.*,[72] without too many details [see Fig. 2(c)].

SAE of III-As nanowire arrays are well developed by different research groups, achieving highly ordered nanowire arrays, surface passivation, and doping[3,73–76] [see Fig. 2(e)]. Despite the enormous growth attempts, crystal purity of III-As nanowires is still challenging, showing mainly mixed ZB and WZ phase. Shapiro *et al.*[77] pointed out that stacking fault formation in GaAs is related to the critical nucleus size. Theoretically, the energy difference between the WZ and ZB nuclei drops as the size becomes larger. Increasing the growth temperature leads to a larger nucleus size, thus suppressing the twin formation density. The existence of stacking faults also increases the lateral growth rate, resulting in GaAs nanowires with a much larger diameter than designed. Replacing the precursor from trimethylgalium to triethylgallium allows growth of GaAs nanowires at a lower temperature and, thus, lower radial overgrowth.[78] In terms of InAs nanowire array,

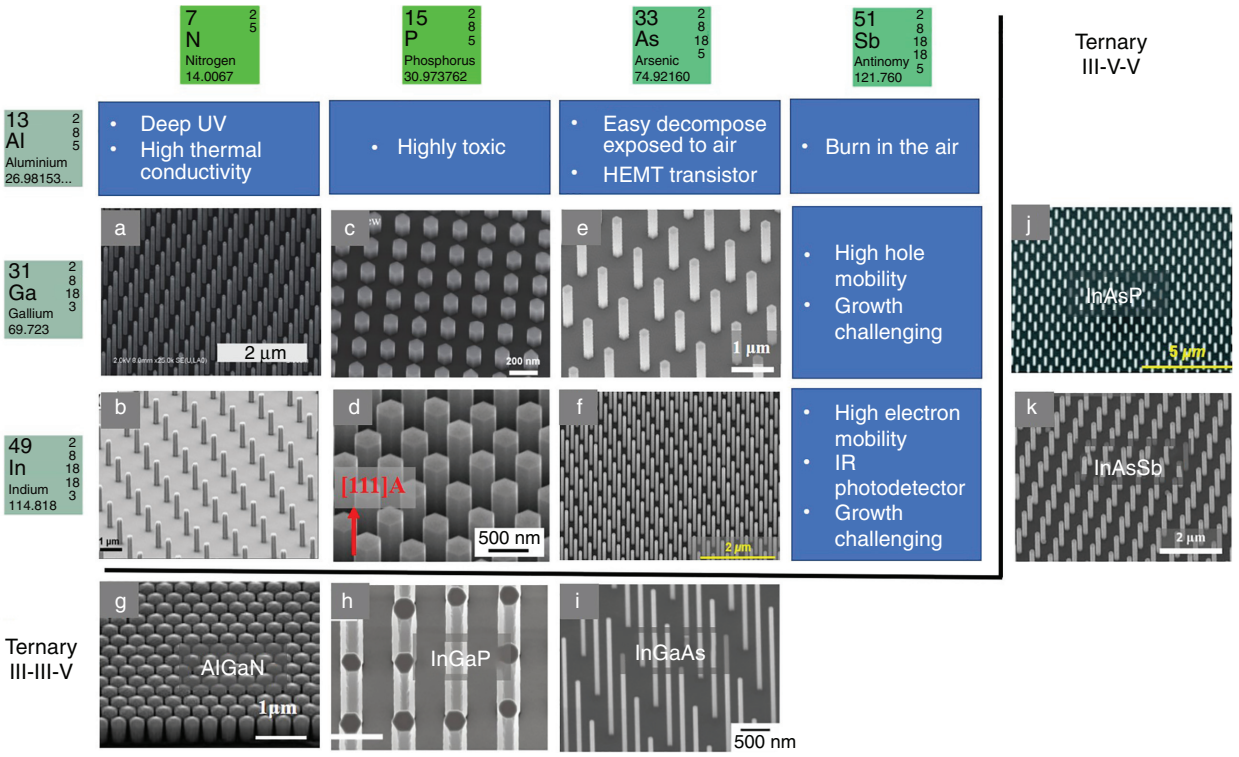

FIG. 2. Examples of various vertical III–V nanowires grown via SAE method. (a) GaN. Reproduced with permission from Lin *et al.*, Adv. Funct. Mater. **24**, 3162 (2014). Copyright 2014 Wiley-VCH.[69] (b) InN. Reproduced with permission from Zeghouane *et al.*, Cryst. Growth Des. **20**, 2232 (2020). Copyright 2020 American Chemical Society.[71] (c) GaP. Reproduced with permission from Choi *et al.*, 2019 Compound Semiconductor Week, Nara, Japan, 19–23 May 2019. Copyright 2019 IEEE.[72] (d) InP. Reproduced with permission from Gao *et al.*, Nano Lett. **14**, 5206 (2014). Copyright 2014 American Chemical Society.[53] (e) GaAs. Reproduced with permission from Bassett *et al.*, Appl. Phys. Lett. **106**, 133102 (2015). Copyright 2015 American Institute of Physics.[73] (f) InAs. Reproduced with permission from Ren *et al.*, Nano Lett. **18**, 7901 (2018). Copyright 2018 American Chemical Society.[81] (g) AlGaN. Reproduced with permission from Liu *et al.*, Opt. Express **25**, 30494 (2017). Copyright 2017 OSA Publishing.[82] (h) InGaP. Reproduced with permission from Berg *et al.*, Nano Res. **10**, 672 (2017). Copyright 2017 Springer Science+Business Media.[83] (i) InGaAs. Reproduced with permission from Sato *et al.*, J. Cryst. Growth **310**, 5111 (2008). Copyright 2008 Elsevier.[84] (j) InAsP. Reproduced with permission from Ren *et al.*, Nanoscale **9**, 8220 (2017). Copyright 2017 Royal Society of Chemistry.[85] (k) InAsSb. Reproduced with permission from Farrell *et al.*, Nano Lett. **15**, 6614 (2015). Copyright 2015 American Chemical Society.[86]

Tomioka *et al.*[79] reported diameter and height evolution of InAs nanowires with growth temperature and V/III ratio and demonstrated the first InAs nanowire arrays with a high-aspect ratio. In general, higher (lower) growth temperature and larger (smaller) V/III ratio are favorable for WZ (ZB) phase formation.[80] However, both phases occur simultaneously with planar defects. The polytypic behavior is linked to InAs (111)B surface reconstruction, where (1×1) reconstruction leads to the planar defect nucleation and tends to occur at lower As partial pressure and higher growth temperature.

III-Sb nanowires show the largest carrier mobility but are the most difficult to grow via either VLS or SAE. Only a small growth window exists, and the nucleation conditions can differ from the growth conditions. Nanowires based on Al-V binary semiconductor are also not well studied.

Extending binary III–V compound to ternary alloy allows continuous tuning of the bandgap, lattice constant as well as band alignment. For instance, the bandgap is adjustable from UV to mid-infrared (IR), which broadens the field of applications. For deep UV light source applications, Al-rich AlGaN nanowires are receiving increasing interest. Liu *et al.*[82] first demonstrated SAE of AlGaN nanowire arrays [see Fig. 2(g)] with nearly the entire compositional range. Moreover, an Al-rich AlGaN shell was spontaneously formed, suppressing the nonradiative surface recombination and thus enhancing the IQE up to 45%. By controlling nanowire coalescence, semipolar AlGaN quasi-3D film structures were grown successfully without dislocations induced by either lattice mismatch and misoriented nanowire.[87] The coalescence of nanowires into a quasi-continuous film of AlGaN led to the demonstration of UV light-emitting diodes (LEDs), with excellent electrical and optical performance.

For the visible LEDs, InGaN, InGaP, and GaAsP are promising. However, reports on the SAE of these ternary nanowire arrays are quite limited. To avoid the large strain-induced deterioration of crystal quality and quantum-confined Stark effect in the GaN/InGaN quantum well (QW) nanowire system, GaN nanowire matrix was replaced by a low-In-content InGaN nanopillar array to minimize the strain effect.[88] Taking advantage of the relaxed lattice constant, efficient QW emission was successfully shifted from the blue to green and even to the red region of the spectrum. SAE of GaAsP has not been reported yet. For InGaP nanowires [see Fig. 2(h)], they suffer from competing behaviors of the binary InP and GaP, which tend to grow along

opposite polarity.[83] Increasing Ga content turned crystal growth from nanowire to islands. Moreover, indium content distribution was nonuniform and increased from bottom to tip of the nanowires.

For applications in the near-IR range, InGaAs, GaAsN, and InAsP ternary nanowire arrays are suitable. Among these compounds, InGaAs nanowires have been extensively studied[84,89–91] [see Fig. 2(i)]. Composition control is one important factor during the growth of ternary nanowires. In general, In content in the nanowire (solid phase) is larger than that in the vapor phase. Due to the large difference in adatom diffusion length between In and Ga, the composition can vary along both the nanowire length and its cross section. Furthermore, the composition depends on the nanowire pitch and growth temperature. These differences lead to different optimized growth conditions for Ga-rich and In-rich InGaAs nanowire arrays. In terms of crystal structure, phase purity in InGaAs has not been reported, and the crystal structure gradually transforms from polytypic WZ to twinned ZB structure with increasing Ga content.[92] The surface of InGaAs contains a high density of nonradiative recombination centers, and *in situ* passivation with the growth of a lattice-matched InAlAs shell can largely improve its optical quality.[93] For InP-based ternary nanowire arrays, SAE becomes even more challenging due to the opposite polarity behavior between As- and P-based materials. InAsP nanowire arrays have been reported to have a similar growth behavior as InAs and prefer to grow along the ⟨111⟩B direction. Therefore, the growth of a thin InAs layer prior to nanowire growth is vital for InAsP nanowires [see Fig. 2(j)], since it can tune the preferred polarity from (111)A to (111)B.[85] SAE growth of dilute nitride (GaAsN) nanowire arrays has so far not been reported.

For the mid-IR applications, III-Sb ternary compounds are of interest thanks to their smallest bandgap among III–V semiconductors. However, the development of III-Sb–related nanowires is restricted by the narrow growth window and large lateral growth rate. Farrell *et al.*[86] demonstrated highly uniform InAsSb nanowire array on InAs substrate, with Sb content up to 15% [see Fig. 2(k)]. The incorporation of Sb tuned the crystal structure to a polytype ZB phase, but further increase in the Sb content led to growth failure. After Al_2O_3 passivation, the optical emission intensity of InAsSb nanowire array was enhanced 50 times, making it a good candidate for mid-IR photodetection.[94] Mitchell *et al.*[95] reported SAE of InAsSb nanowires on Si but with a much lower uniformity and poorer control of their dimensions. Later, they developed a kinetic method to explain the Sb-induced shape evolution.[96] In their model, the evolution of nanowire length and diameter was explained by the difference in In adatom concentration on the sidewall and top of the nanowire.

In conclusion, the development of ternary nanowire arrays is much slower than their binary counterparts. The competing of elements with different chemical properties complicates the growth behavior. In addition, inhomogeneity in composition is another major issue.[83] Moreover, simultaneous axial and radial growths occur on the nanowire arrays. Facet-dependent phase segregation exists, forming either a core/shell structure[82] or phase segregation along different crystal orientations.[95]

B. Selective area vapor-liquid-solid

SAE relies on the growth rate difference between various facets, which can pose a challenge for the optimization process. To add another degree of tunability in the growth, a metal droplet can be introduced into the patterned hole to allow growth to occur under the more matured VLS growth mechanism within a predefined array. This so-called SA-VLS method is divided into two groups depending on the choice of catalyst: self-catalysts (e.g., Ga and In) and foreign metal (e.g., Au).

Self-catalyzed nanowire avoids potential contamination caused by foreign metals and is thus preferred for the integration of III–V nanowires on Si substrates. For example, highly uniform GaAs [Fig. 3(a)],[97–100] InAs [Fig. 3(b)],[101] GaP [Fig. 3(c)],[21] GaAsP [Fig. 3(d)],[24] GaAsSb [Fig. 3(e)],[102] and InAsSb[103] nanowire arrays have been grown on silicon substrates using this technique. Meanwhile, self-catalyzed nanowire arrays, such as InP, have also been realized on III–V substrates [Fig. 3(f)].[63] During self-catalyzed SAE growth, the growth mode can be tuned from VLS to VS using the V/III ratio or hole opening diameter,[63,104] which increases the feasibility in controlling the crystal structure and heterostructure formation.

Compared with self-catalyzed growth, the advantages of foreign metal (e.g., Au)–assisted SA-VLS growth is that Au-seeded III–V nanowire growth is more mature and well understood. To date, much work has been done to grow arsenide nanowires [e.g., InAs in [Fig. 3(g)],[105] phosphide nanowires [e.g., WZ GaP in Fig. 3(h)],[106] and antimonide nanowires [e.g., GaSb in (Fig. 3(i)][107] by SA-VLS using Au as a catalyst. It is worth noticing that this growth technique can be used to achieve direct bandgap WZ GaP nanowire array through crystal engineering [Fig. 3(h)][106] and switching between axial and radial growth of InP nanowires by changing the growth parameters.[108] It also can be used to grow dual-type nanowire arrays (GaAs and InP) on the same substrate to offer increased light trapping compared with single-type array [Fig. 3(j)].[109]

Similar to traditional VLS nanowires, SA-VLS nanowires sometimes exhibit a tapered morphology due to the limitation of the migration distance of adatoms. The migration distance of adatoms along the nanowire side facets is related to the diameter of the seed particle and growth temperature. The migration distance can be increased by reducing the seed diameter or increasing the growth temperature, thereby eliminating the tapering.[110,111] The size, density, and spacing of the openings also have an important effect on the growth of SA-VLS nanowires.[98,101,112] For instance, the small-sized openings can reduce the nucleation yield of nanowires, while large openings may lead to multiple nanowire growth in the same hole, which can subsequently merge.[101] In addition, to understand the influence of the size, density, and pitch of the openings on the mask on nanowire growth rate, the shadow effect has been proposed.[113,114] Recent work showed that the shadow effect can be used to control and even tailor the crystal phase in III–V nanowires grown by SA-VLS.[55]

C. Silicon integration

Monolithic integration of high-gain III–V materials on Si is long sought after for high-performance electronic and optoelectronic devices. Heteroepitaxy of one-dimensional III–V nanowires is a possible way to achieve these goals because it overcomes the problem caused by the lattice and thermal expansion mismatch. Tomioka *et al.*[115] and Tomioka and Fukui[116] reviewed the growth of III–V nanowires on Si (111) substrates. For heteroepitaxial growth of III–V nanowires on Si substrates, uniform vertically aligned III–V nanowire growth and improvement in crystal quality are two main issues of concern. Polarity is a vital factor that limits the vertical growth of III–V

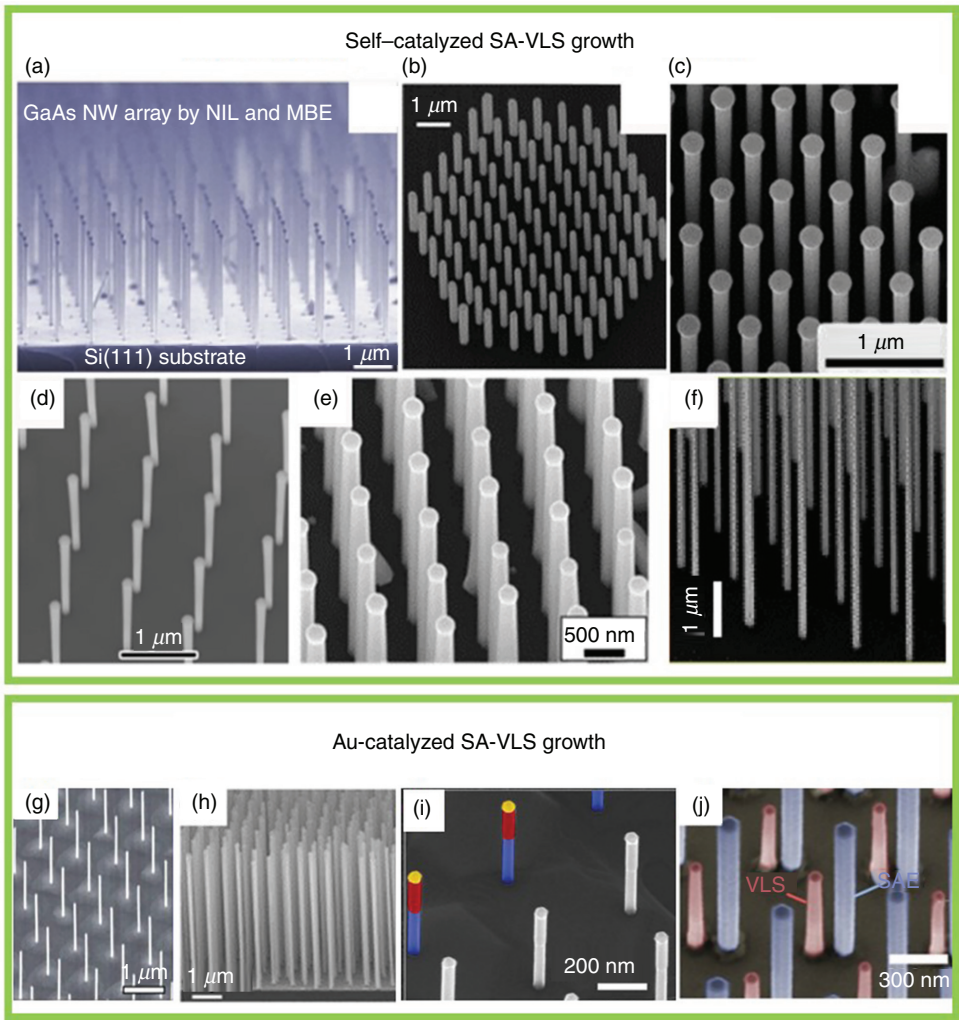

FIG. 3. III–V binary and ternary nanowires grown by SA-VLS method. (a)–(e) Self-catalyzed nanowire arrays on Si substrates. (a) GaAs. Reproduced with permission from Munshi *et al.*, Nano Lett. **14**, 960 (2014). Copyright 2014 American Chemical Society.[100] (b) InAs. Reproduced with permission from Mandl *et al.*, J. Cryst. Growth **334**, 51 (2011). Copyright 2011 Elsevier.[101] (c) GaP. Reproduced with permission from Oehler *et al.*, Nano Lett. **18**, 701 (2018). Copyright 2018 American Chemical Society.[21] (d) GaAsP. Reproduced with permission from Zhang *et al.*, Nano Lett. **14**, 4542 (2014). Copyright 2014 American Chemical Society.[24] (e) GaAsSb. Reproduced with permission from Ren *et al.*, Nano Lett. **16**, 1201 (2016). Copyright 2016 American Chemical Society.[102] (f) Pure WZ InP nanowires grown on (111)A InP substrate. Reproduced with permission from Gao *et al.*, Nano Lett. **16**, 4361 (2016). Copyright 2016 American Chemical Society.[63] (g) Au-catalyzed growth of InAs. Reproduced with permission from Jensen *et al.*, Nano Lett. **4**, 1961 (2004). Copyright 2004 American Chemical Society.[105] (h) Pure WZ GaP nanowires. Reproduced with permission from Assali *et al.*, Nano Lett. **13**, 1559 (2013). Copyright 2013 American Chemical Society.[106] (i) InAs/GaSb axial junction nanowire arrays. Reproduced with permission from Svensson *et al.*, Nano Lett. B, **15**, 7898 (2015). Copyright 2015 American Chemical Society.[107] (j) Combining SAE and VLS growth to implement different types of nanowires on the same substrate. Reproduced with permission from Kakko *et al.*, Nano Lett. **15**, 1679 (2015). Copyright 2015 American Chemical Society.[109] NIL, nanoimprint lithography; NW, nanowire.

nanowire arrays. The nonpolar nature of Si substrates easily leads to random nanowire growth since III–V nanowires prefer to grow along the ⟨111⟩B direction [as illustrated in Fig. 4(a)]. Surface treatment to turn the Si surface from nonpolar to either A or B polar is critical for vertical growth. Tomioka pioneered the SAE of III–V nanowires on Si substrates under a flow rate–modulated epitaxy mode.[115,117–119] In short, the Si (111) substrate was treated with alternating III or V precursor supply at low temperatures (∼400 °C) to form a (111)B-like polar surface before nanowire growth,[118] leading to 100% vertical yield of III-As nanowires. Later, some studies indicated that such a surface treatment process was not necessary,[120,121] and uniform GaAs and InGaAs nanowire arrays could be achieved via direct tuning of the precursor flow rates at higher growth temperatures [see Fig. 4(b)]. In these scenarios, surface treatment was realized by Ga incorporation. Liu *et al.*[122] demonstrated that the introduction of Ga at the nucleation stage can induce and stabilize the B polarity on a nonpolar Si (111) surface and thus facilitate the vertical growth of InAs nanowires.[121] Instead, the yield of vertical InAs nanowire array via MBE method is independent of the prewetting conditions at the nucleation stage.[123] To circumvent the nonpolar nature of Si substrates, growth of III–V

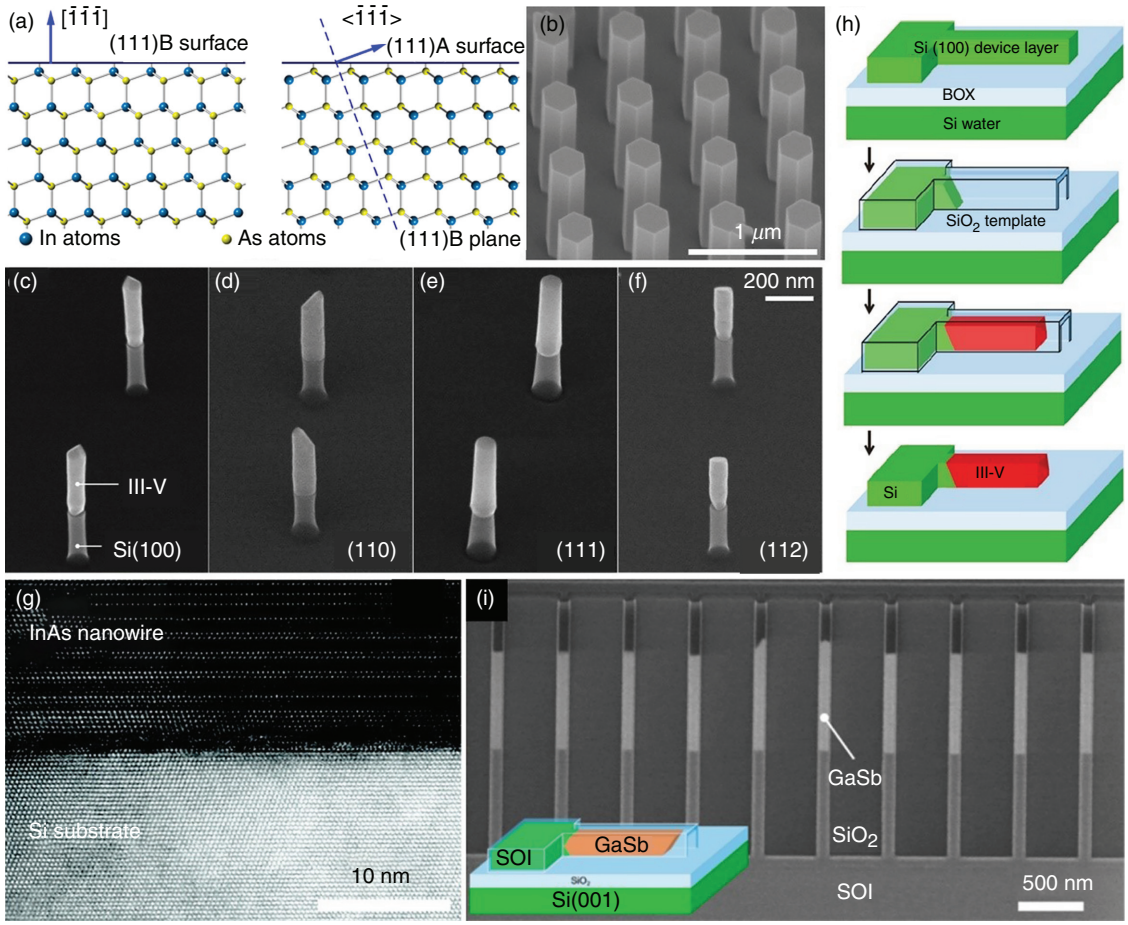

FIG. 4. SAE of III–V nanowires for silicon integration. (a) Schematic of III–V compound semiconductors with (111)B surface (group V–terminated surface) and (111)A surface (group III–terminated surface). (b) SEM image of GaAs nanowires grown on Si (111) substrate. Reproduced with permission from Yao *et al.*, ACS Nano **10**, 2424 (2016). Copyright 2016 American Chemical Society.[120] (c)–(f) SEM images of InAs nanowires grown on [100]-, [110]-, [111]-, and [112]-oriented Si nanowires, respectively. Reproduced with permission from Borg *et al.*, Nano Lett. **14**, 1914 (2014). Copyright 2014 American Chemical Society.[14] (g) HRTEM image of an InAs nanowire grown on Si (111) substrates. Reproduced with permission from Tomioka *et al.*, Nano Lett. **8**, 3475 (2008). Copyright 2008 American Chemical Society.[118] (h) Schematic showing the process flow of TASE technique. Reproduced with permission from Schmid *et al.*, Appl. Phys. Lett. **106**, 233101 (2015). Copyright 2015 American Institute of Physics.[15] The images from top to bottom are, respectively, shape definition, nanotube formation by oxide deposition and Si back-etching, selective growth, and oxide removal. (i) SEM image of GaSb nanostructures grown by TASE technique. Reproduced with permission from Borg *et al.*, ACS Nano **11**, 2554 (2017). Copyright 2017 American Chemical Society.[19]

nanowires in a nanotube template is also an effective method to achieve vertically aligned nanowire arrays.[14,124] This template approach is fully compatible with CMOS processing and avoids the lattice-mismatch–induced defect formation, thus opening up another approach for monolithic integration of III–V materials on Si. Taking advantage of this technique, most III–V nanowire and nanowire heterostructure arrays can be grown on different Si substrates of various orientations [see Figs. 4(c)–4(f)] and even on amorphous Si substrates without defect formation.[14,124,125] In short, although much progress has been made to date in the growth of vertically aligned III-As nanowire arrays, direct epitaxy of III-N,[126,127] III-Sb,[128] and III-P nanowire arrays on Si substrates remains a challenge.

Successful growth of vertical III–V nanowire arrays on Si substrates is a first step toward the merging of electronic and optoelectronic devices. Maintaining high-quality nanowires is also necessary to guarantee device performance. For example, stacking faults and misfit dislocations can act as carrier trapping centers and degrade the performance and reliability of III–V nanowire/Si tandem solar cells.[129] Within the SAE approach, many researchers have reported the difficulty in improving the crystal quality of III–V semiconductor nanowires by only changing the growth temperatures or V/III ratios.[115,117–120] Instead, III–V semiconductor nanowires grown under the VLS mechanism have achieved great success in phase purity.[130–132] Both foreign metal–catalyzed or self-catalyzed SAE growth methods have been applied to realize pure phase III–V semiconductor nanowire arrays,[107,128] such as Ga-catalyzed ZB defect-free GaAsSb nanowire arrays. Another concern is defects occurring at the heterointerface. In 2018, Kunert *et al.*[133] critically reviewed the mechanisms of defect nucleation in monolithic III–V heteroepitaxy on Si (100) substrates. Lattice-mismatch–induced defects can be trapped by the mask under

certain conditions, and hence, threading dislocations, which are commonly observed in film growth, can be prevented in propagating inside the III–V nanowires grown on Si substrates.[115,117–120] Instead, periodic misfit dislocations are only formed at the heterointerface [see Fig. 4(g)].

In addition to vertical nanowire growth along the ⟨111⟩ direction, conformal epitaxy introduces a patterned oxide layer to restrict vertical growth and force the crystal to grow sideways on {100}-oriented Si substrates.[40] Lateral overgrowth that occurs on polycrystal seeds largely reduces the defect density, such that high-quality GaAs,[134] InP,[135] and GaN[136] films can be grown on Si. Moreover, conformal epitaxy has the advantage of lateral doping and heterostructure formation control. Schmid *et al.*[15] and Borg *et al.*[19] modified this method and developed a TASE technique to allow epitaxy of III–V nanostructures on SOI substrate, which has the advantage of forming complex and versatile III–V nanostructures, such as 3D stacked nanowires, nanowire crosses, and the cointegration of different III–V materials [see Figs. 4(h) and 4(i)]. No matter which technique is applied, the purpose of integrating III–V materials onto Si chips is to provide a light source for Si photonics applications or further enhance the speed of Si electronic devices. Based on the SAE principle, room temperature InP nanowire laser array has been demonstrated on Si (100) substrates.[137]

D. Heterojunctions

Heterostructure formation is one advantage of III–V nanowires, which is widely applied to modify the nanowire properties and advance the nanowire arrays for device applications, as illustrated in Fig. 5. Generally, heterostructure formation can be divided into the following aspects: (1) surface passivation to suppress the nonradiative recombination centers, such as core/shell structure; (2) addition of new functionality to the nanowire, such as QDs, and QWs; (3) uniform doping to achieve excellent *p-i-n* structure; and (4) band structure engineering.

III-As nanowires have a fast surface recombination rate and need surface passivation. For surface passivation via core/shell structure formation, lattice matching is important to avoid dislocation formation.

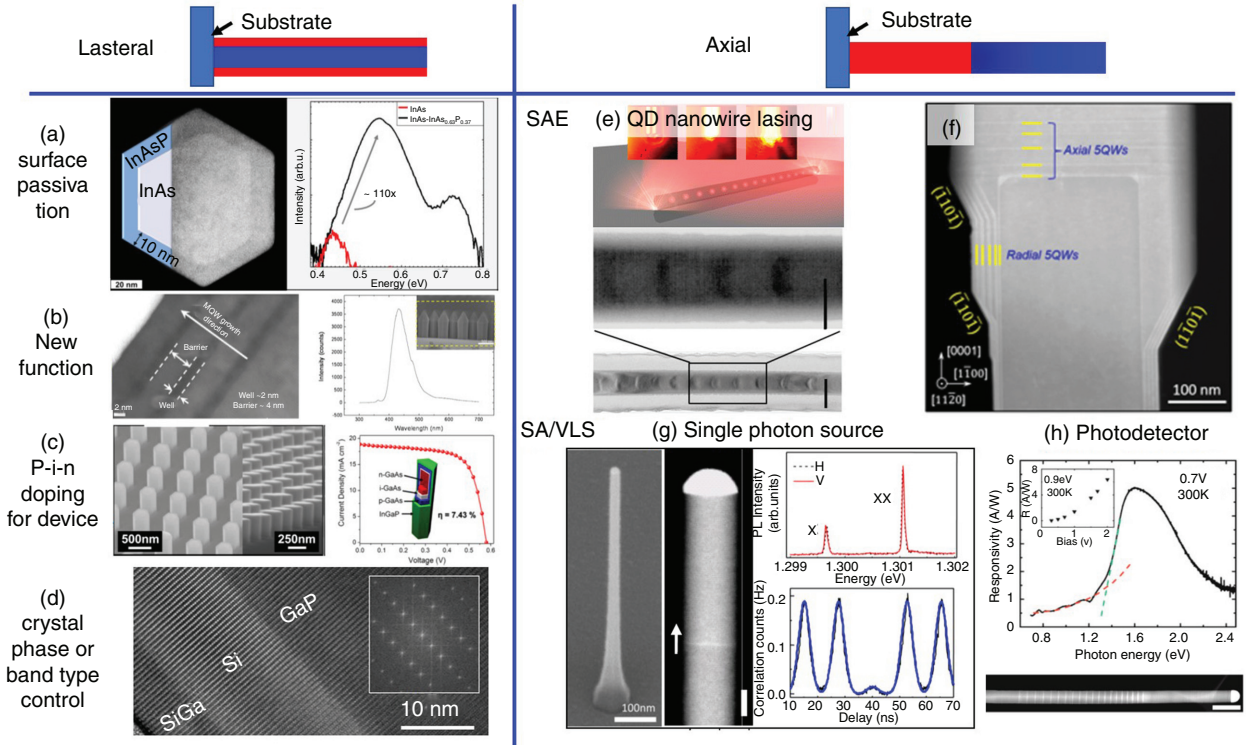

FIG. 5. Nanowire array-based heterostructure formation laterally (a–d) and axially (e–i). SA-grown radial heterostructure with different purposes. (a) Surface passivation in InAs/InAsP core/shell nanowire. Reproduced with permission from Treu *et al.*, Nano Lett. **13**, 6070 (2013). Copyright 2013 American Chemical Society.[142] (b) InGaN QW formation using the large lateral surface for LED applications. Reproduced with permission from Yeh *et al.*, Nano Lett. **12**, 3257 (2012). Copyright 2012 American Chemical Society.[144] (c) *p-i-n* junction in GaAs nanowire for device applications. Reproduced with permission from Mariani *et al.*, Nano Lett. **13**, 1632 (2013). Copyright 2013 American Chemical Society.[145] (d) Direct bandgap SiGe formation using WZ GaP nanowire array as a template. Reproduced with permission from Hauge *et al.*, Nano Lett. **17**, 85 (2017). Copyright 2017 American Chemical Society.[146] (e) SAE of GaAs/InGaAs multi-QD nanowire array for lasing applications. Reproduced with permission from Ho *et al.*, Nano Lett. **16**, 2845 (2016). Copyright 2016 American Chemical Society.[147] (f) Inhomogeneous growth of InGaAs QD in InP nanowires. Reproduced with permission from Yang *et al.*, ACS Nano **12**, 10374 (2018). Copyright 2018 American Chemical Society.[57] (g) Well-controlled axial InP/InAsP QD nanowire grown by SA-VLS for single-photon source applications. Reproduced with permission from Dalacu *et al.*, Nano Lett. **12**, 5919 (2012). Copyright 2012 American Chemical Society.[28] (h) InP/InAsP QD nanowire photodetector. Reproduced with permission from Karimi *et al.*, Nano Lett. **17**, 3356 (2017). Copyright 2017 American Chemical Society.[32] arb., arbitrary; A/W, photocurrent/incident optical power.

GaAs nanowires can be well passivated by an InGaP[138] or AlGaAs shell.[25] For InGaAs nanowire array, InP shell is a good choice thanks to its superior passivation effect and lattice matched to $In_{0.49}Ga_{0.51}As$.[139] Moreover, for different InGaAs compositions, Treu *et al.*[93] demonstrated that an appropriately chosen InAlAs shell lattice matched to that InGaAs composition can be successfully grown for passivation. For III-N and III-P nanowires with good optical performance, surface passivation can be applied to further increase their quantum efficiency.[140,141] Lattice-mismatched shell can also be grown as an *in situ* approach to realize strain engineering, such as InAs/InAsP[142] [see Fig. 5(a)] and GaAs/GaNAs core shell[143] nanowires. However, careful attention should be paid since strain could introduce dislocations or nanowire bending.

Using the nanowires as template, QWs and QDs can be easily formed laterally or axially on the nanowire, allowing the tunability of the bandgap. The core/shell type heterostructure makes full use of the large surface and nonpolar nature of the sidewalls, such as {1–100} and {11–20}. In GaN-based nanowires, the nonpolar or semipolar nature of the nanowire sidewalls can eliminate the piezoelectric fields and enhance the emission efficiency over the traditional film-based structure. Consequently, SA grown GaN/InGaN multi-QW nanorod arrays have been extensively explored by different research groups for LED applications,[144,148–153] as illustrated in Fig. 5(b). Cross-sectional TEM shows that InGaN QWs could only be formed on the nonpolar planes.[144] However, the growth rate and composition of QWs depend on both the crystal facet[153] and the number of QWs,[154] which can lead to an inhomogeneous emission. Normally, it is hard to achieve ohmic contact on p-type GaN nanorods, but this difficulty can be overcome by forming an Al tunnel junction inside the quantum barrier.[155] The introduction of tunnel junction eliminates the use of Mg-doped p-GaN and obtains a higher hole injection efficiency. For the emission in the near-infrared region, InP/InGaAs QW nanowire arrays[57] can be used for light emission in the telecommunication wavelength range.[156,157] During lateral heterostructure formation, lattice mismatch is still an issue, restricting its application. In addition to dislocation formation, strain can bend the nanowire and deteriorate morphology. For instance, it is still challenging to form In-rich InGaN QWs for efficient green and yellow light LEDs.

Instead, axial QD can withstand more strain since it restricts the defects at the interface, making it suitable for LEDs and single-photon emitters. For instance, InGaN/GaN axial multi-QW nanorod LEDs are demonstrated by Nguyen *et al.*[158] In their work, they found that a p-type AlGaN blocking layer was necessary to prevent the electron overflow effects, and no efficiency droop was observed in their device for injection current densities up to 2200 A/cm^2. During QD formation via the SAE approach, complete suppression of lateral growth is desirable, since lateral overgrowth reduces the purity of QD. Pure axial GaAs/InGaAs QD nanowire arrays have been demonstrated, but indium content varies between these QDs.[159] Later, growth conditions were optimized to achieve uniform InGaAs multi-QDs (up to 200) in a single nanowire.[160] The homogeneity is beneficial for increasing the emission brightness and lasing applications[147,161] [see Fig. 5(e)]. In terms of InAs nanowire arrays, InAsSb QDs selectively grow on the {0001} and inclined {1101} facets.[162] For InP-based QD nanowire arrays, the effect of polarity difference make the incorporation of InGaAs[57] and InAsP,[163,164] QDs difficult. InGaAs [see Fig. 6(f)] and InAsP QDs grow both axially and radially. Moreover, these QDs deteriorate the morphological symmetry. Instead, using InAsP nanowire arrays along the [111]B direction as a template, pure axial InAs(Sb) QDs can be achieved.[23] Nanowire arrays grown using a VLS mechanism is a better option for pure axial QD growth thanks to well-accumulated growth knowledge.[22,28] Slightly tapered morphology is shown to increase light extraction efficiency in InP/InAsP QD nanowire arrays.[22] These highly controlled InP/InAsP QD nanowire arrays with high crystal quality was then quickly developed to fabricate bright single-photon sources with high purity and extraction efficiency[28,29] [see Fig. 5(g)]. Also, these multi-QD nanowire arrays are used for efficient room temperature infrared photodetection applications[32] [see Fig. 5(h)].

P-i-n junction formation is the basis for electrically operated device applications. Doping control is easier for SAE than VLS since it avoids the extra complication of dopant incorporation into the nanowire via a metal catalyst.[165] For GaAs,[145] InP,[33] and GaN[155] nanowires, both axial and radial *p-i-n* nanowire junctions can be fabricated. Together with QW/QD formation, *p-i-n* nanowire array junction has been widely used for solar cell, white light emission, and photodetector applications, as illustrated in Fig. 5(c).

Crystal phase engineering is widely applied in the III-P system where its ZB counterpart is indirect bandgap. Using WZ InP as a template, AlInP, GaP, and AlGaP shell with WZ phase have been grown for light emission in the visible range.[166–168] Moreover, this approach is further extended to group IV semiconductors, such as hexagonal SiGe shell on GaP [see Fig. 5(d)].[146] Recently, using pure WZ GaAs nanowire array as a template, lateral epitaxy of a thick layer of SiGe alloy and Ge allows controllable formation of direct bandgap SiGe alloy with efficient emission property in the near-infrared range.[169,170] Pure phase nanowire template is also used to transfer their high quality to the shell where direct growth of that phase is not viable, such as defect-free WZ InP/InAs core shell nanowire arrays.[171] For bandgap engineering, broken type II band alignment between InAs and GaSb is of great research interest. InAs/GaSb hybrid structure forms an inverted band alignment, i.e., the conduction band of InAs and the valence band of GaSb are aligned at the Fermi level. The inverted bandgap material is a natural candidate for topological insulators.[172] In addition, InAs/GaSb-based heterojunction is an ideal heterostructure for tunnel field effect transistors (TFETs) due to a broken band alignment and a narrow bandgap for both InAs and GaSb (0.36 and 0.73 eV, respectively).[173,174] A misfit dislocation–free GaSb shell with up to 40 nm in thickness has been grown on polycrystalline InAs nanowire arrays.[175] To further enhance its performance, Sb is introduced during the InAs core nanowire growth to form a defect-free ZB $InAs_{0.906}Sb_{0.094}$ nanowire template for GaSb shell growth.[176] Electrical measurements reveal the unintentional formation of n-type InAsSb core and p-type GaSb shell. Normal type II structure shows advantages in carrier separation. Alhodaib *et al.*[162] demonstrated InAs/InAsSb multi-QW nanowire arrays on silicon. Despite the type II band alignment, quantum confinement of carriers increases the radiative recombination rate and suppresses Auger recombination.

IV. ADVANCES IN NANOSHAPE ARRAYS AND NETWORKS

Despite the progress in nanowire research for two decades, there are still limitations with nanowires due to their inherent geometry. Other nanostructures with a variety of geometries beyond the

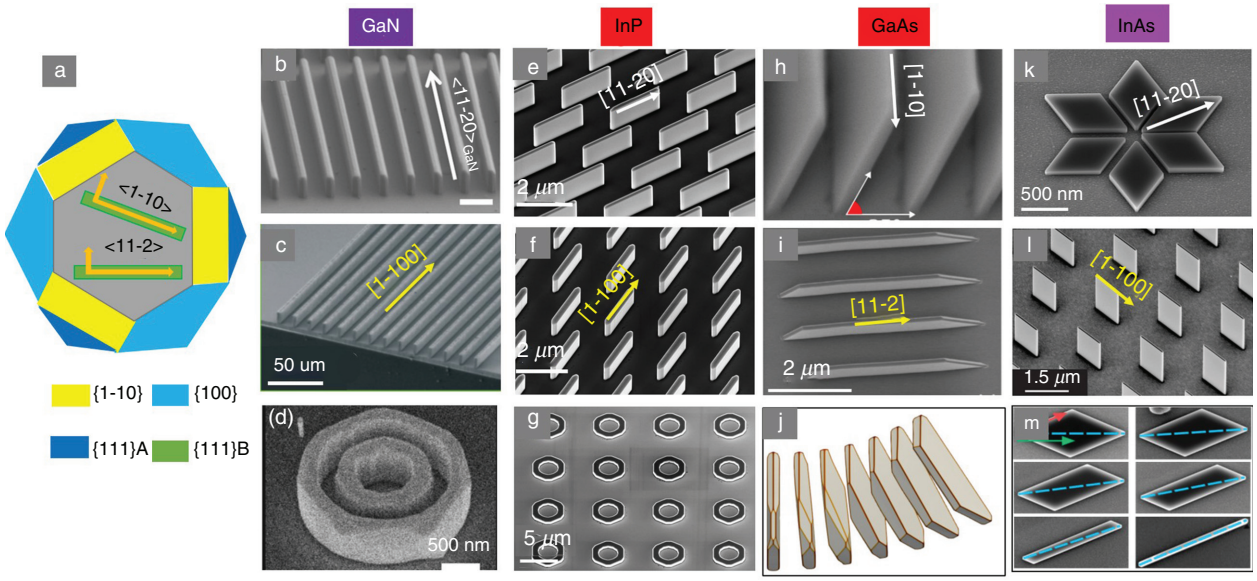

FIG. 6. Different growth behaviors of III–V nanoshapes. (a) Illustration of crystal orientation of the low-indexed facets on {111} substrate together with the commonly designed nano-slot orientations. (b)–(d) GaN and (e)–(g) InP nanosheets formed along both [11–2] and [1–10] directions, thus leading to the formation of an even microring-shaped array in an annular opening on the mask. (h)–(j) Formation of GaAs nanomembranes occurs only along the ⟨11–2⟩ direction, and all other crystal orientations lead to inclined nanomembrane growth. (k) Formation of vertical InAs nanodiamond structure and (l) nanomembrane array along the ⟨11–2⟩ and ⟨1–10⟩ directions. (m) The large radial growth rate of the {1–100} facet is the main driving force for the morphology evolution. Panels (b) and (c) are reproduced with permission from Yeh *et al.*, Appl. Phys. Lett. **100**, 033119 (2012). Copyright 2012 American Institute of Physics.[8] Panel (d) is reproduced with permission from Winnerl *et al.*, Nanoscale **11**, 4578 (2019). Copyright 2019 Royal Society of Chemistry.[178] Panels (e)–(g) are reproduced with permission from Wang *et al.*, ACS Nano **13**, 7261 (2019). Copyright 2019 American Chemical Society.[6] Panels (h) and (j) are reproduced with permission from Albani *et al.*, Phys. Rev. Mater. **2**, 093404 (2018). Copyright 2018 American Physical Society.[61] Panel (i) is reproduced with permission from Chi *et al.*, Nano Lett. **13**, 2506 (2013). Copyright 2013 American Chemical Society.[5] Panels (k)–(m) are reproduced with permission from Seidl *et al.*, Nano Lett. **19**, 4666 (2019). Copyright 2019 American Chemical Society.[9]

limitation of rod-like nanostructures are now developing very fast to meet the requirements of advanced device applications.

A. Nanoshape arrays

Instead of only forming nanowires, SAE can be used to grow nanostructures with different shapes and geometries simply by designing the appropriate patterns. From a crystallography perspective, nanosheet is the simplest morphology other than nanowire, which can be realized via patterning slots along certain crystallographic directions on the substrates [see Fig. 6(a)]. GaN fin arrays can be formed with slot direction along ⟨1–10⟩ and ⟨11–2⟩ on either GaN or sapphire substrates[8,177] [see Figs. 6(b)–6(d)]. This property is further applied to form different types of nanostructure networks.[178] Using GaN array as a template, Park *et al.*[179] demonstrated the growth of well-ordered In-rich InGaN nanoridge arrays. These fin-shaped InGaN nanostructures are nearly defect free despite the large lattice mismatch with GaN. The improved crystal quality leads to a much higher emission intensity than the planar or nanowire counterparts. On the other hand, vertical GaAs nanomembranes only form when the nanoslot is along the ⟨11–2⟩ direction.[5] When the nanoslot direction is aligned off ⟨11–2⟩, inclined nanomembranes are formed [see Figs. 6(h)–6(j)].[61] GaAs nanomembranes show a different growth mechanism from nanowires. GaAs nanomembranes are ZB and twin free, while the GaAs nanowires grown in the same run show a high density of stacking faults. Albani *et al.*[61] further developed the phase field simulation in an attempt to understand the growth behavior of these nanomembranes. They showed that the shape of GaAs nanomembranes grown from different oriented nanoslots was mainly determined by kinetics instead of minimization of surface energy. The same group further attempted to fabricate GaAs nanomembrane arrays on silicon substrate,[7,180] but more work is still required to gain full control of the geometry. Optical simulations and experiments show that GaAs nanomembranes contain more complex 2D asymmetric optical modes than their 1D nanowire counterparts.[181] To enhance their optical performance, defect-free GaAs nanomembranes based on core/shell[182] and QW structures[183] have been grown.

The research in GaAs nanomembranes opens up a new class of vertical nanostructures in other III–V semiconductors. Recently, InP and InAs nanoshape arrays have been demonstrated and proved to be even better than GaAs with a more symmetric shape.[6,9] InP nanostructures can exist with both {1–100} and {11–20} surfaces/facets. Other shapes, such as nanoring, nanomembrane, and nanodiamond arrays [Figs. 6(e)–6(g)], can be formed in the same run with pure WZ phase. Combining the pattern design and intentional lateral overgrowth, large-size WZ InP pillar arrays were achieved, with the size approaching 100 μm^2.[56] These pillars were then applied to demonstrate vertical nanopillar lasers, making use of the underlying SiO_x mask to reduce optical losses into the InP substrate.[184] Furthermore, various InP nanoshape arrays have been demonstrated on InP

substrate with different orientations.[48] The authors established a unified growth model for SAE of InP nanostructure arrays regardless of substrate orientation and geometry. Growth along ⟨111⟩A and ⟨111⟩B directions leads to the formation of WZ and ZB phases, respectively, forming a novel layered nanomembrane with type II band alignment. The morphology evolution of the InP nanoshape is controlled by the confinement effect of designed pattern and minimization of total surface energy. InAsP QWs have also been grown on these InP nanomembranes, revealing that the {11–20} surface allows uniform QW formation, while QW formation on the {1–100} surface is asymmetric. In comparison with InP, InAs stabilizes on the {11–20} surfaces due to the large lateral growth rate of the {1–100} facets at different growth temperatures, thus only forming thin nanosheets.[9] When the slot direction is away from ⟨11–2⟩ direction, the InAs nanostructures would evolve from nanosheet to diamond shaped [Figs. 6(k)–6(m)]. The large radial growth may be used to form InAs film. Despite the highly uniform morphology in InAs nanosheets, growth conditions can be further optimized to suppress defect formation. In general, surface energy plays a key role in the morphological evolution of III–V nanostructures. InP and GaN nanostructures are mainly bound by {1–100} and {11–20} facets, while the GaAs nanomembrane consists mostly of {1–10} facets and {113} facets. Differences in facet stability lead to the morphological differences in different III–V semiconductors.

B. Nanostructure networks

Nanostructure networks provide the basis for future quantum computing applications. Based on the network geometry, it can be divided into three types of architectures: inclined, vertical, and in-plane. Inclined nanowire networks, which provide different types of networks for growth studies and quantum science research, are well developed thanks to accumulated growth knowledge in nanowires and site control advantages of SAE. Wang *et al.*[185] first demonstrated the ability to tune InP nanowire growth direction between ⟨100⟩ and ⟨111⟩. InSb nanowire cross-network arrays were then reported soon after.[186] Using this method, InP/InSb[27] and InAs [see Fig. 7(a)][187] nanowire cross networks are demonstrated. This method relies critically on the ability to tune the growth direction and symmetry of the substrate. Dalacu *et al.*[188] further developed this method by forming InP ridges with {111}B sidewalls on InP{100} substrates, and then Au-seeded InAs nanowires are selectively grown on the patterned inclined {111}B sidewalls, thereby allowing the formation of highly ordered nanowire networks [see Fig. 7(b)]. The growth behavior at the interconnection points becomes complex due to a multinucleation process, which needs further exploration. The crystal phase and defect formation depend on the merging process and crystal orientation of the nanowire branches. For instance, when the cross is formed at the growth front of two WZ InAs nanowires, a ZB intersection is formed.[187,189] Furthermore, Gazibegovic *et al.*[26] managed to grow scalable InSb nanowire networks, crosses, and even loops by combining precisely site-controlled together with advanced metal epitaxy technique. After the formation of high-quality nanowire networks, epitaxial metal layers (e.g., Al, Sn, and Pb) were grown on the nanowire surface to form superconducting electrodes for quantum transport investigations.[190] These hybrid superconductor–semiconductor nanowires reveal Aharonov–Bohm and weak antilocalization effects, which pave the way for quantum devices. Indeed, even without droplet and inclined ridges, SAE of InP and InAs nanowire and nanofin networks can be formed using {100} substrates [see Fig. 7(c)],[48,191] making use of the two inclined ⟨111⟩A or ⟨111⟩B directions. However, the inclined network has to be transferred to another substrate for prototype device studies and, thus, is difficult for scalable device fabrication.

On the other hand, vertical networks are usually formed on nanomembranes grown on ⟨0001⟩/⟨111⟩-oriented substrates. InAs networks with low defect density were grown using free-standing GaAs nanomembranes as a template [see Fig. 7(d)] in quasi-1D quantum transport studies.[192] Using GaN and InP nanofins with different orientations as building blocks, triangular, hexagonal, and rectangle nanofin networks have been demonstrated [Fig. 7(f)].[178] Moreover, they can be used to form active waveguide arrays, such as InP microring with bus waveguide design for whispering gallery mode lasing applications. By promoting lateral growth, these ordered nanofins could form high-quality WZ InP micro-sized pillar arrays that cannot be achieved via direct growth [see Fig. 7(e)].[56] This provides a promising and scalable approach to form films with metastable phases. Compared with free-standing nanostructure networks, in-plane networks are much easier to fabricate. III–V network research is mostly focused on InAs and InSb thanks to their large spin–orbit interactions and, hence, the potential applications in spin-based quantum computing and topological quantum computing. For planar III–V network formation, industry-compatible {100}-oriented substrates are more suitable. Krizek *et al.*[193] investigated facet development of InAs as a function of mask alignment, as shown in Fig. 7(g). Based on strain relaxation using diluted GaAsSb, the improved interface quality in InAs led to strong spin–orbit coupling and phase coherence in the InAs network. Moreover, Vaitiekėnas *et al.*[10] realized high-quality InAs loops and branches grown on InP substrates. Impressively, Al contacts were also epitaxially grown on the InAs networks. Aseev *et al.*[12] optimized the growth of InAs [see Fig. 7(h)] and InSb [(see Fig. 7(i)] planar networks on InP{111}B substrates and proposed a selectivity map of InAs and GaAs networks. Depending on the growth behavior, they divided the growth parameter space into four regimes, which were parasitic III–V crystallites on the mask, droplets on the mask, ideal selective epitaxy, and no growth. Finally, they realize wafer-scale InAs cross-junction networks, which showed Aharonov−Bohm interference effect. The group also managed to overcome the growth challenges associated with InSb where the growth parameter window and nucleation condition do not overlap[194] by treating the nucleation and growth procedures separately.[11] These complex InSb nanowire networks showed high structural quality and ballistic transport in a 440-nm-long channel.

V. APPLICATIONS

The applications of III–V nanostructures can be realized using a single element of the nanostructure, arrays, or networks. The development of a single-nanostructure–based device is progressing rapidly with the promise of realizing miniaturized photonic/optoelectronic systems. A single-nanostructure–based device can be considered as the basic unit, which can be transferred to other substrates for complex device architecture design. For example, single, pure WZ SAE InP nanowires have been used for terahertz (THz) sensing by Peng and colleagues,[195,196] showing a high signal-to-noise ratio and polarization (due to the strong optical anisotropy in nanowire originating from its one-dimensional geometry). More recently, using the "nanoscale

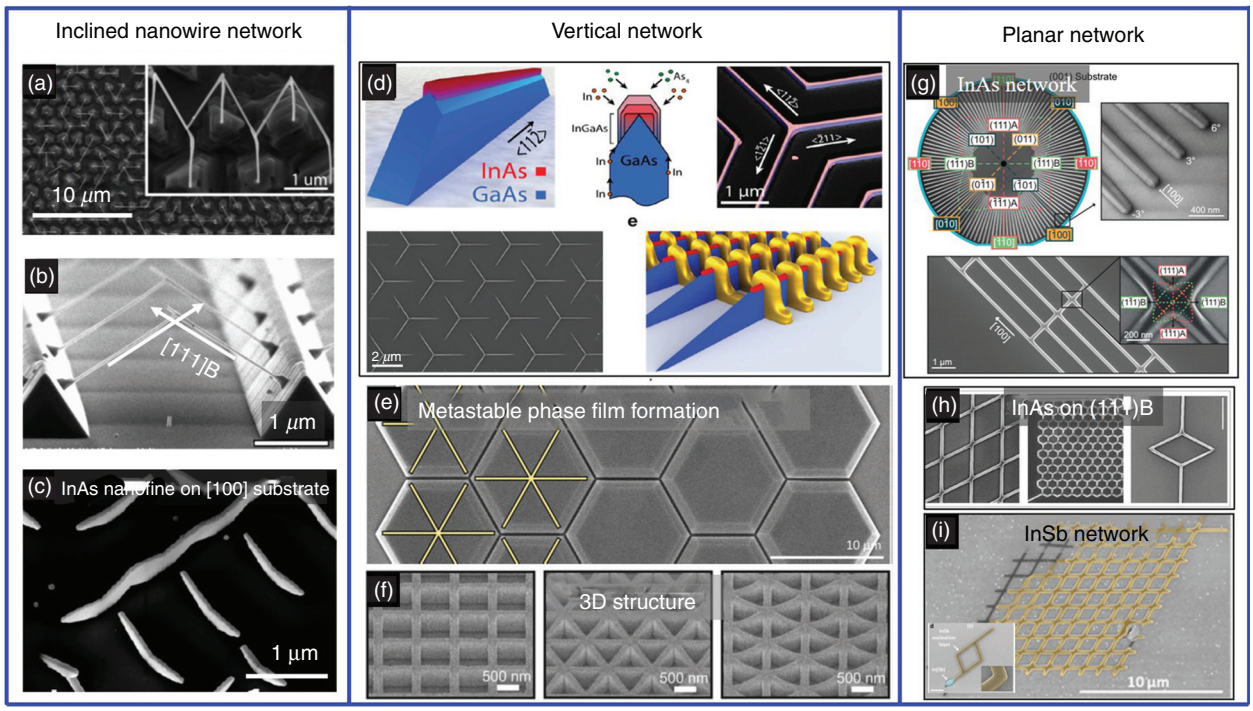

FIG. 7. Three types of nanowire networks grown by SAE: inclined (a–c), vertical (d–f), and planar (g–i). (a) InAs. Reproduced with permission from Krizek *et al.*, Nano Lett. **17**, 6090 (2017). Copyright 2017 American Chemical Society.[187] (b) InAs nanowire networks on InP ridges. Reproduced with permission from Dalacu *et al.*, Nano Lett. **13**, 2676 (2013). Copyright 2013 American Chemical Society.[188] (c) SAE of InAs nanofin network on Si (100) substrate. Reproduced with permission from Conesa-Boj *et al.*, ACS Nano **6**, 10982 (2012). Copyright 2012 American Chemical Society.[191] (d) GaAs/InAs network. Reproduced with permission from Friedl *et al.*, Nano Lett. **18**, 2666 (2018). Copyright 2018 American Chemical Society.[192] (e) WZ quasi-film InP. Reproduced with permission from Staudinger *et al.*, Nano Lett. **20**, 686 (2019). Copyright 2019 American Chemical Society.[56] (f) GaN network. Reproduced with permission from Winnerl *et al.*, Nanoscale **11**, 4578 (2019). Copyright 2019 Royal Society of Chemistry.[178] (g) InAs in-plane nanowire network on (100) substrate. Reproduced with permission from Krizek *et al.*, Phys. Rev. Mater. **2**, 093401 (2018). Copyright 2018 American Physical Society.[193] (h) InAs nanowire network on (111)B substrate. Reproduced with permission from Aseev *et al.*, Nano Lett. **19**, 218 (2019). Copyright 2019 American Chemical Society.[12] (i) InSb nanowire network. Reproduced with permission from Aseev *et al.*, Nano Lett. **19**, 9102 (2019). Copyright 2019 American Chemical Society.[11]

transfer-printing" technique, the same researchers, in collaboration with the University of Strathclyde, realized the integration of two orthogonal SA-grown InP nanowire THz detectors into a single monolithic device, thereby creating three-dimensional nanowire network-based THz detectors that enable fast and precisely measured full THz states.[197] This polarization-sensitive detector is compact without a cross-talk issue, which is beyond what can be achieved by most commercially available THz detectors at present. These single, pure WZ SAE-InP nanowires can also be developed for infrared lasing application by being transferred onto and integrated with a planar waveguide device or cat's eye antenna to change the lasing directionality.[198,199] This opens up the path to establish highly integrated photonic systems in the future, with emitting sources and detection elements based on SAE single nanowires or nanowire networks. In addition to single-nanowire–based devices, the carefully designed and grown nanostructure patterns and networks can be directly used for scalable device fabrication, as discussed in detail in Sec. V A–V D.

A. Photonics

High-aspect and uniform III–V nanowire arrays can form 2D photonic crystals (PCs)[200–202] and are also suitable for 2D PC-based light-emitting devices that contain an active region.[203,204] Scofield *et al.*[205] reported the formation and optical properties of bottom-up PC cavities formed by III–V nanopillars via SAE. These precisely controlled nanopillar arrays enabled formation of active photonic crystal. Wang *et al.*[137] reported the first highly scalable monolithic solution to the long-awaited missing piece of Si photonics: integrated laser sources on Si. In-plane InP-distributed feedback laser array was demonstrated on a 300-mm Si (001) substrate via a combination of SAE and a top-down integration scheme, providing a route toward the integration of dense arrays of III–V laser sources with Si photonic circuits. Kim and colleagues[121,206,207] pioneered the SAE of III–V nanowire arrays on pre-patterned SOI substrate. Using the vertical InGaAs nanowire arrays to form a photonic crystal cavity together with the waveguide structure, they demonstrated room temperature operation of chip-scale optically pumped III–V nanowire array lasers monolithically integrated on silicon [see Fig. 8(a)]. Furthermore, Kim *et al.*[139] demonstrated photonic crystal lasers operating at 1290 nm at room temperature using InGaAs/InP core/shell nanowire arrays grown on SOI substrates. Moreover, these nanowire laser arrays exhibit robust emission without any signature of heating or degradation. Instead of using free-standing nanowires, Han *et al.*[208] demonstrated in-plane InP/InGaAs multi-QW nanoridge arrays on {001} SOI as a template. Using these

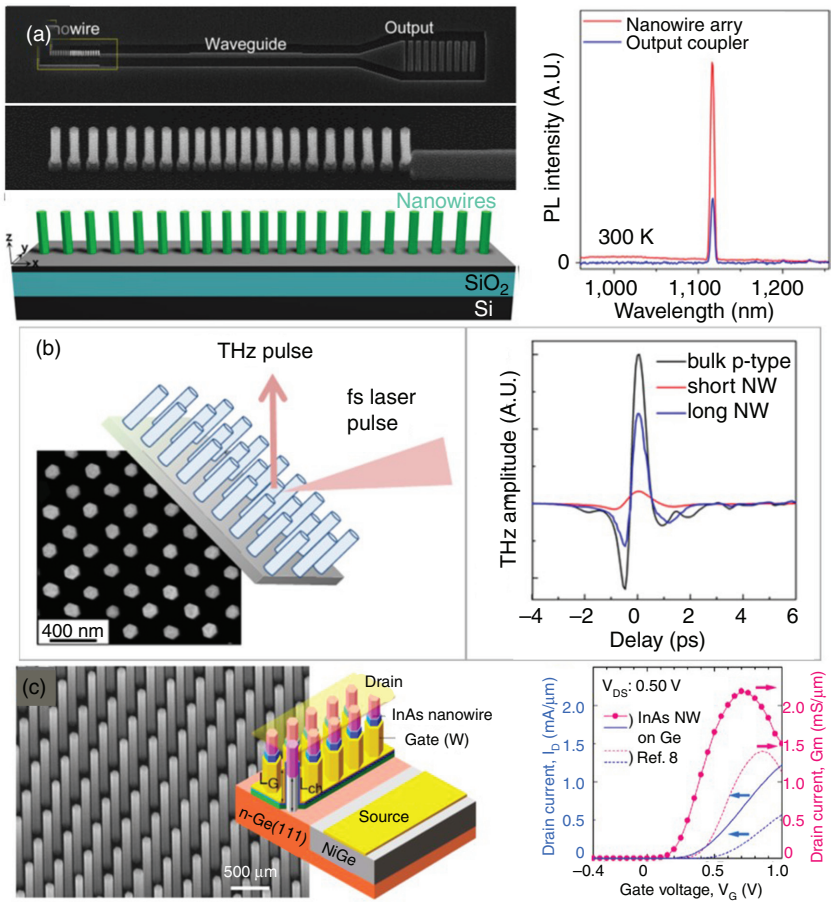

FIG. 8. Applications of nanowire arrays in lasing and FETs. (a) Integration of InGaAs nanowire array laser on SOI substrate with a waveguide structure. Reproduced with permission from Kim *et al.*, Nano Lett. **17**, 3465 (2017). Copyright 2017 American Chemical Society.[206] (b) Strong THz emission using InAs nanowire array. Reproduced with permission from Arlauskas *et al.*, Nano Lett. **14**, 1508 (2014). Copyright 2014 American Chemical Society.[212] (c) Vertical InAs nanowire transistor array. Reproduced with permission from Tomioka *et al.*, Nano Lett. **15**, 7253 (2015). Copyright 2015 American Chemical Society.[213] A.U., arbitrary units; fs, full spectrum; NW, nanowire.

nanoridges as a template, they achieved lasing at room temperature in the telecommunications wavelength range. Recently, they reviewed the progress of III–V lasers selectively grown on (001) silicon substrates.[209] Sergent *et al.*[210] obtained InGaN/GaN quantum disk nanowire arrays and realized room-temperature lasing in the near-ultraviolet range by using GaN as the gain medium. These results represent a new platform for ultra-compact and energy-efficient optical links and provide a pathway toward practical and functional nanowire lasers.

For THz emission applications, the emission intensity depends on the aspect ratio and pitch size of the III–V nanowire arrays.[211] Arlauskas *et al.*[212] demonstrated that the high-aspect-ratio nanowire area is very efficient for emission in the THz range [see Fig. 8(b)]. The THz emission efficiency of an optically pumped n-type InAs nanowire array is found to be up to approximately three times stronger than that of bulk p-type InAs.

B. Electronics

SAE III–V nanowires are of great interest for next-generation high-performance transistors. With integrated circuits being scaled down to deep submicrometer levels, materials with high mobility and integrability are required. Epitaxially grown III–V semiconductor nanowires have a much higher electron mobility than the traditional silicon FET channels. The large surface-to-volume ratio of nanowires, with wrap- or FinFET gates, provides a high on-to-off current ratio. SAE has precise controllability and allows growth at predefined positions without the aid of catalysts; thus, it is a natural path for fabricating wrap-gated FETs (for vertical wires[214]) or FinFETs (for planar wires/nanosheets[17,215]) on a large scale.

Desplanque *et al.*[216] fabricated tunnel diodes based on the InAs/AlGaSb, which has near-broken gap band alignment. Typical Esaki diode characteristics were obtained, with a maximum peak current density >1 MA/cm^2 for large-area devices. Moreover, the anisotropic faceting of selectively regrown InAs induced different tunneling current densities, depending on the orientation of the device with respect to the crystallographic directions. Tomioka and Fukui[217] developed a nanowire-based tunnel FET (TFET) using InAs nanowires on silicon substrates. The fabricated devices showed a switching operation under reverse bias conditions, with a subthreshold slope of 104 mV/decade. The switching behavior with Zener tunneling was achieved at a low drain-source voltage (V_{ds}) of 50 mV. The device also showed the potential of increasing the ON-state current in TFET and steep-slope gate operation. N-type InAs nanowires grown on p-type Ge substrates were used to fabricate vertical transistors with transconductance higher than conventional FETs, as illustrated in Fig. 8(c).[213]

Along with the development of quantum information and quantum computing, the research of SAE of semiconductor nanostructures is becoming more active recently. For example,

semiconductor–superconductor hybrid materials provide a promising field for non-Abelian anyons,[13,218] a fundamental building block of topological quantum computers. The elementary topological quantum computing operation is anyon braiding. The braiding operation has to be executed in two-dimensional systems or one-dimensional network structures.[219–221] SAE is capable of providing III–V semiconductor network structures. Krizek *et al.*[193] demonstrated the growth of InAs networks successfully. They achieved InAs networks on a GaAs-based buffer layer with a substantial enhancement of field effect mobility. These InAs networks with buffered geometry showed a strong spin–orbit interaction and a long phase-coherence length, which are essential features for topological superconductivity. Using an Al/InAs SA–grown network, Vaitiekėnas *et al.*[10] measured the parity effect of a superconductor island, while Ménard *et al.*[222] and Anselmetti *et al.*[223] showed the conductance-matrix symmetries and nonlocal conductance measurements in SA-grown nanostructures.

C. Optoelectronics

For photodetector and solar cell applications, the key characteristic is light absorption. Nanowire and nanoshape arrays are well known to be more efficient in light absorption than their planar counterparts, which is also beneficial in reducing material usage and costs. Moreover, another advantage of nanostructure arrays is the geometry-dependent light absorption characteristics, which can be tuned by pattern design.[224–227] The progress of nanowire array solar cells was critically reviewed by Otnes and Borgström.[228] Currently, the best nanowire solar cell efficiency of GaAs and InP nanowire arrays grown via the bottom-up approach is 15.3%[229] [see Fig. 9(a)] and 13.8%,[33] respectively. The world-record cell efficiency of III–V nanowire array solar cell is 17.8% using top-down–fabricated InP nanowire arrays.[230] However, this number is still far below the Shockley–Queisser limit[231] and is also lower than their planar device counterparts.[232] Among these nanowire array solar cells, the optimized short-circuit current density is close to the theoretical limit, while the open-circuit voltage is still much lower than the radiative limit.[233] The large nonradiative surface recombination velocity deteriorates the optoelectronic device performance. Surface passivation is needed to overcome this drawback, such as GaAs/AlGaAs[229] and GaAs/GaInP nanowires.[138] Moreover, carrier selective contacts can be used to provide both surface passivation and low contact resistance, thereby improving the cell efficiency as demonstrated in InP/ZnO/AZO radial nanowire array solar cells.[234] Increasing omnidirectional light absorption efficiency by either coating the nanowire with dielectric particles to provide Mie scattering or deep sidewall subwavelength structure formation in the nanopillars have been shown to boost cell efficiency.[230,235] Otnes *et al.*[236] combined electron beam–induced current and dark IV measurements using nanoprobes in an SEM to correlate the material properties to cell performance. The understanding gained from charge carrier collection and carrier recombination characteristics was used to improve the design of InP nanowire array solar cells and subsequently increase the efficiency by more than sevenfold.[236] Using III–V nanowire arrays on Si substrates for solar cell applications is quite appealing since they can increase the efficiency while reducing the cost by avoiding the expensive III–V substrates. Furthermore, this architecture can be used as a tandem solar cell by utilizing the different bandgaps of the III–V nanowires on the Si substrates.[237] The optimized bandgap (1.7 eV) in a double-junction device can be realized using InGaP or GaAsP ternary nanowire arrays. To further improve the cell efficiency, the nanowire array geometry (diameter, length, and pitch size) has to be properly designed for current-matching conditions. However, up until now, the efficiency of III–V nanowires on silicon solar cells is still lower than that of single nanowire array solar cells,[238] which leaves space for future optimization. For aerospace applications where high-efficiency, low-weight, and tolerance to irradiation are required, III–V nanowire solar cells are ∼10 times more tolerant to radiation damage compared with their planar counterparts.[239]

Taking advantage of the light trapping effect in periodic nanowire arrays, incident light can be reflected and refracted multiple times to enhance the light absorption, which can greatly improve the performance of photodetectors. Lee *et al.*[240] demonstrated vertically InAsSb nanopillar array photodiodes where the small size and three-dimensional geometry of the nanopillars were used to reduce the dark current and increase the path length of incident light and carrier diffusion length. In addition, localized surface plasmon resonances can be excited by partially coating the InAsSb nanopillars with a metal layer, leading to high quantum efficiencies of ∼29% at 2390 nm.[240] Using the intersubband transitions in QWs or QDs is an approach to extend the range of detection wavelengths. Karimi *et al.*[31] demonstrated an excellent broadband InP/InAsP QW nanowire array photodetector operating from the visible to the far-infrared region (20 μm). Vertical p-n heterojunction structure in nanowire arrays can be used to suppress dark current and enhance the signal-to-noise ratio of the device[81,241] [Fig. 9(b)]. For instance, Gibson *et al.*[241] fabricated a highly sensitive photodetector using tapered InP nanowire p-n junction array. The photodetector showed near-unity multispectral absorption, high multiplication gain ($>10^5$), subnanosecond time response, and high timing resolution photodetection without the need for cryogenic cooling,[241] opening up new possibilities for applications in remote sensing, three-dimensional imaging, and quantum communication. Chiba *et al.*[242] grew vertical InGaAs nanowire array photodiodes on Si. By implementing a heavily Sn-doped contact layer, the contact resistance between the nanowires and Ti/ITO was significantly reduced, which improved the diode characteristics and photoresponsivity about twofold. Moreover, the passivation effect provided by the InP shell increased the photocurrent density in the 1.55-μm wavelength band.

For LED applications, GaN-based *p-i-n* or heterostructure nanowires are widely used for both UV and visible light.[152,243] UV-C band (100–280 nm) is particularly useful for sterilization applications, but the materials technology suffers from extremely low efficiency. To improve its efficiency, Liu *et al.*[82] reported the growth of AlGaN nanowire arrays with full tunability of Al composition. The spontaneously formed Al-rich AlGaN shell significantly suppressed nonradiative surface recombination to achieve an internal quantum efficiency of 45% at room temperature. These nanowire LEDs operated in the UV-C band and exhibited excellent optical and electrical performance, including a small turn-on voltage of ∼4.4 V and an output power of ∼0.93 W/cm^2 at a current density of 252 A/cm^2. This achievement is promising to break the efficiency bottleneck of deep UV LEDs. InGaN/GaN QW nanowire arrays are well established for LEDs operating in the visible light range, covering from red to blue emission. In addition to the ability to tune the emission wavelength by adjusting the QW thickness/composition, the LED wavelength can also be tuned from 690 to 440 nm, covering the emission range from red to blue, by

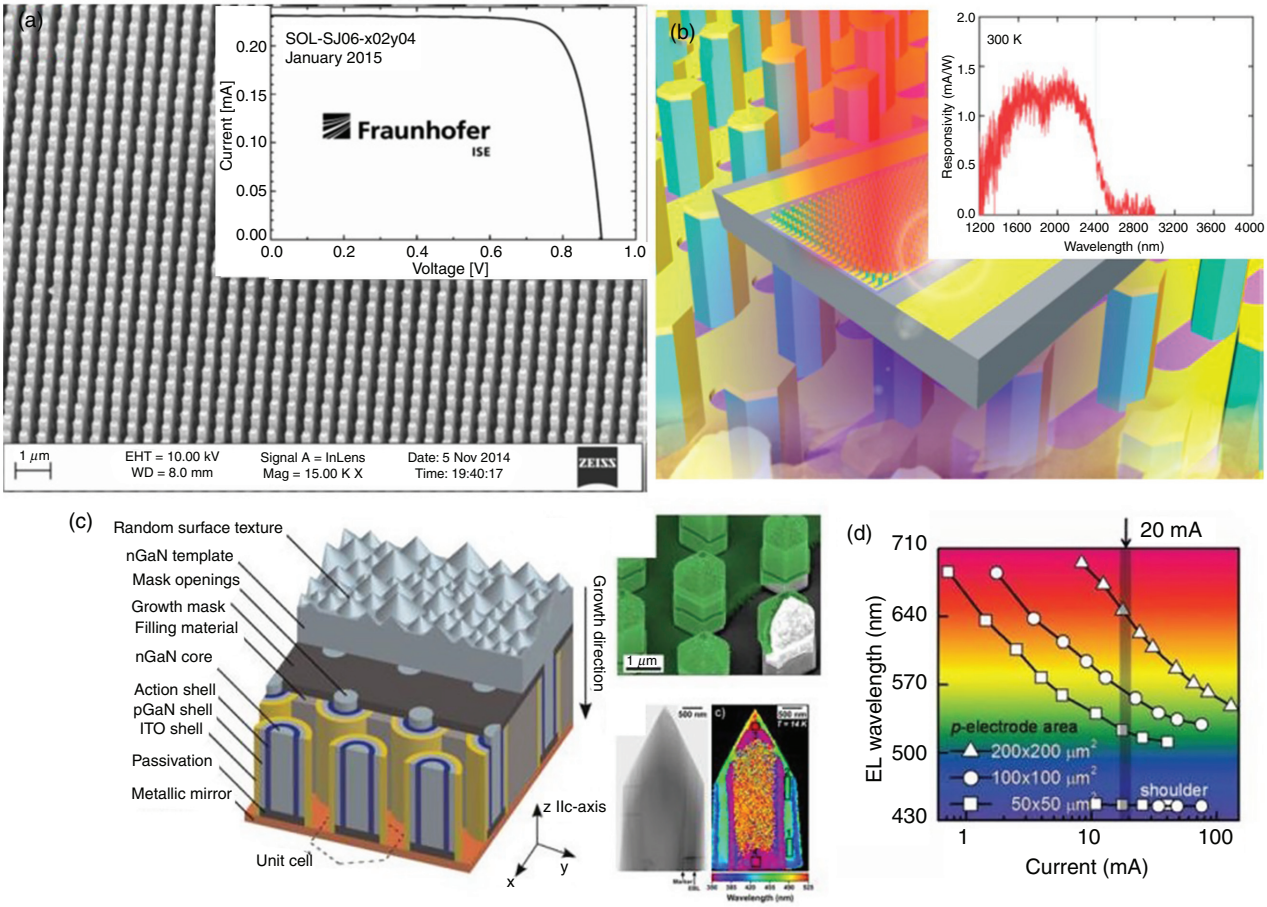

FIG. 9. Application of nanowire arrays in optoelectronics. (a) GaAs nanowire array solar cell with world-record efficiency. Reproduced with permission from Åberg *et al.*, IEEE J. Photovolt. **6**, 185 (2016). Copyright 2016 IEEE.[229] (b) Mid-infrared InAs nanowire array photodetector operation at room temperature. Reproduced with permission from Ren *et al.*, Nano Lett **18**, 7901 (2018). Copyright 2018 American Chemical Society.[81] (c) InGaN/GaN QW microwire array operating in the visible wavelength range. Reproduced with permission from Schimpke *et al.*, Phys. Status Solidi (A) **213**, 1577 (2016). Copyright 2016 John Wiley & Sons, Inc.[150] A/W, photocurrent/incident optical power; EHT, electron high tension; EL, electroluminescence; Mag, magnification; WD, working distance.

simply increasing the bias voltage.[244] Scalable production of InGaN/GaN QW microrod white LEDs has been demonstrated on a 4-in. sapphire wafer with an external quantum efficiency of 3% and an internal quantum efficiency of 10%.[150] White light emission could be achieved with two approaches. The first is polychromatic mixing of red, green, blue, and yellow color-emitting diodes. This color mixing could be realized by a multiple-stacked tunnel junction core–shell structure[155] that integrates the multicolor emission in one single epitaxial step. The second is blue/violet LED coating with yellow phosphor as an alternative approach to achieve white light emission. For nano-LEDs, micrograin phosphors can be used to fit between individual microrods and to adapt to the unique morphology of the nanowires. In addition to the nanowire shape, InGaN QWs grown on semipolar planes and nonpolar planes in nanosheets and nanopyramids result in a higher indium content[245] and are used to tune the emission wavelengths in nano-LEDs. Wu *et al.*[246] fabricated an electrically driven phosphor-free white LED using InGaN/GaN nanopyramids. They found that the QW width and composition varied on the {10–11} planes, leading to emitted light changing from blue to yellow along the planes of the pyramidal nanostructures. Nanosheet/nanostrip green LEDs were fabricated by Nakajima *et al.*,[247] with dimensions ranging from 100 to 300 nm. A sharp electroluminescence emission peak was observed from QWs grown on {10–11} facets and blue-shifted from 551.1 to 541.1 nm with increasing injection current. Novel contacting approaches were used in nano-LED fabrication. Tchernycheva *et al.*[248] used transparent graphene to contact single nanorods and compared the performance of graphene with metal contacts. For the near-infrared LED applications, InP- or GaAs-based QW nanowire arrays are more suitable, as demonstrated by Yang *et al.*[157] using InP/InGaAs multi-QW nanowire arrays.

D. Other fields

In addition, III–V nanowire arrays can be applied for other applications thanks to their specific properties. For instance, the nontoxicity of InP makes it a suitable biomaterial. The uniform InP nanowire

arrays were utilized as scaffolds for understanding the regeneration of neurons and their networks.[249] They demonstrated that the isotropic arrangement of InP nanowires acted as physical cues to guide neurite growth, leading to the formation of a neuronal network. Moreover, the suitable bandgap and superior electronic properties make III–V semiconductors promising candidates for photoelectrochemical applications.[250] The band edge of InP and GaP are very suitable for water splitting. With the advances in InP and WZ GaP nanowire array fabrication, Standing *et al.*[251] and Gao *et al.*[252] demonstrated that the photocathode conversion efficiencies of nanowire array were higher than their planar counterparts. They achieved a photocathode efficiency of 6.4% using p-type InP nanowire arrays as the photocathode. The deposited MoS_3 nanoparticles effectively increase the efficiency, meanwhile improving its stability. Still, the application of III–V nanowire array in water-splitting application is limited by high costs and severe corrosion issues. By coating III–V nanowire arrays with cocatalysts like cobalt oxide and nickel oxide, it has been shown that stability of the nanowire electrodes could be improved as these oxide layers protect nanowires, act like hole scavengers, and protect from photocorrosion.[253]

VI. CHALLENGES AND OPPORTUNITIES

A. Crystal growth engineering

Shape control and crystal phase purity are fundamental topics in SAE and form the basis for high-performance devices based on these nanostructures.

The interest in growing nanoshape and network arrays has been increasing in recent years. This field, however, is still in the early stages. Most works are related to pure binary compound growth. Understanding the growth fundamentals of nanoshapes needs further development to guide the growth and allow the formation of nanostructures of different shapes and geometries for both photonics and electronics applications. In terms of shape engineering, InP and GaN are more suitable candidates compared with InAs and GaAs. However, the formation of nanoshapes with other III–V semiconductors needs further exploration. Numerical simulations are also needed to understand the absorption, scattering, and different light–matter interaction processes within the nanoshape arrays with different geometries. New types of heterostructures can be explored using nanosheets and other nanomembranes as a template. Nanosheet-based heterostructure provides a new platform for fundamental optical property studies, such as WZ/ZB nanosheet homojunction with a large area interface for type II band alignment. Vertical nanoshape device fabrication is more difficult than the in-plane nanoshape device. Thus, assembly of horizontal nanoshape arrays and networks can have the advantage in scalable fabrication of electronic and photonic devices with a compatible process planar device technology. Moreover, the high-quality III–V semiconductors can be grown in the in-plane configuration compared to vertical nanostructures, such as III-Sb compound.[11,12] In addition, advances in the growth of nanowire network arrays are just beginning. Previous studies of vertical InSb nanowire networks have achieved great success. However, in-plane network formation shows design feasibility as well as an easy device fabrication process. For quantum science, epitaxial growth of high-quality metal on the III–V nanostructures is vital. Recently, Gill *et al.*[254] presented SAE of Al on InSb nanowires, realizing near-unity Andreev reflection at the InSb–Al interface. However, this process still needs sulfur passivation and pre-ion–milling steps, which could introduce defects at the semiconductor–superconductor interface. Consequently, further advances of metal epitaxy on the semiconductors are required.

Crystal phase control is still a challenge for most III–V (except for InP) nanowire arrays grown by SAE. A high density of twin defects can be easily formed in these nanowires. Liu *et al.*[80] correlated the surface reconstruction of (111) surface to polytypism in InAs nanowires. Using classical nucleation theory and synchrotron radiation, they showed that surface recombination can reduce the stacking fault energy to favor the WZ nucleation. Still, the pure phase InAs nanowire array has not been achieved. Phase purity via pattern design does not apply to InAs nanosheet arrays. Instead, it seems that SA-grown InAs nanowires and nanosheets show a similar growth behavior.[9] Thus, the crystal quality of III-As nanoshape arrays needs further optimization. Compared with the great success of III-N, III-P, and III-As nanowire arrays, direct growth of III-Sb nanowire and nanoshape arrays is still of great challenge.

Metastable hexagonal crystal phase formation is another approach to modify the electronic structure and performance of materials. One amazing role of metastable WZ/hexagonal phase formation is its possibility to tune the indirect bandgap-to-direct bandgap structure in GaP, Ge, and SiGe alloys. The exciting direct bandgap nature of Ge-based alloys could realize light sources compatible with CMOS circuits.[169] However, direct growth of III–V or IV planar layers with metastable phase is extraordinarily challenging. Metastable WZ phase only forms when grown axially along the ⟨111⟩ direction or laterally on a WZ template. Up to now, three methods have been developed and show promise to produce metastable phase film: radial epitaxy,[56,169] conformal epitaxy,[51] and TASE.[15,19] Radial epitaxy makes use of the matured growth of WZ III–V nanowire arrays (SA-VLS for GaAs, GaP, and InAs; SAE for InP) and have been successfully applied to form direct bandgap SiGe nanowires and films. The lattice-matching requirement for this method suggests that WZ GaAs and ZnS are two promising candidates since their lattice constants are the closest to Ge. Moreover, detailed growth studies of the merging process should be carried out to avoid dislocation, antiphase boundary formation. Thermodynamics and kinetics calculations in the nanosystem should also be developed to guide the parameter window for producing the metastable phase. The beauty of conformal epitaxy and TASE is the ability to directly form a WZ/hexagonal-layered structure on prepatterned {001}-oriented substrates, which are the most commonly used orientation in the industry. However, these two methods require a complex set of fabrication steps, starting with nucleation, deposition of sacrificial layer (a-Si, for example), oxide mask cavity formation, etching of the sacrificing layer, etc. Still, these two methods are developing rapidly thanks to their potential for integration of III–V materials on Si substrates.

B. Si CMOS-compatible integration

Having both optical and electronic elements on the same chip with a large-scale production and compatible process with CMOS techniques is the dream of the semiconductor industry. The high-gain property of III–V materials make them suitable as the light source. Consequently, monolithically integrating III–V nanostructures on silicon or SOI is attracting a lot of interest, where SAE offers great freedom and the possibility of designing and growing III–V photonic crystals and active layers on SOI substrates with predesigned

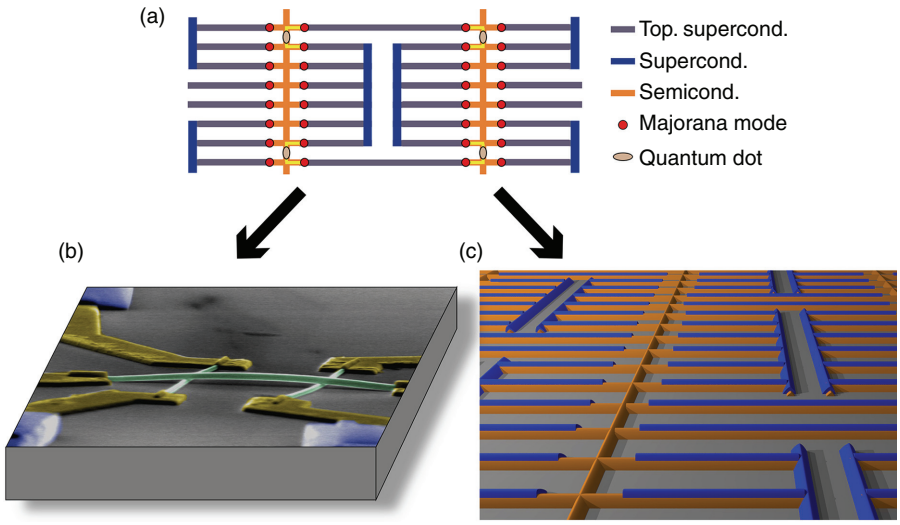

FIG. 10. Realization of complex quantum networks. (a) Schematic of a non-Abelion operation network. Reproduced with permission from Karzig *et al.*, Phys. Rev. B **95**, 235305 (2017). Copyright 2017 American Physical Society.[221] (b) Electrical contacts formed on nano crosses. (c) Large-scale 1D SA-grown nanowire network. semicond., semiconductor; supercond., superconductor; top. topological.

waveguide or grating structure to pave the way for the on-chip photonic integration.[121] Until now, the epitaxy of free-standing InP nanowire and nanoshape arrays on silicon is still challenging. InP microring provides both gain material and a circular-shaped cavity where whispering gallery modes are supported. Moreover, multiple ring lasers can be coupled to a single bus waveguide, which can be used for optical interconnects and wavelength division multiplexing applications. Therefore, based on the current progress of SAE of InP nanostructures, solving the nucleation difficulties of InP on Si can significantly advance the development of Si-based photonics. For instance, whispering gallery mode microring lasers, vertical nanowire lasers, and random nanowire lasers can be achieved depending on the design. Apart from the free-standing nanowires, in-plane III–V nanowires on {001} silicon substrate or SOI is quite promising. The use of patterned Si nanoridge with inclined {111} facets on SOI can be used to guide planar III–V nanostructure formation, making full use of the well-accumulated knowledge in top-down fabrication technique to isolate the optical mode from the substrate. Thus, it is very promising for on-chip light source applications.

C. Quantum science applications

For quantum science applications, III–V semiconductor nanowire networks are highly desired. For example, InAs/InSb nanowire–-based spin–orbit qubit devices[255] or topological quantum devices need to have a high density of nanowires over a large area. For fault-tolerant topological quantum computing, where the quantum gate is realized by utilizing non-Abelian braiding operation, T-shape or X-shape nano crosses are critical. Figure 10(a) shows a typical topological computing network structure, which is difficult to assemble. Cross structures by the controlled deposition of individual nanowires are hard to scale up and avoid defect formation [Fig. 10(b)]. SAE is a perfect platform for large-scale growth of the nanowire networks. The network location and shape can be precisely controlled by defining the openings on the pattern of the mask [Fig. 10(c)]. High-quality joints are required to ensure phase coherence to enable spin or Majorana modes to move freely in these networks.

VII. CONCLUSIONS

SAE is a powerful bottom-up approach for researchers to create semiconductor nanostructures with a variety of shapes and geometries, such as free-standing and in-plane nanowire arrays, nanoshape arrays, and nanowire networks with high crystal quality and uniformity. Furthermore, SAE allows easy incorporation of dopants and heterostructure formation. By designing appropriate dimensions of the mask thickness and opening, threading dislocations induced by lattice mismatch can be trapped on the sidewalls of the mask, thereby allowing monolithic integration of III–V nanodevices on silicon substrates. Thanks to these unique advantages offered by SAE, it is fast becoming the technique of choice to produce nanobuilding blocks for the next-generation photonic, electronic, and optoelectronic devices as well as for quantum science applications.

AUTHORS' CONTRIBUTIONS

X.Y. and D.P. contributed equally.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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