SILICON / SILICON OXIDE / LPCVD SILICON NITRIDE STACKS: THE EFFECT OF OXIDE THICKNESS ON BULK DAMAGE AND SURFACE PASSIVATION

Hao Jin, K.J.Weber, A.W.Blakers
Centre for Sustainable Energy Systems, Faculty of Engineering and Information Technology, The Australian National University, Canberra ACT 0200, Australia
ph +61 2 6125 5132; fax +61 2 6125 0506; E-mail hao.jin@anu.edu.au

ABSTRACT: Silicon / thermally grown silicon dioxide / LPCVD silicon nitride stacks were formed to investigate the influence of the oxide thickness on silicon bulk and surface properties after thermal processing. With no oxide, the LPCVD silicon nitride layer causes serious irreversible bulk damage to silicon wafers after a high temperature treatment. A thin oxide layer (~10nm) helps to substantially reduce the damage. A thick oxide (more than 50nm) can help completely eliminate the bulk damage. An increase of surface states was indicated by an increase of emitter the saturation current density for the stacks with thin oxide layers after high temperature treatments. Even after a re-growth of thick oxide layer and forming gas anneal, the stacks previously without oxide layer shows a much higher emitter saturation current value, which indicates silicon nitride causes a serious Si-SiO_2 interface damage.
Keywords: LPCVD, Emitter saturation current, Effective lifetime

1 INTRODUCTION

Silicon Oxide / LPCVD Silicon Nitride stacks are potentially useful for novel solar cell structures due to the favourable properties of the silicon nitride layer. LPCVD SiN is also used in BP's SATURN cell process. LPCVD is an economic and very reliable batch production method that provides a nearly stoichiometric (Si_3N_4) film. It is an excellent oxidation and diffusion mask and is resistant to chemical attack by alkaline or acidic silicon etchants. To take full advantage of these properties, the nitride layer should be able to withstand high temperature process steps without significantly degrading the surface or bulk properties of the silicon wafer.

LPCVD silicon nitride, different from PECVD silicon nitride, can not passivate silicon surface. The difference comes from the hydrogen concentration difference between LPCVD (H atom concentration 5%-10%) and PECVD (H atom concentration 20%-25%). Hydrogen has been studied for decades and demonstrated to play a significant role at Si-SiO_2 interface. It can passivate the silicon surface by reacting and combining with silicon dangling bonds. Hydrogen concentration in silicon nitride film, silicon oxide and Si-SiO_2 interface will devrease as the stack is heated at high temperature. Losing hydrogen at Si-SiO_2 interface results in an increasing in silicon surface states and silicon surface recombination velocity.

Previous work [1-3] has shown that i) serious bulk damage is introduced into the silicon wafer when the nitride layer is deposited directly onto silicon, due to stress generated during annealing between Si and Si_3N_4; ii) loss of hydrogen from the Si-SiO_2 interface of Si/SiO_2/SiN structures is chiefly responsible for the increased surface recombination following such high temperature treatments; and iii) hydrogen can be re-introduced by high temperature forming gas anneals. Here, we investigate the effect of oxide thickness in more detail in order to obtain a better understanding of the interface region and hence allow better optimisation of process conditions.

2 EXPERIMENTAL DETAILS

The effective lifetime τ_{eff} was measured by quasi-steady state photoconductivity decay (QSSPCD) measurements, as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{2S}{W} \qquad (1)$$

Where τ_b is the bulk lifetime. S and W are the surface recombination velocity and wafer thickness. S has the relationship with J_{oe}, the emitter saturation current as follows [4,5]:

$$S = J_{oe}\frac{N + \Delta n}{qn_i^2} \qquad (2)$$

Where Δn is the injection level and N is the emitter doping level.

Equation (1) shows that at a certain injection level (we use the injection level of $6x10^{15}$ /cm^3) the emitter saturation current is proportional to surface recombination velocity, which is related with hydrogen concentration at silicon / silicon oxide interface.

Equations (2) shows that if the silicon surface is well passivated, the effective lifetime can be referred as the minimum bulk lifetime.

Float Zone (FZ), p-type, 100 Ω/cm, (100), 500 μm thickness wafers, FZ, p-type. 0.8 Ω/cm, (100), 350 μm thickness wafers and CZ, n-type, 0.5 Ω/cm, (100), 500 μm thickness wafers were used to investigate the protective effect of oxide layers on the silicon bulk. FZ, p-type, 100 Ω/cm, (100), 500 μm thickness wafers were also used to investigate changes in the silicon surface properties due to the nitride layer following thermal processing. Both sides of the wafers were passivated with a light phosphorous diffusion (R~ 300 Ω/□ after thermal drive in), a thermally grown oxide (900°C or 1000°C for different times) and a 30minute anneal in nitrogen [6] followed by a 30 minute anneal at 450°C in forming gas (FGA, 5% H_2 in argon) to ensure an initially well passivated surface.

LPCVD Si_3N_4 deposition was done at 775°C and 0.5torr to give an approximately 50nm thick nitride layer. The wafers were subjected to a high temperature anneal (HTA) at 1000°C in nitrogen. In order to distinguish

between silicon bulk and surface damage, the nitride layers were then stripped in hot phosphoric acid, without substantially etching the underlying oxide, and a FGA followed resulting in a well-passivated surface. Some wafers were deglazed in 10% HF solution until hydrophobic and an 80nm oxide was grown on both sides followed by a FGA to give a well-passivated silicon / silicon oxide interface.

3 RESULTS AND DISCUSSION

3.1 Nitride effect on silicon bulk

Figure 1 shows the comparison of effective lifetime for high resistivity wafers without oxide layer and with a thin (10nm) oxide layer. Both stacks underwent a 1000°C HTA. After being deglazed in 10% HF solution, an 80nm thick oxide was grown on both sides and a FGA followed. It is clear that even a 10nm oxide can significantly reduce bulk damage, compared to the case of no oxide (for its highest value, around 1.2ms at the injection level of $2x10^{14}$ /cm^3). The wafer without oxide was seriously bulk-damaged during the HTA process.

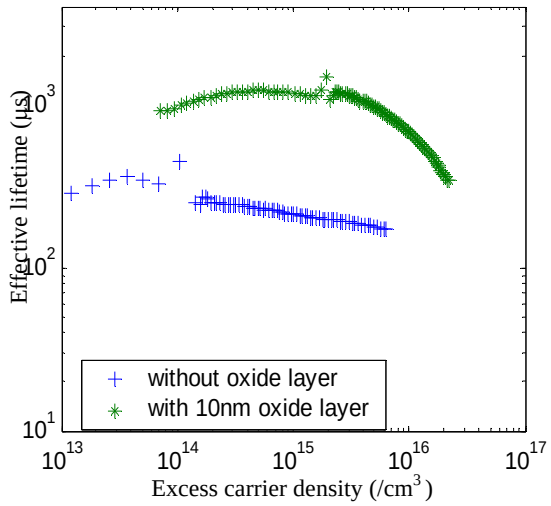

Figure 1: Comparison of the effective lifetime of wafers with and without oxide layer, following a 1000°C anneal

	original oxide thickness (nm)			
	0		50	
	FZ	CZ	FZ	CZ
Effective lifetime as oxidised (μs)	--	--	60	9.0
Effective lifetime after re-oxidation (μs)	13	1.4	49	7.1

Table 1: Comparison of the effective minority carrier lifetime of diffused, oxidised wafers before and after nitride deposition and anneal, for 0.8 ohm-cm p-type FZ and 0.5 ohm-cm n-type CZ wafers

Figure 2 shows the comparison of effective lifetime for wafers with a 10nm oxide. The 'as oxidised' values are for a sample undergoing a thermal oxidation and a forming gas anneal. The 'after oxide re-growth' values are for the same sample after removal of both SiO_2 and Si_3N_4 layers, followed by re-growth of an 80nm oxide and FGA. The drop in effective lifetime demonstrates significant bulk damage to the initially 10nm thick oxide sample after re-growth of an 80nm oxide layer. Therefore, the presence of a 10nm oxide between the silicon wafer and LPCVD silicon nitride, although beneficial in helping to reduce bulk damage, does not entirely prevent bulk damage to the silicon wafer caused by the presence of the nitride film.

For the stacks with a thin oxide (10-25nm), a drop in effective (minimum bulk) lifetime is apparent after HTA and 80nm oxide layer re-growth compared with the effective lifetime of the as-oxidised wafers. Three wafers are used for each measurement. All wafers demonstrate the similar changes. The average value from the measurements, at an injection level of $2x10^{14}$ /cm^3, are summarised in table 2.

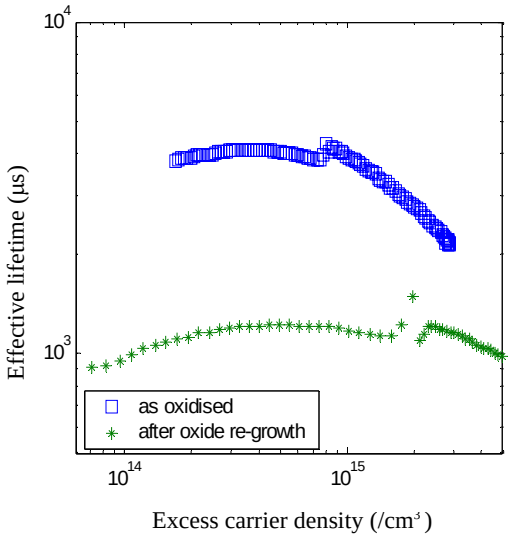

Figure 2: Comparison of the effective lifetime for wafers with a 10nm oxide before and after a 1000°C anneal

	original oxide thickness (nm)		
	10	25	50
τ_{eff1} (as oxidised, ms)	3.8	5.4	5
τ_{eff2} (re-oxidised, ms)	1.1	2.4	3.8
τ_{eff2} / τ_{eff1}	0.29	0.44	0.76

Table 2: Effective lifetime values for wafers with different oxide thicknesses before and after a high temperature anneal

With the increase of oxide layer thickness, the bulk lifetime comes closer to the as-oxidised value, indicating less bulk damage due to the protection of thicker oxide layer. More than 50nm oxide should be applied to prevent the apparent damage.

3.2 Dependence of surface passivation on oxide thickness

For high resistivity wafers, the emitter saturation current density (J_{oe} per side) at an injection level of $6x10^{15}$ /cm^3 was determined after the re-growth of an 80nm oxide and a FGA. Three wafers are taken and the average value is recorded in table 3. The table shows that the J_{oe} of the wafer without oxide before nitride deposition is almost double that of a wafer with a 25nm oxide. The increase in J_{oe} may indicate an increase in the silicon surface defect density caused by the stress at the Si - Si_3N_4 interface.

Oxide thickness before LPCVD (nm)	0	10	25
J_{oe} (10^{-14}A/cm^2) after growth of 80nm oxide and FGA	3.8	2.3	2.2

Table 3: Emitter saturation current density Joe per side as a function of the initial oxide thickness, following a high temperature anneal, removal of oxide and nitride and re-growth of an 80nm oxide.

Table 4 shows a comparison of J_{oe} values for wafers with thin oxide layers before and after HTA. All J_{oe} values were measured at the injection level of $6x10^{15}$ /cm^3. The 'J_{oe} as oxidised' indicates the emitter saturation current measured just after an initial oxidation and a FGA. The same wafers then underwent a LPCVD, HTA, nitride strip and FGA. 'J_{oe} after H-reintroduction' was then measured. Around a 20% increase in J_{oe} was observed, which may be caused by a slight increase in the interface defect density.

Oxide thickness (nm)	10	25
J_{oe} as oxidised (e^{-14}A/cm^2)	2.6	2.7
J_{oe} after H-reintroduction (e^{-14}A/cm^2)	3.0	3.3

Table 4: Comparison of emitter saturation current density J_{oe} before and after a high temperature anneal

4 CONCLUSIONS

In conclusion, both CZ and FZ silicon wafer with low or high initial resistivity are demonstrated to have serious bulk damage after HTA if there is not any oxide layer protecting the silicon surface between silicon and LPCVD silicon nitride. Slight Si-SiO_2 interface damage and silicon bulk damage could be introduced after high temperature process to Si / thin SiO_2 / Si_3N_4 stacks. Silicon bulk damage level and silicon interface defect states density may go down as more oxide is applied. A more than 50nm oxide layer should be used in order to prevent the bulk and surface damage most completely.

ACKNOWLEDGMENTS

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