

Ultrathin (<10nm) Nb₂O₅/NbO₂ Hybrid Memory with Both Memory and Selector Characteristics for High Density 3D Vertically Stackable RRAM Applications

Seonghyun Kim¹, Xinjun Liu¹, Jubong Park¹, Seungjae Jung¹, Wootae Lee¹, Jiyong Woo¹, Jungho Shin¹, Godeuni Choi¹, Chumhum Cho², Sangsu Park², Daeseok Lee¹, Eui-jun Cha², Byoung-Hun Lee^{1,2}, Hyung Dong Lee³, Soo Gil Kim³, Suock Chung³, and Hyunsang Hwang^{1,2*}
¹School of Materials Science and Engineering, ²Dept. of Nanobio Materials and Electronics, Gwangju Institute of Science and Technology, Gwangju, Korea, ³R&D Division, Hynix Semiconductor Inc., San 136-1 Ami-ri Bubal-eub Icheon-si, Gyeonggi-do, Korea
Phone: +82-62-715-2314, Fax: +82-62-715-2304, *e-mail: hwanghs@gist.ac.kr

Abstract

We report, for the first time, the novel concept of ultrathin (~10nm) W/NbO_x/Pt device with both threshold switching (TS) and memory switching (MS) characteristics. Excellent TS characteristics of NbO₂, such as high temperature stability (~160°C), fast switching speed (~22ns), good switching uniformity, and extreme scalability of device area (φ~10nm)/thickness (~10nm) were obtained. By oxidizing NbO₂, we can form ultrathin Nb₂O₅/NbO₂ stack layer for hybrid memory devices with both TS and MS. Without additional selector device, 1Kb cross-point hybrid memory device without SET/RESET disturbance up to 10⁶ cycles was demonstrated.

Introduction

Resistive switching memory has been intensively studied as most promising candidates for next generation non-volatile memory application, owing to its excellent scalability, high speed operation, and low power consumption [1]. However, for integration of cross-point (4F²) structure, the bi-directional selector is required to suppress the sneak current path. Although various candidates were reported as a selector (Fig. 1(a)), several problems such as uni-directional [2,3], destructive readout [4], complex material composition [6], Cu ion control [7] and low current density [8] need to be solved. Although VO₂ with Insulator-Metal-Transition (IMT) characteristics is promising selector candidate, the operation temperature (~67°C) is too low for memory applications [5].

In this paper, we propose unique hybrid memory device with both IMT selector and memory characteristics. Hybrid memory structure by simply stacking alternatively has an advantage in terms of process complexity over 1S1R for 3D cross-point structure (Fig. 2). The concept of hybrid memory structure was illustrated by simulation result with MATLAB (Fig. 3).

Experiment

Both NbO_{2-x} film (~10nm) for threshold switching and Nb₂O_{5-x} film (~10nm) for memory switching were formed by controlling oxygen concentration using via-hole structure (φ=250 nm) on Pt/Ti/SiO₂/Si substrate. Pt or W top electrode was deposited by DC sputtering system. We also fabricated cross-point 1Kb hybrid memory (φ=150 nm) array with bi-layer NbO_x (Nb₂O_{5-x}/NbO_{2-x}) by controlling oxidation condition (Fig. 4).

Results and discussion

Characterization of threshold switching behavior of Pt/NbO_{2-x}/Pt with high thermal stability and excellent scalability

Fig. 5 shows typical bipolar resistive switching behavior of W/Nb₂O_{5-x}/Pt device. After forming process, uniform switching characteristics was observed. Fig. 6 represents *I-V* characteristics of Pt/NbO_{2-x}/Pt. We intentionally formed NbO_{2-x} film by reactive sputtering method to obtain TS property. After 1000 cycles, excellent uniformity of switching parameter such as, V_{th} and V_{hold} was shown in Fig. 7. Thermal stability of TS device was measured at a high temperature (Fig. 8). TS property remains stable up to 433K, which is much higher than VO₂ film (only a 340K) [4]. Fig. 9 shows physical property of MS and TS film by XPS and Raman analysis, where different

atomic ratio (Nb/O) and Raman shift were observed between each films. We simulated temperature distribution of TS device using COMSOL. Under SET operation, we have confirmed relatively high temperature at the center of the device which might explain IMT behavior of TS (Fig. 10). Additionally, fast switching speed (~22ns) was observed using real-time oscilloscope measurement (Fig. 11). To investigate the scalability of TS film, *I-V* characteristics was measured by C-AFM with 10nm Pt-coated tip (Fig. 12). Excellent scalability of TS down to 10nm was clearly observed. The switching current was also proportionally with scaling device area which indicates bulk conduction through NbO₂ layer. Compare with filament-type local conduction, bulk TS can guarantee excellent uniformity of TS as shown in Fig. 7.

Excellent characteristics of hybrid memory (W/NbO_x/Pt) and 1Kb cell array for 3D vertical cross-point applications

Fig. 13 shows *I-V* characteristics of hybrid memory (W/ultrathin bi-layer NbO_x/Pt stack). Compared with control RRAM without selector, hybrid memory exhibits significant reduction of leakage current of unselected cell (±1/2V_{read} region). In addition, hybrid memory shows sufficiently high ON current (>2MA/cm²). The estimated current for 10×10nm² device is about 2uA which is sufficient for SET/RESET operation. Fig. 14 illustrated proposed switching mechanism of W/NbO_x/Pt hybrid memory device. A 10nm-thick NbO_x film which consisted of Nb₂O_{5-x} for MS and NbO_{2-x} for TS can produce ideal memory operation with internal selector characteristics. During SET/RESET mode, high voltage was applied which activate both TS and MS. In contrast, only TS property is activated under V_{read} condition. Under 1/2V_{read} condition, TS maintains off state which can suppress parasitic leakage current. Fig. 15 shows x-TEM image and EDX line profile of W/NbO_x/Pt device. 10nm-thick of NbO_x layer is clearly observed. Compared with VO₂ IMT device which has limited operation temperature (<67°C), hybrid memory device shows excellent memory characteristics up to 125°C with good switching uniformity as shown in Fig. 16.

To confirm the feasibility for 3D RRAM, we fabricated 1Kb hybrid memory cell array with 150nm active area. DC switching behavior in 1Kb cell array is comparable with discrete device. Disturbance of unselect device under read mode (@±1/2V_{read}) is negligible. Furthermore, we achieved stable SET/RESET operation up to 10⁶ cycles without disturbing unselect device (@±1/2V_{SET/RESET}) (Fig. 17 & Fig. 18). Finally, calculated read-out margin was significantly improved by suppressing the LRS current at 1/2V_{read} of unselected cell in hybrid memory (Fig. 19).

Considering ultrathin film thickness (~10nm) and excellent device characteristics, hybrid memory is promising candidate for the 3D vertical memory applications [9]. (Fig. 1(b))

Conclusion

Ultrathin hybrid RRAM with MS and TS is successfully demonstrated by controlling oxygen concentration of NbO_x. Hybrid memory exhibits excellent memory characteristics such as, ultrathin film thickness, simple process step, excellent disturbance immunity for cross-point memory, high temperature stability, and area scalability down to 10nm. Hybrid memory shows promise for high density vertical 3D cross-point memory applications.

Acknowledgement This work was supported by R&D Program of the Ministry of Knowledge Economy in Korea.

References [1] International Technology Roadmap for Semiconductors (ITRS), 2009 [2] Y. Sasago et al., *Symp. On VLSI Tech. Dig.*, p. 24, 2009 [3] M.-j. Lee et al., *IEDM Tech. Dig.*, p. 771, 2007 [4] E. Linn et al., *Nature Mater.*, Vol. 9, p. 403, 2010 [5] M.-j. Lee et al., *Adv. Mat.*, Vol. 19, p. 3919, 2007 [6] D. Kau et al., *IEDM Tech. Dig.*, p. 617, 2009 [7] K. Gopalakrishnan et al., *Symp. On VLSI Tech. Dig.*, p. 205, 2010 [8] J. Shin et al., *JAP*, 033712, 2011 [9] I. G. Baek et al., *IEDM Tech. Dig.*, p. 737, 2011

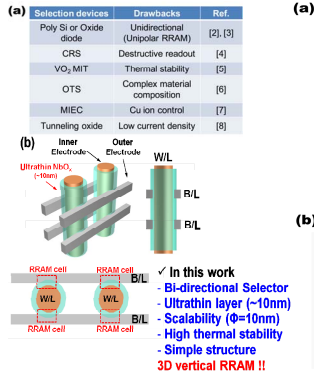


Fig. 1 (a) Drawbacks of existing selection devices. (b) 3D vertical RRAM structure using ultrathin NbO_x layer (~10nm) - In this work

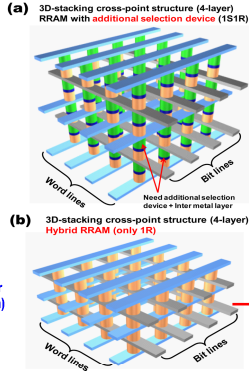


Fig. 2 Comparison of 3D stacking structure (a) 1S1R (b) only 1R & SEM image of 4-layers-hybrid memory.

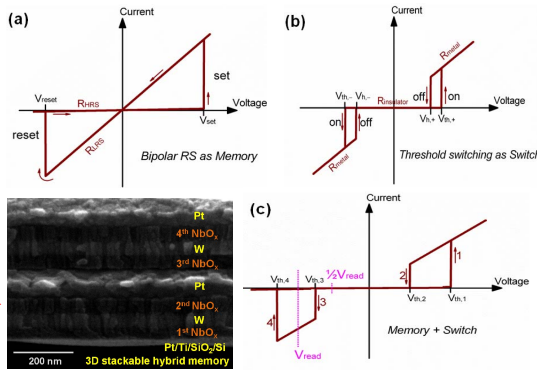


Fig. 3 Ideal concept of hybrid memory + switch element for 3D cross point RRAM device with MATLAB simulation.

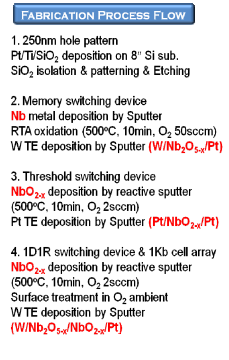


Fig. 4 Summarized fabrication process flow in this work.

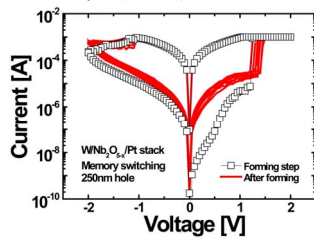


Fig. 5 Memory switching behavior of W/Nb₂O_{5-x}/Pt stack in 250 nm hole.

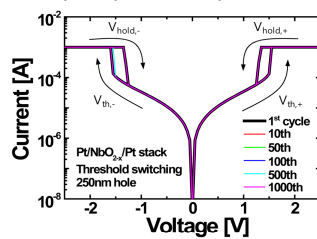


Fig. 6 Threshold switching behavior of Pt/NbO_{2-x}/Pt stack in 250 nm hole.

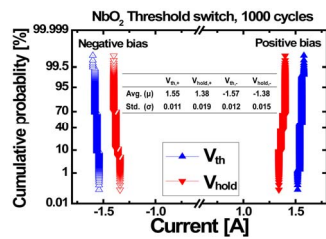


Fig. 7 Cumulative probability of V_{th} and V_{hold} during 1000 cycles in NbO_{2-x} threshold switch device.

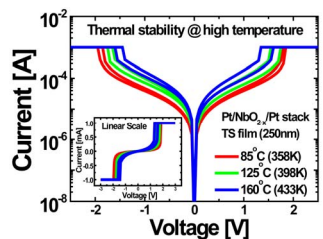


Fig. 8 Thermal stability test of NbO_{2-x} threshold switch device at high temperature measurement.

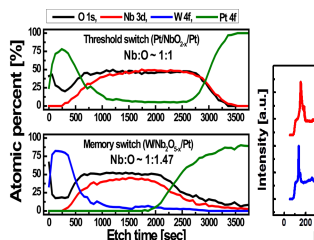


Fig. 9 XPS depth profile and Raman analysis of both threshold switching and memory switching devices.

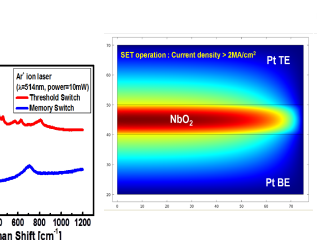


Fig. 10 Thermal simulation of TS film under SET operation by COMSOL.

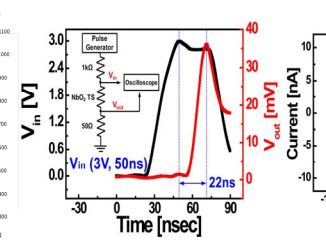


Fig. 11 Real-time response of switching speed using oscilloscope in TS device.

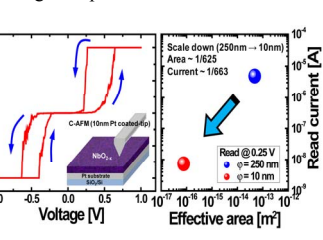


Fig. 12 C-AFM scanning results with extreme nanoscale tip (~10nm) for investigation of scalability.

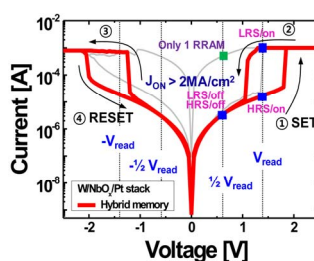


Fig. 13 I-V characteristics of hybrid memory device (W/NbO_x/Pt) in 250 nm scale and schematic of data reading.

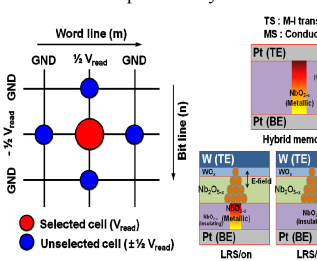


Fig. 14 Proposed switching mechanism.

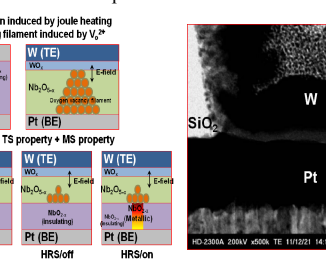


Fig. 15 Cross section TEM image and EDX line profile of W/NbO_x/Pt hybrid memory device.

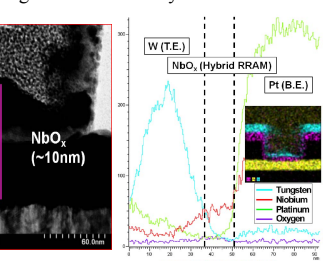


Fig. 16 I-V characteristics of hybrid memory device (W/NbO_x/Pt) at high temperature measurements and distribution of randomly selected 50 cells of hybrid memory devices.

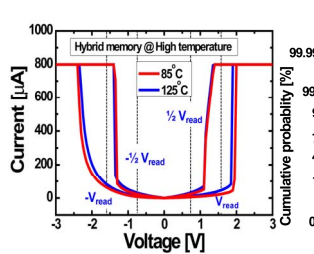


Fig. 17 Optical & SEM images and I-V curve of hybrid memory in 1Kb cross-point structure.

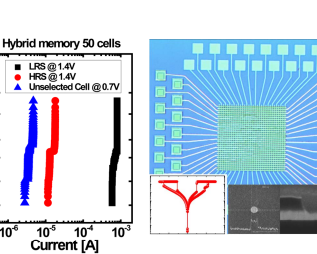


Fig. 18 Disturbance test of unselected device under read mode (1/2V_{read}) and set/reset mode (1/2V_{SET/RESET}) in 1Kb cell array.

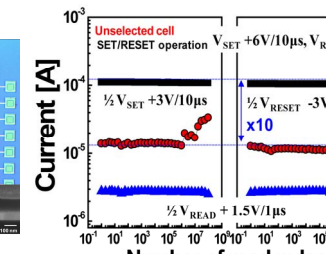


Fig. 19 Calculated readout margin of hybrid memory and only 1 RRAM device under worst case.

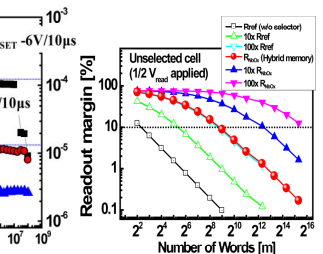


Fig. 20 Calculated readout margin of hybrid memory and only 1 RRAM device under worst case.