Transfer of monocrystalline Si films for thin film solar cells

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ABSTRACT: Monocrystalline silicon is an excellent material for photovoltaic applications. Until recently, it was considered to be unsuitable for the next generation of thin film solar cells since no cost effective ways of producing thin, monocrystalline silicon layers were known. However, the last few years have seen the development of a number of new techniques which allow the detachment of silicon films from a single crystal substrate. These new approaches promise higher cell efficiencies than appear to be possible with more traditional thin film polycrystalline silicon solar cells at a similar cost. This paper reviews the layer transfer approaches currently under investigation and briefly discusses some of the issues that need to be addressed for commercial production.

INTRODUCTION

Solar cells based on crystalline silicon (c-Si) have dominated the photovoltaic market since its birth. Today, several other promising materials which may be used in the next generation of solar modules have been identified and intensively studied. However, while good efficiencies are being achieved for some materials, such as copper indium diselenide, all are likely to face substantial obstacles to their widespread deployment. In particular, the relative scarcity of some of the elements needed for several of these semiconductors, such as Ge for a-Si/Ge cells, In for CIS cells and Te for CdTe cells means that their ultimate potential impact on world electricity production is limited [1]. CdTe cells face a further obstacle due to the toxicity of Cd. For these reasons, it is likely that c-Si cells will continue to play a dominant role in photovoltaics for decades to come.

Since about half the cost of a PV module based on c-Si cells lies in the starting wafer, it is clear that substantial reductions in the price of PV electricity can only be achieved if the cost of the starting material is reduced. Consequently, thin film c-Si solar cells, with an active layer thickness of only several microns to tens of microns, have been of considerable interest over the last decade. A recent review of current research efforts in this field is given in [2,3]. Most of the research

effort over the past decade has focussed on the deposition of silicon on foreign substrates, such as glass, ceramics and graphite. Serious problems have been encountered with all of these approaches, mainly resulting from the difficulty of obtaining a high quality silicon film when it is deposited on a non-silicon substrate. The low quality of the silicon, and in particular the low minority carrier lifetime, limit the efficiency potential of solar cells.

A recent approach which sidesteps this difficulty is to epitaxially deposit silicon on specially prepared monocrystalline silicon substrates. Following fabrication of solar cells on the epitaxial layer, it is released from the substrate and the substrate is re-used. Thus, the active silicon layers are monocrystalline and can be of excellent electronic quality, while the high cost of the single crystal substrate wafer can be tolerated because it is re-used many times. Although the relevant techniques have only been developed in the last few years, progress has been rapid and good cell efficiencies have already been achieved. This is a clear indication of the potential of these approaches to meet the challenge of a cost effective, solar cell technology. In this paper, we review the various approaches that have been suggested for the transfer of thin monocrystalline silicon films and briefly discuss various issues that will need to be addressed in the future.

1. Approaches based on epitaxial lateral overgrowth

In epitaxial lateral overgrowth (ELO) the substrate is coated with a masking material into which openings are made to expose the substrate. When epitaxial growth is carried out under the right conditions, growth will begin in the areas where the substrate is exposed and then spread laterally over the substrate. Note that the entire deposit has the same crystal orientation as the substrate. Successful ELO requires selective epitaxial growth, in other words, the prevention of spurious nucleation on the masking layer.

ELO was first extensively studied for III-V compounds grown by vapour phase epitaxy. McClelland et al. used (110) oriented GaAs substrates coated with patterned carbonised photoresist [4-6]. The process is illustrated in figure 1. The openings in the resist layer formed stripes spaced 50 _m apart and 2.5 _m wide. Under the appropriate conditions, epitaxial growth proceeded out of the stripes and laterally over the carbonised resist layer. The separate growth fronts eventually coalesced together to produce a continuous epitaxial layer. The ratio of lateral to vertical growth rate was reported to be about 25.

ELO of silicon has been investigated more recently. Several investigators have used liquid phase epitaxy to produce ELO structures on near (111) oriented silicon substrates [7-9]. Chemical vapour deposition has also been investigated [10-12]. However, with CVD spurious nucleation on the masking layer is often observed, and avoiding spurious nucleation requires either very careful control of all the growth parameters or the use of growth/etch back cycles [13]. The sophistication required of this process is such that it is likely to remain too expensive for photovoltaic applications. In contrast, LPE offers virtually perfect selectivity by virtue of the fact that growth takes place close to thermal equilibrium.

In order to utilise ELO for the transfer of monocrystalline films, a method must be found of detaching the epitaxial layers from the substrate and transferring them to a suitable (temporary or permanent) substrate. In the CLEFT technique (Cleavage of Lateral Epitaxial Films for Transfer) of McClelland et

al, the epitaxial film and GaAs substrate are bonded to suitable supports and cleaved off.

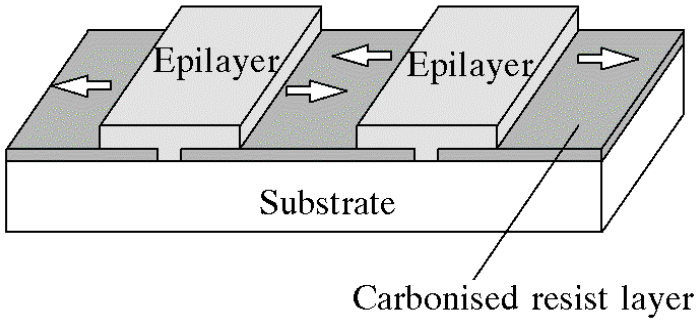

Figure 1: Illustration of ELO for the CLEFT technique. Separate epitaxial layers laterally overgrow the masking layer until the growth fronts coalesce.

This approach was successful because the adhesion of the epitaxial layer to the masking layer was very weak, and the attachment areas between the epilayer and substrate were small. In this way it was possible to grow and separate several epilayers from the same substrate. In principle, the same approach could be used for silicon as well. LPE on carbonised resist coated substrates has been carried out in our group, and under appropriate conditions the adhesion between resist layer and epilayer has been found to be small. In practice, however, the CLEFT approach becomes impractical for large area structures. Another approach is to remove the masking layer and introduce an etchant into the gap between the epilayer and the substrate. If the attachment regions are kept narrow, the etchant can readily detach the epilayer from the substrate without significant damage to either substrate or epilayer. The possibility of using etching for the detachment of the epilayer was realised by Bozler et al. [14] although it does not appear to have been implemented.

1.1 The Epilift technique

The Epilift technique has been described in several recent publications [15-17]. A silicon substrate is provided with a masking layer (usually SiO_2), in which line seeds are opened. The line seeds form a continuous pattern such as a square mesh pattern. Typically, the line seeds are 5-10 μm wide and spaced 100 μm apart. An epitaxial layer is then selectively grown by liquid phase epitaxy. The epilayer initially grows out of the seed lines and then progressively overgrows the substrate. This results in a continuous mesh, with holes which become progressively smaller as growth is continued. Growth is terminated before the holes have closed up completely. In order to detach the layer from the substrate, the oxide is first removed in HF. A silicon etchant is then introduced into the gap between the epilayer and the substrate. The attachment regions are etched through and the epilayer can be removed from the substrate. The process is illustrated in figure 2.

The growth of epilayers using the Epilift technique is similar to that using the CLEFT approach of Bozler et al. The most important difference is the use of a continuous mesh as the seeding pattern, as opposed to the use of discrete seeding lines. The growth of epilayers according to the technique of Bozler et al. results in a completely closed epilayer, so that etchant can only be introduced from the edges of the wafer. This approach quickly becomes impractical for epilayers with an area of 1 cm^2 or larger, as the distance that the etchant has to travel becomes too great. In the Epilift approach, the array of holes remaining in the epilayer following growth provides access for the etchant, so that any size of epilayer can be detached. This is particularly important for flat plate solar cells which typically have dimensions of 10x10 cm^2 or larger.

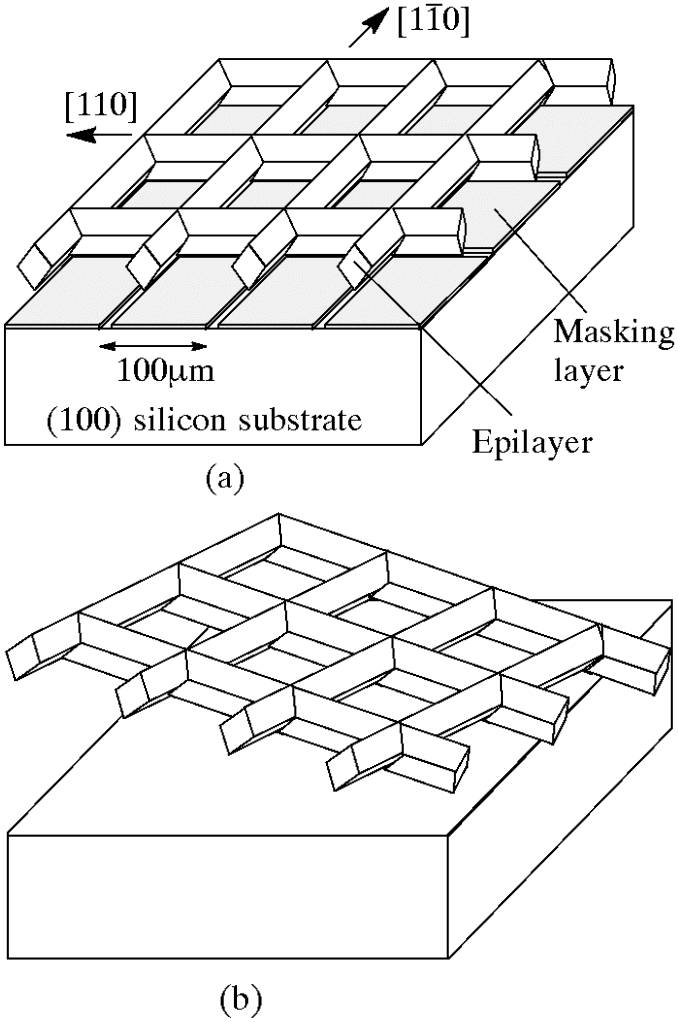

Figure 2: The Epilift technique. (a) An epitaxial layer is grown out of seed lines on a (100) or (111) silicon substrate, (b) following cell fabrication, the grid is detached and the substrate is re-used.

Another advantage of the use of a continuous mesh is that it avoids two problems commonly associated with the growth by LPE out of discrete openings. The first problem is the coalescence of separate epitaxial growth fronts. Depending on the type of pattern employed, coalescence may not take place or may lead to inclusions or the formation of defects at the seam where the epilayers merged [18]. Only under a limited set of conditions, and over small areas, has it to date been possible to join epilayers with little or no defects at the seam [18,19].

The second problem is the impact of dislocations and other extended crystallographic defects on epitaxial growth. The growth of dislocation free epitaxial islands is limited by the formation of {111} crystal planes, leading to the formation of epitaxial islands of predictable shape. However, in the presence of dislocations with a significant screw character, the dislocations act as a source of atomic steps. This has a dramatic impact on epitaxial layer morphology, and the predictable shape of the islands is lost [20]. In the case where the seed lines form a continuous mesh, the presence of dislocations does not significantly alter the epitaxial layer shape. In this case, the internal corners of the epitaxial structure provide a continuous supply of atomic steps which appears to be much more effective than any dislocations [21].

Solar cell processing must be adapted to the fact that the epilayer contains many holes. The presence of holes can be used to advantage because it is easy to transfer both electrons and holes to the rear surface, thus eliminating the metal grid on the sunward facing side.

Cells with any desired degree of transparency can be fabricated for specialist applications. A detached lambertian reflector behind the cells allows the collection of nearly all the light that passes through the holes. A transparency of 50-70% can be tolerated which means that a significant reduction in epitaxial growth time and silicon usage is possible. Few details of the epitaxial growth or cell processes have been released. A single sided cell design is used, where the metal grids of both polarities are on the rear (non illuminated) side of the cell, has been found to be suitable. An efficiency of 10.9% has been measured on a 50cm^2 area cell.

2. Approaches based on porous silicon

Porous silicon can be produced by a number of techniques. For photovoltaic applications electrochemical etching appears to be the most practical approach. Porous silicon has been of intense interest chiefly due to its potential application in silicon optoelectronics and several excellent reviews on the subject are available [22,23]. Typically, a p type silicon wafer is immersed in a 10% HF solution. When a positive bias is applied, dissolution of the silicon results. At low current densities, porous silicon formation results while at high current densities, electropolishing results. The size and morphology of the pores depends on the doping and type of the silicon, its crystal orientation, the current density and the solution concentration [24]. In general, lightly doped silicon results in large pores up to 1μm or larger, while heavily doped silicon leads to the formation of small pores down to several nm in diameter. The exact mechanism of porous silicon formation is still under debate. In general terms, the HF attacks the silicon in the presence of holes, with the holes being supplied by the material (in the case of p type silicon) or by illumination. Two important feature of porous silicon formation by electrochemical etching are that etching generally only takes place at the porous-Si – monocrystal Si interface, and that the porosity of the material depends on the current density. This allows the creation of extremely useful structures which have a low porosity surface but a high porosity layer buried beneath the surface. The porosity can be varied to be anywhere between approximately 10 and 90%.

2.1 The Ψ process

In the perforation within silicon (Ψ) process [25,26], a (100) oriented silicon substrate is first textured with random pyramids, or with inverted pyramids using photolithographic techniques. The pyramids have a feature size of several microns. A porous silicon film of the order of 1 μm thick is then produced by electrochemical etching. An epitaxial layer several microns thick is deposited on the porous layer. The use of ion assisted deposition (IAD) [27] at 700^{o}C results in a conformal epitaxial layer. Subsequently, the sample is detached from the substrate, by the application of ultrasound or by bonding the epilayer to a suitable superstrate and applying a mechanical force. Characterisation by X-ray diffraction has demonstrated that the layers are monocrystalline. Due to the highly textured nature of the films, excellent light trapping can be expected. Modelling indicates that cell efficiencies up to 18% may be achievable for devices less than 5 μm thick. Chemical vapour deposition has also been used. This results in improved material quality, but deposition is no longer conformal. A 15 μm thick cell has achieved 12.5% efficiency, while a 5x5 cm^2 five cell module recorded 10.2% [28].

If silicon deposition is carried out with IAD, the Ψ process potentially allows for very simple monolithic series connection of cells. Brendel suggested the technique of shadow epitaxy [28]. In this approach, a series of wires serve to shield portions of the substrate from epitaxial deposition. By changing the position of the wires during the deposition of the 3 layers (back surface field, p type layer and n type layer), series connection can be achieved. A mini-module containing 6 cells was demonstrated.

2.2 The SCLIPS process

The SCLIPS process (Solar Cells by Liquid Phase Epitaxy over Porous Silicon) [29,30] originated from the ELTRAN (Epitaxial Layer Transfer) process developed at Canon [31]. A porous silicon layer

approximately 10 μm thick is formed by electrochemical etching. The porous silicon is oxidised, the oxide is removed from the top surface with HF and the sample is annealed at 1000°C in H_2. This closes the pores at the surface. An epitaxial layer is grown by liquid phase epitaxy. Detachment of the epilayer is achieved by a water jet which splits the layer from the substrate. An efficiency of 9.5% has been demonstrated on a small area (0.2 cm^2) solar cell [31].

2.3 The QMS process

In the QMS process investigated by the University of Stuttgart [33], as well as a similar process at Sony Corp. [34], the silicon wafer is provided with two regions of very different porosity, as shown in figure 3. Initially, the wafer is electrochemically etched at a low current density, resulting in the formation of a low porosity surface layer. The current density is then increased to create a high porosity buried layer. During annealing, the pores coalesce to form voids. As a result, the low porosity surface layer is turned in a monocrystalline layer containing voids up to 1μm in size, while the high porosity layer transforms into a separation layer with weak Si bridges. Due to the presence of voids, the surface layer is termed quasi monocrystalline silicon (QMS). Epitaxy is carried out by CVD from $SiHCl_3$. Solar cells have been fabricated on the epitaxial layers. At the University of Stuttgart, the structure typically consists of a 3 μm thick, heavily B doped layer acting as a back surface field, and a more lightly doped, active layer [33]. Standard laboratory solar cell processes were employed. Detachment of the epilayer was achieved following cell fabrication by bonding the cell to a glass superstrate and applying a mechanical force. Efficiencies of 15.4 and 16.6% for 4 cm^2 devices with active layer thicknesses of 24.5 and 46.5 μm thickness, respectively, were demonstrated. [35].

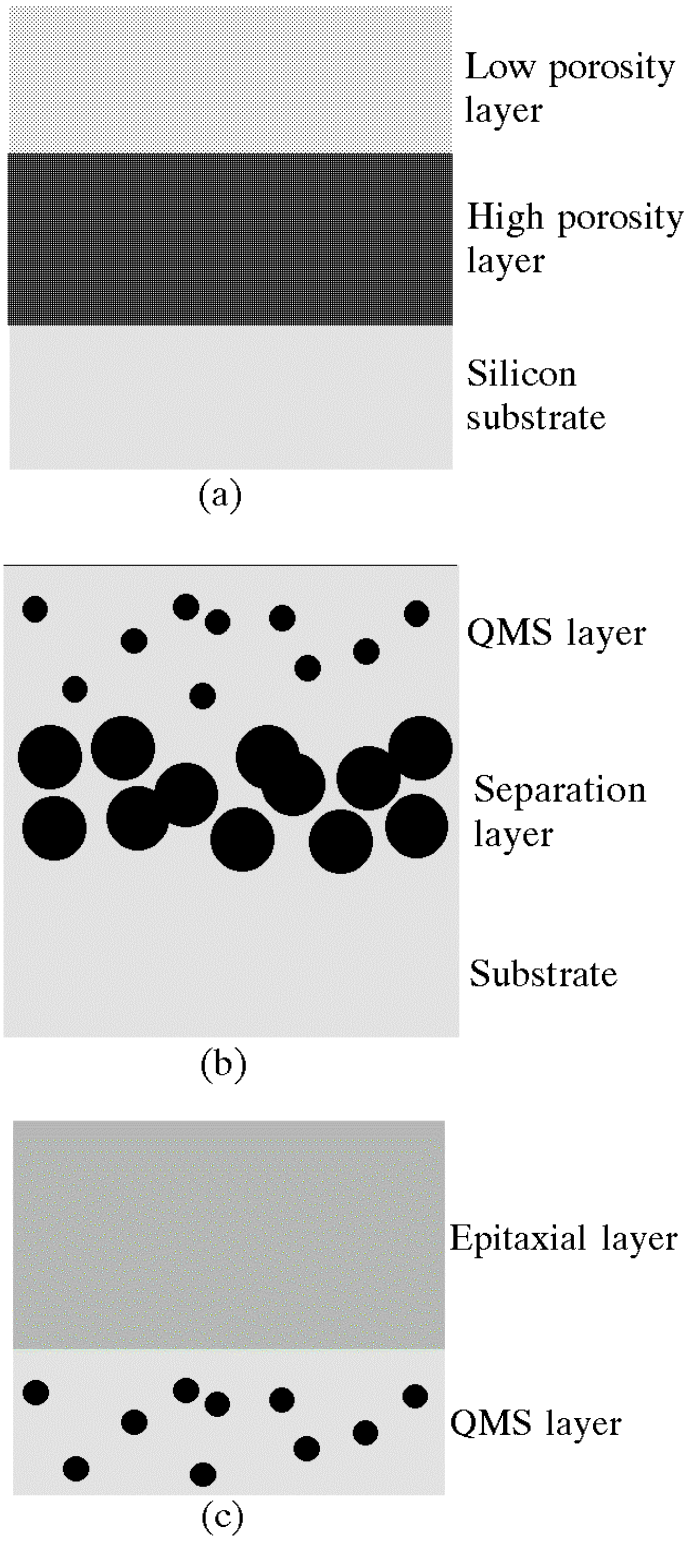

Figure 3: The QMS process. (a) The surface of the wafer is provided with a high porosity and a low porosity layer, (b) high temperature annealing leads to the formation of voids, (c)

following epi growth, the epilayer and QMS layer can be detached from the substrate.

It was also demonstrated that the voids in the QMS film contribute to light trapping in the cell by scattering weakly absorbed, long wavelength light. By increasing the size of the voids and optimising their density, further improvements in light trapping and cell efficiency are expected [36]. At Sony, a 12μm thick cell resulted in an efficiency of 12.5% for a 4cm^2 cell [34].

An interesting variation is to use the quasi monocrystalline film as the active layer of the cell, thus obviating the need for epitaxial growth [37]. A key issue with this approach will be the impact of the voids on recombination in the material. If the voids can somehow be passivated, this approach would appear to hold out significant potential.

3. Approaches based on macroporous silicon

The technology of macroporous silicon formation was developed by Lehmann et al. [38,39]. It is similar to that of porous silicon formation in that anodic etching in an HF containing solution is employed. However, the requirements are more stringent: a relatively lowly doped n type silicon wafer must be used, and the sample must be illuminated with short wavelength light from the rear side (so that it is absorbed before it reaches the other side of the sample), which is protected from etching. The sample is initially provided with a series of indentations (formed, for example, by photolithography and KOH etching) which form a regular array. Under these conditions, it is observed that the initial indentations etch to produce deep pores extending up to hundreds of microns into the sample. The remarkable features of this technology are the straightness of the pores for the case where a (100) oriented wafer is used, and the fact that etching only occurs at the pore tips. Thus, most of the sample remains unetched without any kind of protective layer being present. The mechanism responsible for this behaviour was worked out in detail by Lehmann. Holes photogenerated by the incident light diffuse to the front surface. Under anodic bias, the electric field around the pre-existing indentations attracts the holes. Thus, the holes reach the sample surface close to the bottom of an indentation and cause silicon dissolution there. The diameter of the pores can be varied to some extent by varying the illumination, which changes the current density. However, in order to obtain holes up to 10 microns in diameter, lowly doped silicon (>1 Ω-cm) must be used. For more heavily doped silicon samples, the range of stable pore diameters is in the nm range. The relationship between hole diameter and doping density for electrochemical and photoelectrochemical etching appears to be caused by the dependence of depletion region width on doping density [39].

Photoelectrochemical etching can be applied to solar cells by making use of the achievable variation in pore diameter [40]. This is illustrated in figure 4. The n type starting wafer is provided with a series of indentations which are spaced up to 10 μm apart. Etching under suitable conditions results in pores with a diameter of several microns extending into the wafer. When a suitable depth of 10-50 μm is reached, the etch current is increased to widen the pores to such an extent that they join, or almost join. This either detaches the top film from the substrate or results in a detachment layer which subsequently can be easily broken using a mechanical force. The substrate wafer can be re-used and will already have the required pattern of indents in it, so that photolithography need not be carried out again.

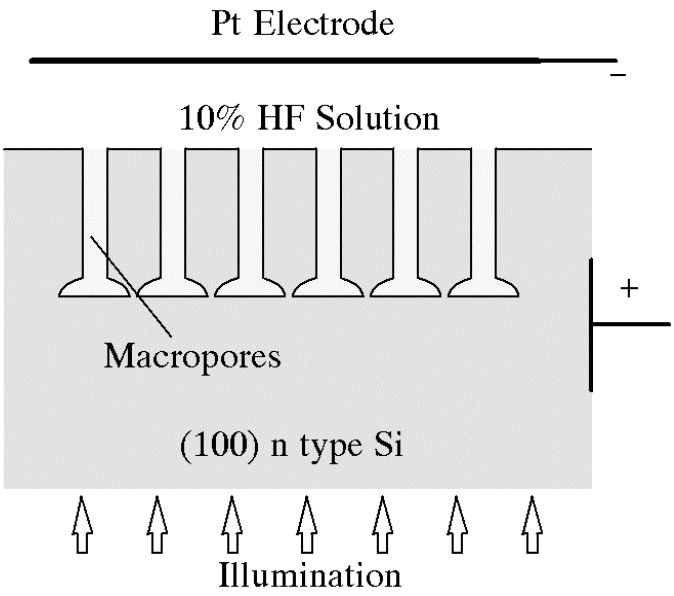

Figure 4: Application of macroporous silicon technology to the detachment of thin silicon films.

Recent investigations have shown that it is also possible to use fluoride containing salts in place of HF in the etching solution [41]. These solutions have a negligible dissolution rate of SiO_2, which would increase the flexibility of the process to some extent. However, while a cell processing sequence was proposed by Lehmann et al. [40] to date no solar cells have been reported.

4. Approaches based on alkaline etching of (110) silicon

Silicon wafers of (110) orientation have the property that two sets of {111} planes vertically intersect the wafer surface. This can be combined with the property of many alkaline etches, that they etch the Si {111} planes at a much slower rate than any other crystal planes. When this is done, it is possible to obtain trenches with vertical sidewalls in silicon. This technology has been known and reasonably well understood for several decades [42,43], and has found application particularly in the area of microelectromechanical systems (MEMS). If combined with dopant selective etching, it can also be used for the transfer of monocrystalline silicon layers.

A method of producing a thin interconnected film of silicon using the above technique has been developed at the Australian National University. Using KOH etching, the structure shown in fig. 5. is produced. A light phosphorus diffusion is made to typically 100Ω/square. The wafer is again immersed in KOH solution until the phosphorus diffusion at the bottom of the trenches has been etched through. Now, the wafer is electrochemically etched in an HF solution in the dark. Electrical contact is only made to the p type substrate. Under these conditions, the n diffusion will resist etching while the p type substrate will readily dissolve [44]. The etch current is kept sufficiently high to prevent the formation of porous silicon. This results in isotropic etching at the bottom of the trenches. Eventually, the cavities created at the bottom of each trench merge, resulting in the detachment of the top layer from the substrate.

Figure 6 shows the structure part-way through the electrochemical etching process and a section of a layer that was detached from the substrate. We have demonstrated the release of small area (1 cm^2) films using the above process. However, this process may be too complex for photovoltaic applications. Nevertheless, the process could find application in the area of MEMS.

5. The Smart Cut process

In the Smart Cut process [45-47], hydrogen ions are implanted into a silicon wafer to a depth of several microns. The implanted wafer is bonded to another silicon wafer and the assembly is heated to about 500^{o}C. This causes the silicon layer above the implanted region to split off. The substrate can

be re-used. The process is similar in its end result to the approaches based on porous silicon. However, because it requires high dose ion implantation it would appear to be inherently more expensive, and therefore less suited to photovoltaic applications.

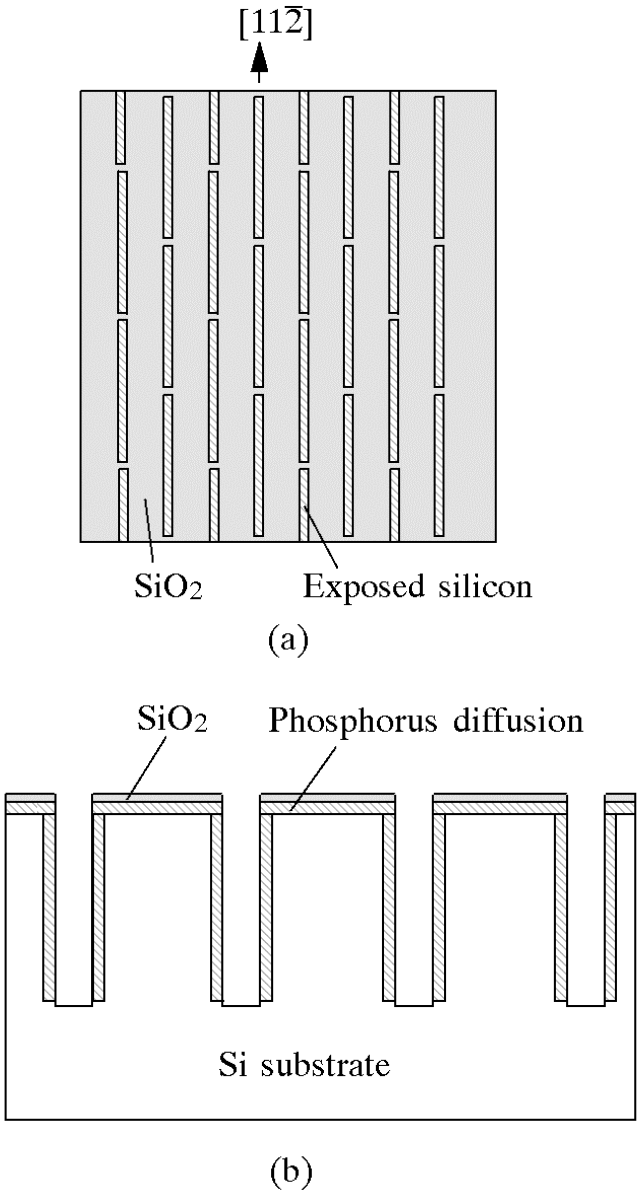

Figure 5: Transfer of silicon films using KOH etching. (a) top view of the pattern of stripes in the SiO2 layer for KOH etching. The stripes are typically 0.5mm long and spaced 20 μm apart, (b) cross section view of the structure just prior to electrochemical etching.

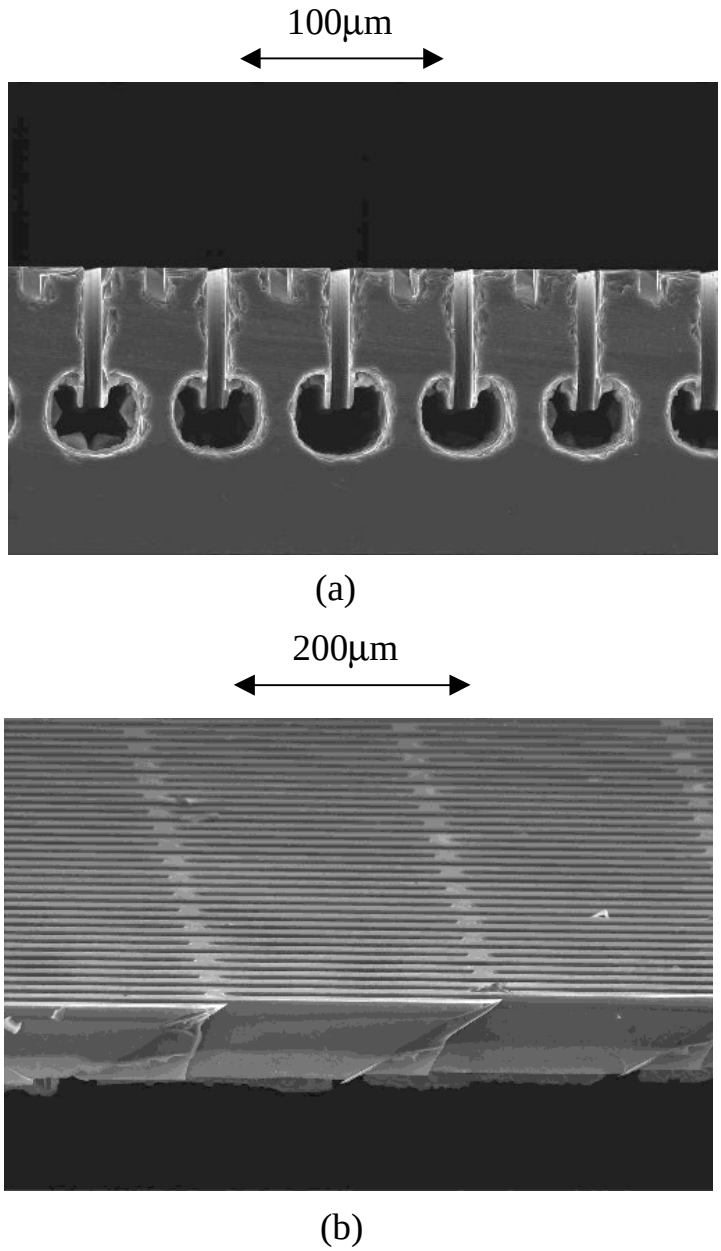

Figure 6: (a) cross section view of silicon layer part way through the electrochemical etching process, (b) a silicon layer detached from the substrate. The top side is smooth, while the rear (etched side) is highly textured (not visible in the picture).

6. Challenges for thin film Si cells produced by transfer approaches

The transfer approaches discussed above face several challenges that need to be addressed before they can become commercial reality for photovoltaic applications. One obvious issue is that of substrate re-usability. If a substrate is to be re-used 10 times and there is a 5% chance of loss of the substrate in each cycle (through breakage, for example) then the average substrate would only last 7.6 cycles rather than 10. Combining this with some realistic numbers for the amount of silicon consumed from the substrate in each cycle (30 μm), the minimum thickness of the wafer before it cannot be re-used any more (300 μm) and kerf loss due to ingot slicing (200 μm) leads to an average consumption of 105 μm of non-epi silicon per cell. This is still significantly less than the amount of silicon per cell in even a very advanced process using 200 μm thick wafers (400 μm). Nevertheless, it is not insignificant, and the economics depend quite sensitively on the probability of loss of substrate during a process cycle.

For non-epi approaches, the challenge is even more severe, since not only must the substrate physically survive a process cycle with a high probability, but its electronic quality must also remain intact. Since the wafer is usually taken through the full range of process steps, including metallisation, before the solar cell is separated, there would appear to be significant opportunity for metallic contamination and defect generation due to stresses resulting from thermal cycling etc. Thus, while conceptually very attractive, these approaches may prove too difficult to implement in a cost effective manner.

In order to keep the cost of epitaxial deposition low, it will be necessary to choose a technique with a high throughput rate and low materials consumption. LPE, CVD and IAD are all suitable candidates in this regard. High temperature CVD deposition, should allow high deposition rates of several microns per minute. Critical issues are likely to be the maintenance cost of the CVD system and the consumption of H_2 and the silicon containing gas. These considerations may exert a strong pressure for very thin silicon films, with a thickness of only 10-20 μm. For such films, the achievement of good surface passivation and light trapping will become extremely important. If LPE is used, gas and silicon consumption should be less of an issue than for CVD. The polycrystalline silicon feedstock used for Cz crystal growth can be used as the silicon source material. Very little H_2 gas is required, and the silicon utilisation is very good. However, LPE requires relatively high purity metals such as tin as the solvent. The cost of the pure metals is significant, and the process will only be economic if it is possible to keep the melt clean for a long period of time and prevent the loss of a substantial amount of melt during each growth cycle. For IAD, the most important considerations are the electronic quality of the epitaxial layers and the need for a relatively high vacuum, which will lead to lower throughput rates.

Finally, low cost cell processes need to be developed that allow production efficiencies of around 15% to be realised, so that these technologies can truly compete with wafer based silicon cells. This will be challenging, since efficiencies to date have been below the 15% mark, even on small area cells that were processed with high efficiency laboratory techniques. Nevertheless, there are no fundamental limitations here, and with time this goal should be realised. Indeed, modelling shows that efficiencies in excess of 20% can be theoretically realised for silicon films with a thickness of less than 20 μm [35].

Conclusion

Work in the last 5 years has demonstrated that films made using monocrystalline silicon transfer techniques are of excellent electronic quality, often display excellent light trapping features and can be processed into solar cells in a relatively straightforward manner, using the processes that are usually applied to solar cells made from silicon wafers. Monocrystalline silicon transfer techniques have therefore opened an exciting new avenue towards a low cost solar cell process.

Acknowledgements

The authors gratefully acknowledge the financial assistance for this work by Origin Energy Pty Ltd. and the Australian Research Council. The various valuable contributions of all members of the ANU Epilift group, both past and present, are gratefully acknowledged. 'Epilift' is a registered trademark.

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