Aspects of Silicon Solar Cells: Thin-Film Cells and LPCVD Silicon Nitride

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Declaration

This thesis is an account of research undertaken between April 1998 and July 2002 at The Centre for Sustainable Energy Systems, The Department of Engineering, Faculty of Engineering and Information Technology, The Australian National University, Canberra, Australia.

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and has not been submitted in whole or part for a degree in any university.

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Abstract

This thesis discusses the growth of thin-film silicon layers suitable for solar cells using liquid phase epitaxy and the behaviour of oxide/LPCVD silicon nitride stacks on silicon in a high temperature ambient.

The work on thin film cells is focussed on the characteristics of layers grown using liquid phase epitaxy. The morphology resulting from different seeding patterns, the transfer of dislocations to the epitaxial layer and the lifetime of layers grown using oxide compared with carbonised photoresist barrier layers are discussed. The second half of this work discusses boron doping of epitaxial layers. Simultaneous layer growth and boron doping is demonstrated, and shown to produce a 35μm thick layer with a back surface field approximately 3.5μm thick.

If an oxide/nitride stack is formed in the early stages of cell processing, then characteristics of the nitride may enable increased processing flexibility and hence the realisation of novel cell structures. An oxide/nitride stack on silicon also behaves as a good anti-reflection coating. The effects of a nitride deposited using low pressure chemical vapour deposition on the underlying wafer are discussed. With a thin oxide layer between the silicon and the silicon nitride, deposition is shown not to significantly alter effective lifetimes.

Heating an oxide/nitride stack on silicon is shown to result in a large drop in effective lifetimes. As long as at least a thin oxide is present, it is shown that a high temperature nitrogen anneal results in a reduction in surface passivation, but does not significantly affect bulk lifetime. The reduction in surface passivation is shown to be due to a loss of hydrogen from the silicon/silicon oxide interface and is characterised by an increase in J_{oe}. Higher temperatures, thinner oxides, thinner nitrides and longer anneal times are all shown to result in high J_{oe} values. A hydrogen loss model is introduced to explain the observations.

Various methods of hydrogen re-introduction and hence J_{oe} recovery are then discussed with an emphasis on high temperature forming gas anneals. The time necessary for successful J_{oe} recovery is shown to be primarily dependent on the nitride thickness and on the temperature of the nitrogen anneal. With a high temperature forming gas anneal, J_{oe} recovery after nitrogen anneals at both 900 and 1000°C and with an optimised anti-reflection coating is demonstrated for chemically polished wafers.

Finally the effects of oxide/nitride stacks and high temperature anneals in both nitrogen and forming gas are discussed for a variety of wafers. The optimal emitter sheet resistance is shown to be independent of nitrogen anneal temperature. With textured wafers, recovery of J_{oe} values after a high temperature nitrogen anneal is demonstrated for wafers with a thick oxide, but not for wafers with a thin oxide. This is shown to be due to a lack of surface passivation at the silicon/oxide interface.

List of Acronyms and Symbols

AIC	Aluminium Induced Crystallisation
AR	Anti-Reflection
ARC	Anti-Reflection Coating
a-Si	amorphous Silicon (no crystal structure)
BSF	Back Surface Field
BSR	Back Side (or Surface) Reflector
CVD	Chemical Vapour Deposition
APCVD	Atmospheric Pressure CVD
cat-CVD	Catalytic CVD
CC CVD	Closed Chamber CVD
EBEP CVD	Electron Beam Excited Plasma
ECR CVD	Electron Cyclotron Resonance CVD
ECR PACVD	Electron Cyclotron Resonance Plasma Assisted CVD
HR CVD	Hydrogen Radical CVD
HWCVD	Hot Wire CVD
LPCVD	Low Pressure CVD
PACVD	Plasma Assisted CVD (also called Plasma CVD)
PCVD	Plasma CVD (also called PECVD and PACVD)
PECVD	Plasma Enhanced CVD (also called plasma CVD)
remote PECVD	Plasma CVD with a remote plasma source
RF PECVD	Radio Frequency Plasma Enhanced CVD
RTCVD	Rapid Thermal CVD
SA CVD	Sub-atmospheric CVD
Cz	Czcholaski grown silicon
Dessis	a 2 dimensional computer program for solar cell simulation
DLARC	Double Layer Anti-Reflection Coating
EBIC	Electron Beam Induced Current
efficiency	(for solar cells) output energy/input energy
EFG	Edge-defined Film-fed Growth
ELO	Epitaxial Layer Overgrowth
EQE	External Quantum Efficiency
EWT	Emitter Wrap Through
FF	Fill Factor, equal to $I_{sc}V_{oc}/P_{max}$
FGA	Forming Gas (5% hydrogen in argon) Anneal
FZ	Float Zone
IAD	Ion Assisted Deposition
IC	Integrated Circuit
I_{sc}	Short Circuit Current
ITO	Indium Tin Oxide, commonly used as an anti-reflection coating

i-type	intrinsic (undoped)
IQE	Internal Quantum Efficiency
J_{oe}	emitter saturation current density
J_{sc}	short circuit current density
LBL	Layer-By-Layer
L_{diff}	diffusion length
LPE	Liquid Phase Epitaxy
L/W	the ratio of diffusion length to wafer width
mc-Si	multi-crystalline Silicon, the non-crystalline material with the largest grains
MG-Si	Metallurgical Grade Silicon
μc-Si	micro-crystalline silicon, grain sizes smaller than poly-crystalline silicon, but larger than nano-crystalline silicon
MIRHP	Microwave Induced Remote Hydrogen Passivation
n^+	heavily doped n-type
n^{++}	very heavily doped n-type
n-type	doped with atoms with single electron in their valance band, eg. phosphorous, arsenic or antimony
nc-Si	nano-crystalline silicon
ONO	a triple stack; SiO_2, SiN_x, SiO_2
p^+	heavily doped p-type
p^{++}	very heavily doped p-type
PC1D	a 1 dimensional computer programme for solar cell performance simulation [32]
P_{max}	the maximum operating power output
poly-Si	poly-crystalline Silicon, grain sizes in between multi and micro-crystalline silicon
p-type	doped with atoms with a single hole in their valance band, eg boron, aluminium or gallium
QMS	Quasi Mono-crystalline Silicon, mono crystalline silicon that has been electrochemically etched to form porous silicon.
$R_{\square}$	sheet resistance, typically measured after a diffusion or drive-in step using a 4-point probe.
PRTP	Pulsed Rapid Thermal Processing
RGS	Ribbon Grown onSsubstrate
RTP	Rapid Thermal Process
sc-Si	single (or mono) crystalline Silicon
SEM	Scanning Electron Microscope
S_{front}	front surface recombination velocity
Si:H	Hdrogenated Silicon (usually amorphous or very small grained)
SiO_2	Slicon Oxide
SiN	Silicon Nitride
SOI	Silicon On Insulator
SPC	Solid Phase Crystallisation
S_{rear}	rear surface recombination velocity
SRH	Schottky-Read-Hall
SRV	Surface Recombination Velocity
SSP	Silicon Sheets from Powder
τ	lifetime

τ_{eff}	effective lifetime
UHV sputtering	Utra-High Vacuum sputtering
UMG-Si	Ugraded Metallurgical Grade Silicon
VHF-GD	Very-High Frequency Glow Discharge
V_{oc}	open circuit voltage
ZMR	Zone Melt Recrystallisation

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