SILICON SOLAR CELLS FOR TANDEM HIGH-EFFICIENCY SOLAR CELLS (VHESC)

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ABSTRACT: *Development of high efficiency solar cells is a crucial objective to make solar energy affordable in the long run. The VHESC program initiated by the Defense Advanced Research Projects Agency program to address the need of increasing solar cell efficiency is one such development. The VHESC program comprises around 20 contributors including ANU, and has adopted a multi-junction concentrator tandem approach. ANU's involvement in this program is to design and develop high efficiency silicon solar cells, which are to be used in conjunction with other high-band gap and low-band gap solar cells, for 50% efficient multi-junction solar cells. The VHESC program is steadily progressing and to date it has reported to develop solar cell device results summing to 42.9% efficiency. In this paper we report current progress towards the 2nd milestone of targeted efficiency for VHESC program. We also discuss various design considerations, characterization and testing of completed solar cells. Additionally, we describe experimental work to analyse and rectify problems encountered in developing the 2.5 x 8* mm^2 *silicon solar cells.*

1. INTRODUCTION

Solar cell efficiencies are improving with time. The highest efficiency reported for a single-junction silicon solar cell under non-concentrated light is about 24%, while for multiple-junction GaInP/GaAs/Ge device it is around 32% (M. Green *et al.* 2008). To further increase efficiency, a novel device structure is required. The VHESC program sponsored by DARPA aims to use the novel architecture of six-junction tandem solar cells to reach the efficiency goal of 50% and more (A. Barnett *et al.* 2006; C. Honsberg *et al.* 2006; A. Barnett *et al.* 2007). As silicon is one of the solar cells in the six-junction tandem approach, the design and development of silicon solar cells will have to be based on novel designs and fabrication approaches.

In a six-junction tandem solar cell as shown in figure 1.1, individual solar cells will be arranged so that each solar cell absorbs the appropriate slice of the solar spectrum. The eventual goal of six-junction tandem solar cell package is to achieve the combined efficiency of >50% under 20suns illumination. Silicon is one of the cells in the tandem structure, and absorbs energy of 1.1 to 1.42 eV. The role of the silicon cell is to convert 7% of the light incident on the tandem structure into electricity. Other cells in the stack contribute the balance of the electricity. Key design parameters for the silicon cells are that it should have dimensions of 2.5x8mm^2 and it needs to transfer light energy of less than 1.1eV to the underlying solar cells.

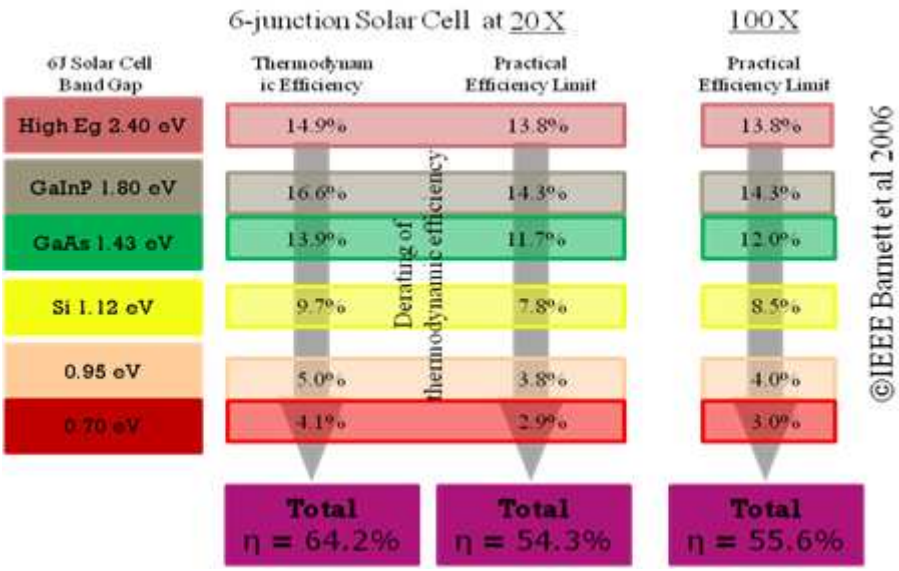

Fig 1.1 Band Gap Architecture of Six-Junction Tandem Stack

2. CELL STRUCTURES AND DESIGN CONSIDERATIONS

The external dimensions of the silicon solar cell are 2.5mm in width and 8mm in length. Cells were fabricated using 450μm thick <100> p-type float-zone 1Ωcm wafers. The cells have an active n-type emitter region on both front and back of cell with the dimension of 6.5 x 2.5mm^2. Metal contacts are made to both sides of the cell. The n-contact to the external world is on sunward side and the P-contact is on the back of cell. Metal contacts are designed with a spacing of 1.9mm in the lateral direction and 5.5 mm in the lengthwise direction as shown in the figure 1. Multiple cells are processed simultaneously on each wafer until the metallization step is completed, at which time they are diced out of the wafer to form individual solar cells.

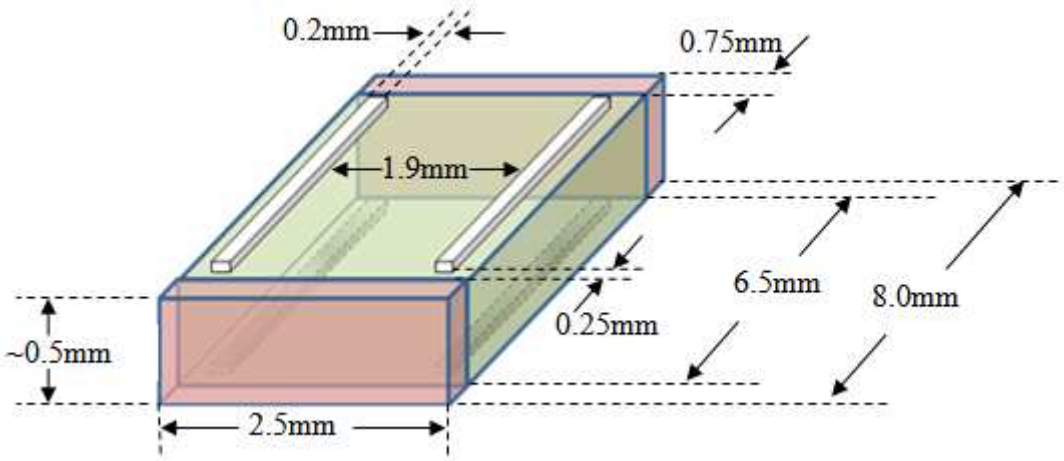

Fig 2.1: Structure and Dimension of Silicon Solar Cell

2.1 Illumination

Light of energy less than 1.42ev will be transferred to the silicon after having most of the light directed to high-band gap materials while light of energy less than 1.1ev will need to be passed on to underlying low-band gap material cells. Thus texturing and back surface reflection (BSR) cannot be used. Based on the modelling, to achieve reasonable conversion efficiency especially in the weak absorption range of 875 to 1100nm silicon cell thickness should be from 0.5 to 2mm.

2.2 Recombination

Recombination in such small solar cell can be a significant matter for cell efficiency. Surface recombination will be minimised by thermal oxidation. To prevent edge recombination cells are processed in the host wafer before dicing out to form individual cells after the last processing step. Additionally, the cell's emitter region is kept at least 0.75mm away from the edge of the cell. Contact recombination is suppressed by maintaining metal contact to the silicon less than 1% of the total surface area.

2.3 Anti-reflection Coating

A combination of oxide and nitride layers is used for anti-reflection coating. To target for reflection loss of less than 1% in air and 3% under encapsulation optimisation of oxide and nitride layer thickness will be addressed carefully.

2.4 Internal Quantum Efficiency

To achieve the internal quantum efficiency of greater than 90% the diffusion length is kept at least 3 times more than the cell thickness.

2.5 Resistive Losses

Modelling predicts that 500μm thick wafer will absorbs 87% of light in the wavelength range of 875 to 1100nm in the top half of the cell. If a cell with bifacial emitter is used, current sharing will minimise the resistive losses partially but not significantly. However, electron current generated at the rear of diffused emitter will be small.

2.6 Resistive Losses

Electron transport resistance losses are of more concern than those of holes since the sheet resistance (20Ω/□) of 500μm thick wafer with resistivity of 1Ωcm is much less than the sheet resistance of the n-type emitter diffusion. To achieve the target resistive loss of less than 5%, the best arrangement of n-contacts is to be placed at both edges and both ends of the top active emitter region, facing towards the light. N-contacts will need to be at the top of the cell since most of the light generated will be close to the top surface, thus minimising transport resistance. Similar arrangements also apply to p-contacts at the bottom of the cell.

3. TARGETED CELL EFFICIENCY AND CELL MODELLING

3.1 Cell Efficiency

Under 20suns concentration, the incident power density of the light on the entire six-junction tandem stack including silicon is 20W/cm$^{2.}$ After the light spectrum passes the high-band gap material solar cells, the incident power density on silicon becomes 7.2W/cm^2 in the wavelength range from 875 to 1100nm. The light incident on the silicon is in the form of 1.9mm diameter spot, which has the area of 0.0284cm^2. Silicon solar cell has the input sun power of 0.204W. For the current design discussed above, the efficiency targeted is 5.2% and thus the output cell power has become 0.0106W. Using the equation for the targeted efficiency of 5.2%, the output cell power can be achieved by short-circuit current, Jsc of 6mA, open-circuit voltage, Voc of 630mA and fill-factor, FF of 78% under 20suns concentration.

3.2 Modelling to Predict the Cell Performance

Modelling was made using PC1D to predict the expected current and voltage as well as IQE of 2.5x6.5mm silicon solar cell (D. Clugston & P. Basore, 1997). Major parameters used for modelling include active area of 15mm; one-sun intensity; bifacial emitter diffusion; and heavy n+ and p+ diffusions. Modelling was also done without GaAs being covered on top of silicon. Modelling predicts short-circuit current of around 4.17mA and open-circuit voltage of 630mV (fig 3.1) can be achieved.

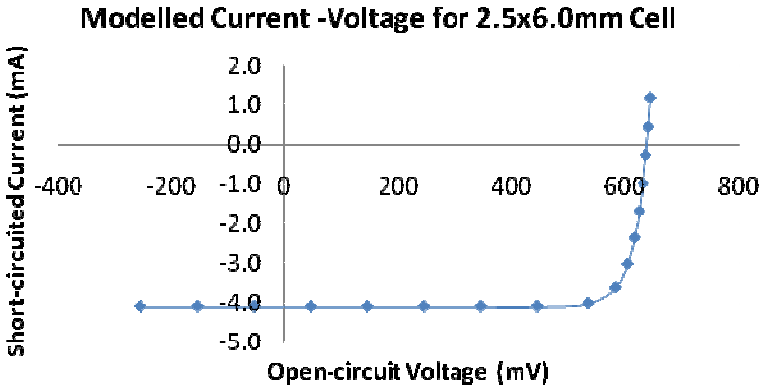

Fig 3.1: Modelled Current-Voltage by PC1D

Since light incident on the silicon solar cell will have been rejected by the GaAs and other higher band-gap materials, most of the light silicon absorbs will be in the range of 875nm to 1100nm. Modelling predicts that internal quantum efficiency of up to 90% can be achieved in the desired range (fig 3.2).

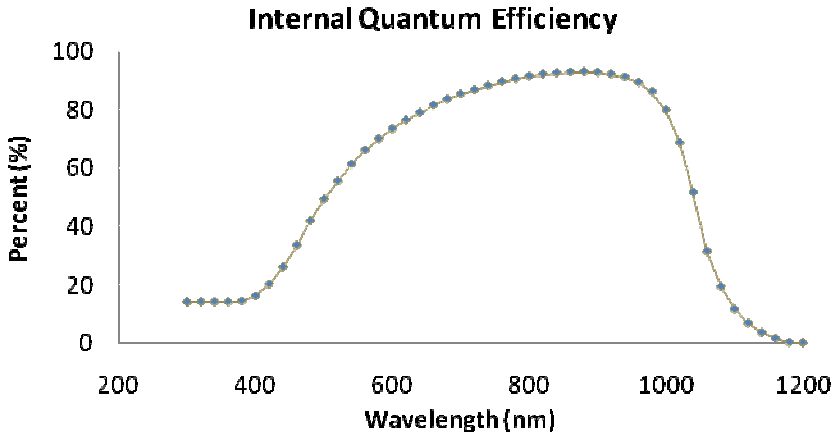

Fig 3.2: Modelled Internal Quantum Efficiency by PC1D

4. CELL FABRICATION AND CHARACTERISATIONS

4.1 Cells Fabrication

Cells were fabricated using standard silicon process techniques, as shown in the table 2. Completed cells were diced out from wafer to form individual cells. Cells were tested by current-voltage flash tester (Keogh *et al.* 2004) under 1sun illumination intensity without having the light being filtered by GaAs.

Table 2: Cell Making Process

	Process	Details
1.	Si Etch	Etch in HF:HNO_3
2.	Cell Formation	Laser machining to form grooves TMAH etch Cleaning in standard solution
3.	Emitter Formation	Oxidise. Deposit nitride as a diffusion barrier Open a window for emitter diffusion
4.	Emitter Diffusion	Light phosphorous diffusion (~100Ω/□) Phosphorous glass deglaze
5.	Passivation + ARC	Growing thin oxide layer Depositing antireflection layer
6.	n++ Contacts Formation	Open windows for n++ contacts
7.	Phosphorous Diffusion	Heavy phosphorous diffusion (~10Ω/□) Deglase phosphorous glass
8.	Boron Barrier Oxide	Dry-Wet-Dry oxidation (~100nm)

9. p+ Contacts Formation	Open windows for n++ contacts 10% HF etch to remove residual oxide
10. Boron Diffusion	Heavy boron diffusion (~20Ω/□) Deglase boron glass Stripping all barrier oxide
11. Hydrogenation	FGA annealing at 400°C for 120mins
12. Metallisation	Evaporating Cr/Pd/Ag metal stacks Sintering at 400°C for 30mins
13. Dicing	To form individual cells out of host wafer
14. Testing	IV testing under 1 sun illumination

4.2 Characterisation of 2.5x8mm Silicon Solar Cell

The early batch of cells fabricated was found to have serious shunting problems as shown in fig 4.1. It is important to solve the shunt resistance problem to reach the high efficiency potential of the solar cell.

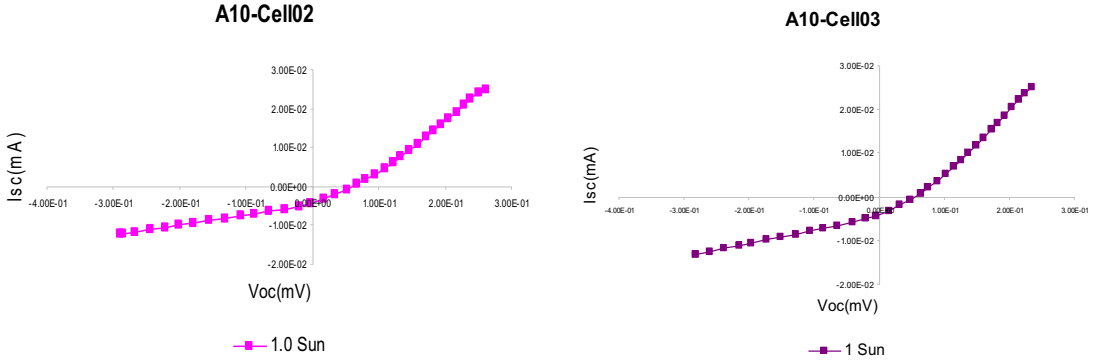

Fig 4.1: Shuting problems associated with the cells fabricated in the early batch

Possible shunting routes for silicon solar cells, having baficial emitters surrounded by passsivation oxide and ARC with n++ contacts on top of the cell and p+ contacts at the bottom are shown in the figure 4.2. Possible scenarios causing the shunting issues are broken down into

- #1, Shunting caused by pinholes
- #2, Shunting caused by insufficient barrier oxide thickness for boron diffusion
- #3, Shunting originated by insufficient diffusion drive-in
- #4, Shunting induced by phosphorous and boron diffusions direct overlap.

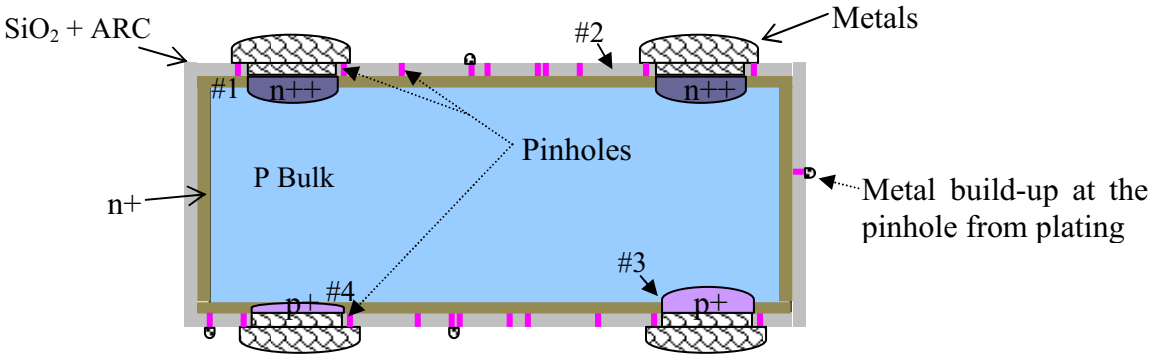

Fig 4.2: Possible shunting paths for 2.5x8mm silicon solar cells

4.2.1 Pinhole Short, #1

The first scenario, #1 represents that a pinhole can easily lead to direct shunting between the phosphorous emitter and base contact after metallisation. Typical pinholes on the solar cells after metallisation are shown in figure 4.2. These pinholes are associated with the particular LPCVD SiN layer deposited using our equipment, and are not regarded as generic (K. Weber & A. Blakers, 2005).

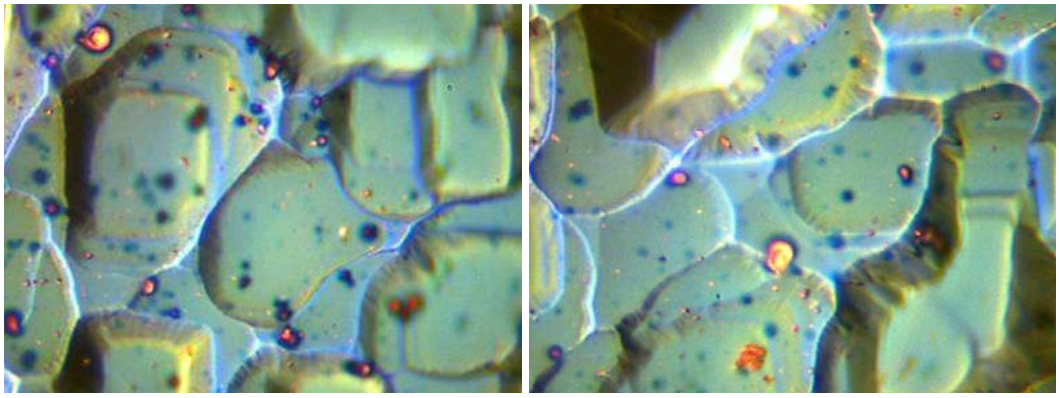

Fig 4.3 Pinholes on the cell after metallisation

To find out if these pinholes can cause shunting problems, a method to isolate the shunted regions from the active cell region was used (M. Abbott *et al.* 2007; J. Arumughan et al. 2005). A group of cells was fabricated using the same processing sequence, as shown in table 2 but without boron diffusion to eliminate possible shuntings induced by boron diffusion and completed cells were performed a junction isolation. Laser machining was used to scribe a trench on each side of the solar cell, isolating the two p- and n-contacts totally. The first group of shunted cells included a very deep trench by laser scribing while the second group of cell was made with several laser scribings with different trench depths to observe any gradual improvements for shunting problems with respect to trench depths.

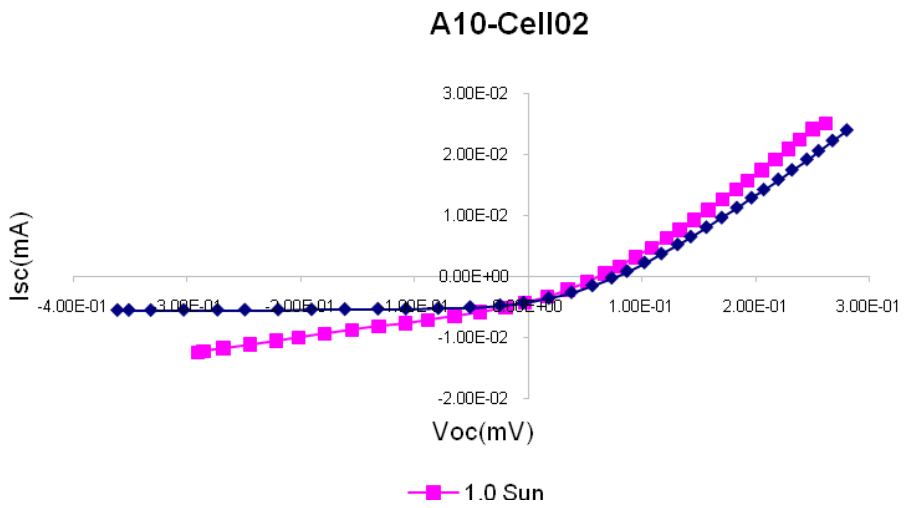

Fig 4.4: Behaviour of Shunt Cell before and after Junction Isolation

After the deep laser scribe, the first group cells were measured in the current-voltage tester. The cells previously shunted prior to the deep laser scribe have indeed recovered from the shunt completely, as shown in figure 4.4. A second group of cells were also observed to gradual improvements eventually leading to free of shunting with the varied depth of trenches made by laser scribe, as shown in figure 4.5. Based on this experiment, it can conclude that pinhole shunting can readily cause the shunting problems, especially in bifacial solar cells.

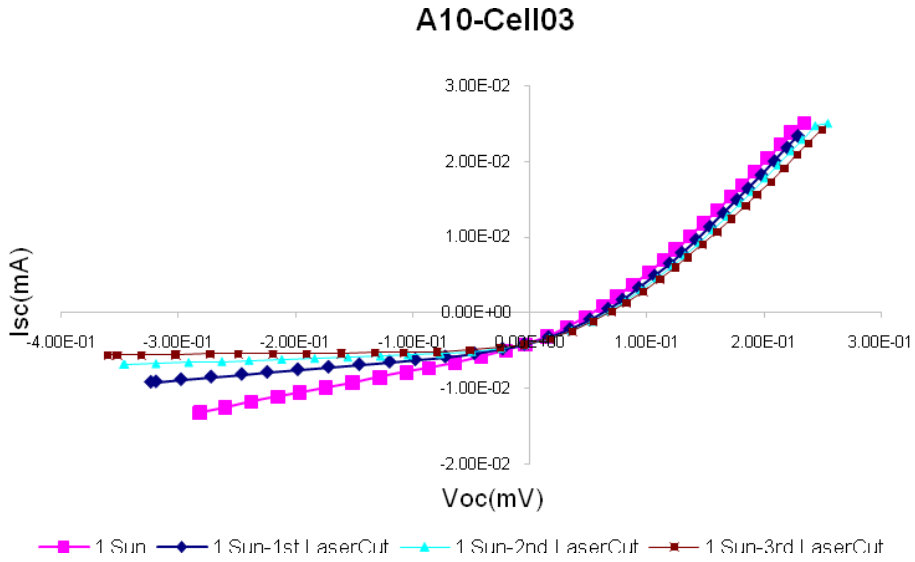

Fig 4.5: Behaviours of Shunt Cell after Junction Isolation with Varied Trench Depths

4.2.2 Shunting Due to Insufficient Oxide Thickness to Resist Boron Diffusion, #2

The second possible shunting scenario, #2 represents that insufficient oxide thickness to resist heavy boron diffusion could lead to a direct junction shunting between heavy

phosphorous and heavy boron diffusions. Due to the required fabrication sequence of high-efficieny bifacial solar cells, processing of heavy phosphorous and boron diffusions have to be done one step after another. Following on from the heavy phosphorous diffusion, a thick oxide was grown to prevent subsequent boron diffusion entering into phosphorous region. Boron contact windows were then made and TMAH etchant was used to strip emitter phosphorous diffusion from the contact windows. Since TMAH etches the oxide layer slowly, even a relatively thin layer of oxide film coated on the contact windows can prevent TMAH etching the phosphorous emitter. Thus the oxide film needs to be stripped properly to enable TMAH etching of the phosphorous emitter. However, prolonged etching of oxide film from the boron contact windows could also thin down the thick oxide, grown on the other side of the cell (the function of which is to prevent the subsequent boron diffusion entering into phosphorous contact diffusion). An experiment was carried out to find the optimum oxide thickness to resist the heavy boron diffusion by first growing varied oxide thickness ranging from 60 to 150nm on different wafers. Wafers with different oxide thicknesses were then placed in the furnace for heavy boron diffusion. Post-boron diffused wafers were then etched in 10% HF solution to remove all oxides and sheet resistances were measured. Data has shown that oxide thickness of 100nm or more can resist the heavy boron diffusion. Shunting caused by boron diffusion entering into phosphorous diffusion due to insufficient oxide thickness can be prevented by growing the optimum oxide thickness of 100nm or more to resist boron diffusion and controlling the etch time on oxide films.

4.2.3 Shuting due to Insufficient Diffusion Drive-In, #3

Scenario #3 represents that if the diffusion drive-in is insufficient following the emitter diffusion, it can also create the shunted regions. Guo reported that a longer diffusion drive-in is critical to avoid shunting problems in the case of fabricating high-efficiency interdigitated back contact solar cells (J. Guo *et al.* 2003; J. Guo *et al.* 2006). To find out if insufficient diffusion drive-in has a contribution to low shunt resistance, wafers were split into two groups – group A and group B. Cells from group A were fabricated using the same processing sequence highlighted earlier but without the drive-in step after the emitter phosphorous diffusion. Group B cells were fabricated using exactly the processing sequence as the first group but with 60mins of drive-in after emitter phosphorous diffusion. After all processings, cells were tested for current-voltage. Group A cells tested present the severe shunting problems with no current-voltage curve can be seen. Cells from group B with diffusion drive-in has seen a significant improvement in the current-voltage curve as shown in figure 4.6. Hence insufficient drive-in could contribute to the shunt resistance issues in solar cells. However, the I-V curves indicate that there are some other factors still causing the shunting since the cell does not exhibit the full potential of expected IV behaviour and efficiency as compared to modelling results.

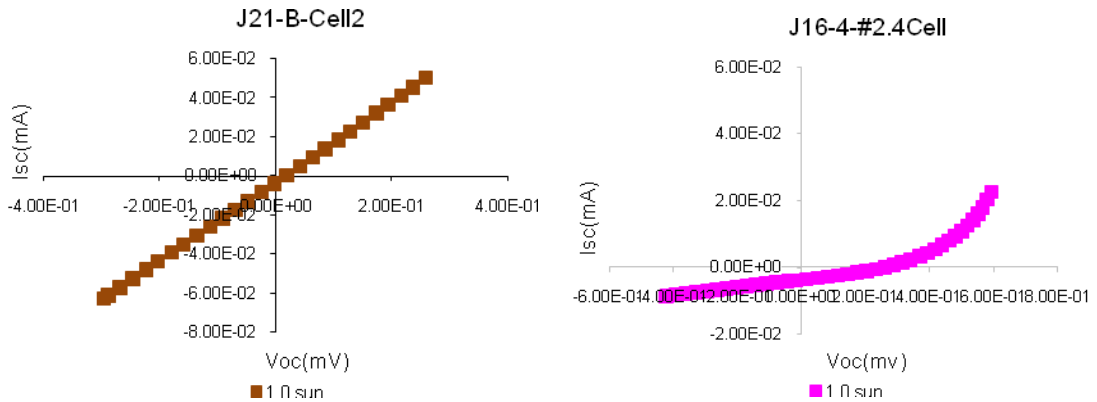

Fig 4.6: Current-voltage curves for cells without or without diffusion dirve-in

4.2.4 Shuting due to Diffusions Overlap, #4

A fourth possible scenario, #4, represents the direct overlap of phosphorous diffusion and boron diffusion, inducing the shunt. The problem of direct diffusions overlap could be due to the remain of phosphorous emitter caused by insufficient etching from the p+ contact windows prior to heavy boron diffusion. Since the cells have bifacial emitters, a proper etching has to be introduced to remove phosphorous emitter diffusion after the formation of p+ contact windows to prevent a direct diffusions overlap. Dry etching was used to remove phosphorous diffusion from the boron contact windows. However, completed cells after IV testing still have shunting issues. Thus, wet chemical etching using TMAH etchant in addition to dry etching to remove phosphorous diffusion was incorporated and completed cells were tested for current-voltage under 1sun concentration. Current-voltage data for cells after inorporating wet chemical etching to remove phosphorous emitter diffusion from the p+ contact windows was observed with completely free from shunting, as shown in figure 4.7.

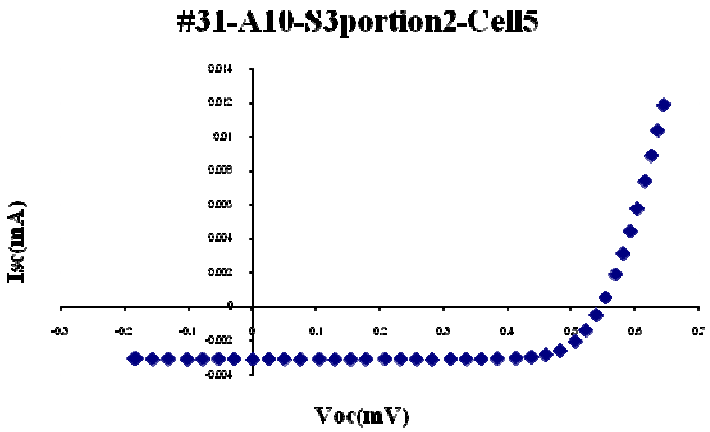

Fig 4.7: Current-voltage curve for the cell after incorporating wet chemical etch

The values of the open-circuit voltage, short-circuit current and fill factor for cells tested after using the wet chemical etching to remove emitter phosphorous diffusion was shown in table 3.

Table 3: IV Data for Cell Tested under 1sun Illumination

Cell#	Intensity	Voc(mV)	Isc(mA)	FF(%)
1	1 sun	552	3.21	78.11
2	1 sun	550	3.18	78.84
3	1 sun	549	3.16	78.36

5. CONCLUSION

Early batch of 2.5x8mm^2 silicon solar cells fabricated were associated with shunting problems. Shunting could be caused by four scenarios - pinhole short, insufficient oxide thickness to resist boron diffusion, insufficient post diffusion drive-in and direct duffusion overlap due to residual emitter phosphorous. These four scenarios have been identified and experimented to have caused the shunting problems, affecting the expected efficiency potentials in 2.5x8mm^2 silicon solar cells.

Cells fabricated after rectifying the above problems demonstrate the absence of shunts and a good fill factor. However, the open circuit voltage and current are low compared with the results expected from the modelling due to process issues. The possible root causes of low open-circuit voltage and short-circuit current have been characterised and identified (N. Zin *et al.* 2008). We believe that subsequent fabrication of 2.5x8mm^2 silicon solar cells could lead to sharply increased cell efficiency.

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