Annealing temperature dependence of capacitance-voltage characteristics in Ge-nanocrystal-based nonvolatile memory structures

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The annealing temperature (T_A) dependence of capacitance-voltage (C-V) characteristics has been studied in metal-oxide-semiconductor structures containing Ge nanocrystals (NCs) produced by ion implantation and annealing. These structures are of interest for application as nonvolatile memory and T_A is shown to have a strong influence on the C-V hysteresis. This behavior is shown to be correlated with structural changes of the Ge NCs which have been characterized by synchrotron-radiation photoemission spectroscopy. Specifically, well-defined C-V characteristics with large hysteresis were found only for annealing temperatures greater than 950 °C where Ge nanocrystals are known to form. In this temperature regime, transmission electron microcopy and energy dispersive x-ray spectroscopy demonstrate the existence of regularly arranged Ge NCs of approximately 3–5 nm diameter located around 6.7 nm from the interface. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2168249]

Over the past decade Si and Ge nanocrystals (NCs) embedded in insulating host materials have been the subject of intensive investigation as potential materials for electronic and optoelectronic device applications.[1,2] One of the most exciting such applications is as nonvolatile memory (NVM) and the demonstration of nonvolatile NC memory operation at room temperature has further stimulated the interest in such materials.[3,4] Indeed, several research groups have successfully fabricated high-quality NVM devices by employing Si or Ge NCs but each study shows different NVM characteristics without a detailed explanation for how the characteristics depend on the physical properties of the materials or the relative role of NCs and/or defects.

In principle, Ge NCs have greater potential than Si NCs to improve the NVM function because of their smaller energy band gap.[5] Quantum confinement effects should also be greater in Ge than in Si because of its smaller electron and hole effective masses and larger dielectric constant.[6] Charge storage in Ge–NC-based metal-oxide-semiconductor (MOS) structures is influenced by several mechanisms including quantum confinement/Coulomb blockade effects, and interface/defect states.[4,7] A number of groups have published reports on the structural properties of Ge NCs,[8,9] with the most detailed[9] providing important insight into the effect of annealing on the evolution of Ge nanocrystals. However, it is very important to investigate such behavior in the context of the present study, especially in relation to the influence of the SiO_2/Si interface and the SiO_2/metal contact in MOS structures which may directly affect the NVM characteristics.

This letter reports on a detailed study of the effect of annealing on the formation of Ge nanocrystals and the development of well-defined capacitance-voltage (C-V) characteristics in MOS structures containing Ge NCs. This is undertaken by employing several experimental techniques, including C-V, transmission electron microscopy (TEM), synchrotron-radiation photoemission spectroscopy (SRPES), and energy dispersive x-ray spectroscopy (EDS).

SiO_2 layers with 30 nm thickness were grown on n-type (100) Si substrates in a conventional furnace. The SiO_2 layer was implanted with 30 keV Ge_2^- to nominal fluences of 5.0×10^{15} and 1.0×10^{16} Ge cm^{-2} at room temperature and subsequently annealed at temperatures in the range from 800 to 1050 °C for 10 min in an Ar atmosphere. The peak excess-Ge concentration for these implants was calculated,

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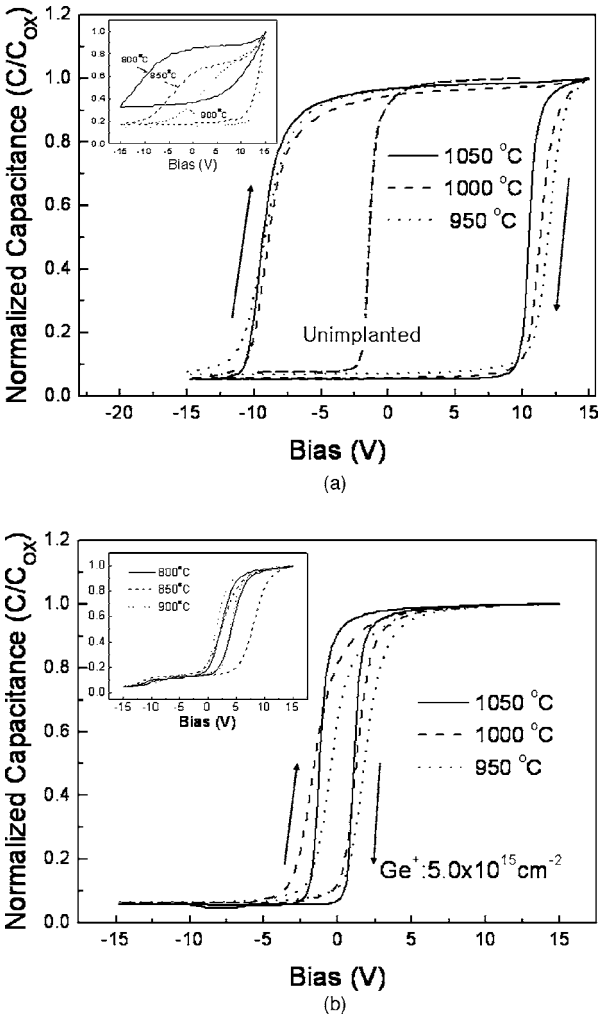

FIG. 1. Annealing temperature dependence of *C-V* hysteresis loops for MOS structures with oxides implanted with Ge ions to fluences of (a) 1.0×10^{16} (b) 5.0×10^{15} cm^{-2}. The *C-V* curve of an unimplanted sample is included for reference.

from TRIM simulation, to be around 6% and 11%, respectively.[10]

The density and size of Ge NCs were investigated by TEM and depth profile of Ge atoms was evaluated by EDS. To investigate the chemical structures of the surface region, SRPES measurements were carried out at the 7B1 beamline of Pohang Accelerator Laboratory. The SRPES data were taken at normal emission angle: 0° with 170 eV photons. Al electrodes with a diameter of 300 μm were deposited on the samples in vacuum for *C-V* measurements, which were carried out at 300 K by using a Boonton 7200 capacitor meter to study the memory effects from Ge NCs in MOS capacitors.

Figure 1 compares the *C-V* hysteresis loops of MOS structures with oxides implanted with Ge ions to fluences of 1×10^{16} and 5.0×10^{15} cm^{-2} and annealed at various temperatures. The hysteresis in the *C-V* curves can be attributed to the reversible storage of holes or electrons in the NCs based on quantum confinement and/or in the defect states at their interfaces with the SiO_2 matrix.[11] If the stored charge is stable, the shift in the flatband voltage produces a corresponding shift in the threshold voltage,[12] showing ideal hysteresis behavior, as shown for annealing temperatures (T_A)

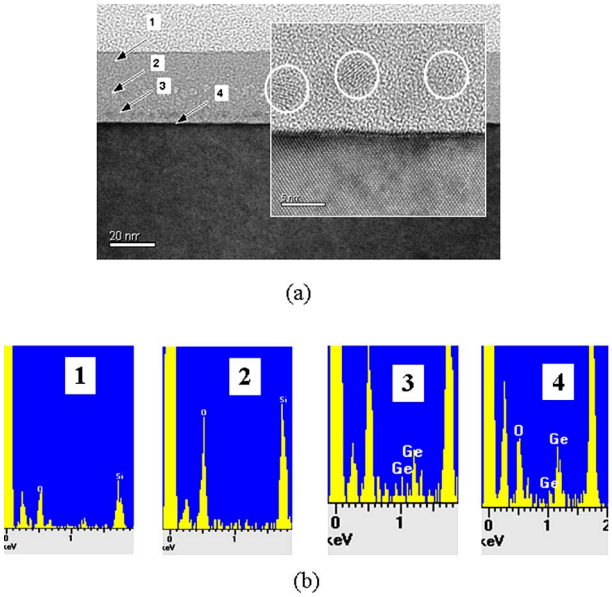

FIG. 2. (a) Cross-sectional TEM images and (b) EDS spectra for Ge implanted SiO_2 after annealing at 950 °C for 10 min. The implant fluence is 1.0×10^{16} cm^{-2} and Ge NCs are indicated by circles.

$\geqslant$950 °C in Figs. 1(a) and 1(b) In some cases, oxides and SiO_2/Si or SiO_2/metal interfaces contain unstable charges that can be influenced by the applied voltage. In this case, the threshold voltage itself depends on the gate voltage. The *C-V* curve is then distorted,[12] as shown at lower T_A's in the insets in Figs. 1(a) and 1(b).

Figure 2 shows the cross-sectional TEM images and EDS signals of a 30 nm oxide implanted with Ge ions to a fluence of 1×10^{16} cm^{-2} and subsequently annealed at 950 °C. Figure 2(a) shows an array of dark spots indicating Ge NCs along Si/SiO_2 interface. The higher-resolution image confirms the presence of Ge NCs of approximately 3–4 nm in diameter, as indicated by circles in the inset. The average distance from the Si substrate to the Ge NC layer is estimated to be about 6.7 nm and the nanocrystal density is calculated as 2×10^{12} cm^{-2} from plane-view TEM images.

Figure 2(b) shows the EDS spectra from different depths in the direction from the SiO_2 surface to Si substrate. The analysis reveals only low Ge concentrations in the near-surface region of the sample and in the middle of SiO_2 layer [as indicated by 1 and 2 in Fig. 2(a)] but shows a high concentration of Ge at positions near the Ge NC layer and the SiO_2/Si interface [as indicated by 3 and 4 in Fig. 2(a)]. It is also evident that the peak ratio of Ge to O in the EDS spectra increases in the direction toward the Si/SiO_2 interface. These results are consistent with the fact that ion-implantated Ge has diffused during annealing and accumulated at the Si/SiO_2 interface.[8]

Figure 3 shows the SRPES spectra of selected Si 2*p* and Ge 3*d* core levels for the samples implanted with a fluence of 1×10^{16} cm^{-2} as a function of T_A. Note that the analysis was performed on the sample surface and SRPES is only sensitive to a region of several-nanometer depth. The binding energy (103.3 eV) of the Si 2*p* spectrum corresponds to Si in the SiO_2 phase as demonstrated in the previous reports.[13] For the Ge 3*d* level spectra have been previously been found to

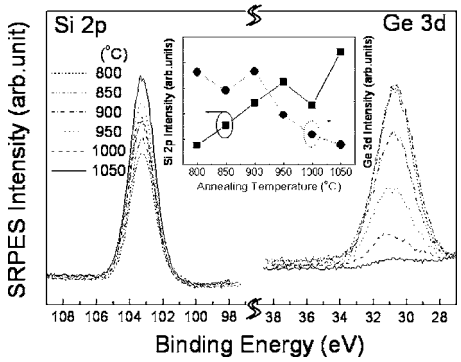

FIG. 3. SRPES spectra of selected Si 2*p* and Ge 3*d* core levels for the samples implanted with Ge ions to a fluence of 1×10^{16} cm^{-2} as a function of the annealing temperature.

split into two components related to Ge–Ge and Ge–O bonds, respectively,[14] but in this work only the signal from the Ge–O bond is observed, as shown in Fig. 3. The binding energy (30.8 eV) of the Ge 3*d* level is about 1.0 eV smaller than that of stoichiometric GeO_2.[13] These considerations suggest the presence of an underoxidized GeO_x structure without metallic Ge. Therefore, a mixture of SiO_2 and GeO_x appears to exist in the near-surface region of the Ge-implanted oxide layer. The T_A dependence of the two peaks is summarized in the inset of Fig. 3. With increasing T_A, the GeO_x phase decreases and the SiO_2 phase increases. Similar behavior was observed for the samples implanted with a fluence of 5×10^{15} cm^{-2}.

When Ge ions are implanted into SiO_2 films Si–O bonds are destroyed resulting in a mixture of Ge, Si, and O atoms. At low T_A's, Ge–O (including GeO_x) bonds can be formed in addition to Si–O bonds. At high T_A's, GeO_x is reduced by Si to produce SiO_2 and Ge, consistent with the data in Fig. 3 and previous report.[9] During this stage, Ge atoms diffuse throughout the layer and accumulate at the Si/SiO_2 interface, consistent with the EDS results in Fig. 2(b). The precipitation of Ge nanocrystals coincides with the onset of well-defined *C-V* curves, as shown in Figs. 1(a) and 3. The *C-V* curves of samples annealed at lower temperatures, inset in Fig. 1(a), are consistent with the fact that the mixed SiO_x/GeO_x phase and/or defects in the oxide layer induce unstable charge at the SiO_2/metal interface.

The above analysis suggests that the presence of Ge NCs is important for establishing well-defined *C-V* characteristics and that the memory effect is therefore related to charges stored in Ge NCs. The existence of Ge NCs is confirmed by TEM, as shown in Fig. 2. Moreover, it is known that the formation temperature of Ge NCs is $\geqslant$850–900 °C,[9] which is much lower than that of Si NCs. In Fig. 1, the samples annealed at T_A's$\leqslant$900 °C show distorted *C-V* curves consistent with the lack of well defined nanocrystals. Therefore, it is necessary to anneal the Ge-implanted samples above 900 °C for well-defined *C-V* curves in Ge-NC-based NVM memories.

In conclusion, *C-V*, TEM, EDS, and SRPES were used to characterize MOS structures containing Ge NCs produced by ion-implantation and annealing. The *C-V* hysteresis curves were shown to depend strongly on T_A, with well-defined *C-V* curves being observed for $T_A\geqslant950$ °C where Ge nanocrystals are known to form. In this regime TEM and EDS demonstrated the existence of regularly arranged Ge NCs of approximately 3–5 nm diameter located around 6.7 nm from the interface. This data provide strong support for the fact that the *C-V* hysteresis is dominated by charge trapping at Ge nanocrystals.

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[1] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Cabbe, and K. Chan, Appl. Phys. Lett. **68**. 1377 (1996).
[2] G. Iannaccone and P. Coli, Appl. Phys. Lett. **78**, 2046 (2001).
[3] W. K. Choi, W. K. Chim, C. L. Heng, L. W. Teo, Vincent Ho, V. Ng, D. A. Antoniadis, and E. A. Fitzgerald, Appl. Phys. Lett. **80**, 2014 (2002).
[4] Y. H. Kwon *et al.*, Appl. Phys. Lett. **80**, 2502 (2002).
[5] M. Kanoun, A. Souifi, T. Baron, and F. Mazen, Appl. Phys. Lett. **84**, 5079 (2004).
[6] Y. Maeda, Phys. Rev. B **51**, 1658 (1995).
[7] N. Takahashi, H. Ishikuro, and T. Hiramoto, Appl. Phys. Lett. **76**, 209 (2000).
[8] E. S. Marstein, A. E. Gunnæs, A. Olsen, T. G. Finstad, R. Turan, and U. Serincan, J. Appl. Phys. **96**, 4308 (2004).
[9] M. C. Ridgway *et al.*, Nucl. Instrum. Methods Phys. Res. B **218**, 421 (2004).
[10] J. P. Biersack and L. G. Haggmark, Nucl. Instrum. Methods **174**, 257 (1980).
[11] L. W. Teo *et al.*, Appl. Phys. Lett. **81**, 3639 (2002).
[12] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981), Chap. 7.
[13] A. Agarwal, J. K. Patterson, J. E. Greene, and A. Rockett, Appl. Phys. Lett. **63**, 518 (1993).
[14] T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland, Appl. Phys. Lett. **83**, 1444 (2003).