

## **Carrier lifetime studies of deeply penetrating defects in self-ion implanted silicon**

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Carrier lifetime measurements have been used to characterise residual defects after low-energy implanting of silicon ions followed by high temperature annealing (900 or 1000°C). The implant was found to result in two distinct regions of lifetime-reducing damage. Firstly, a high recombination region, most likely due to stable dislocation loops, remained near the surface. In addition, deeply propagated defects, which were not present prior to annealing, were also detected. These deep defects, which are possibly silicon interstitials, diffuse so rapidly during annealing that their distribution becomes effectively uniform to a depth of 100 microns. Annealing at higher temperatures was found to reduce the severity of both the surface and the deeply propagated defects.

Ion implantation is the technique of choice for introducing dopant species into semiconductors for microelectronic devices. Subsequent high temperature annealing then serves the purpose of healing the lattice damage, as well as activating dopant atoms. The evolution of the primary damage during annealing is relatively well understood, as are the types of defects that remain in the near-surface region. However, fewer studies have explored the possibility of very deeply penetrating defects that may extend many tens of microns below the surface. In this work, we have used highly sensitive carrier lifetime techniques to study such deep-lying residual defects that remain after annealing, even at 1000°C.

Lattice vacancies and interstitials arising from the implantation process annihilate one another very rapidly during annealing at elevated temperatures. This leaves, in principle, only one interstitial for every implanted atom, as commonly expressed in the “+1” model<sup>1</sup>. Transmission electron microscopy studies have shown that these excess interstitials, upon annealing at moderate temperatures, form agglomerations such as rod-like clusters lying on {311} planes<sup>2</sup>. Their subsequent dissolution emits interstitials that drive effects such as transient enhanced diffusion of dopants<sup>3</sup>. If the initial damage is sufficiently severe, these clusters can also form end-of-range dislocation loops that are stable at temperatures up to 1000°C<sup>4</sup>. These loops occur predominantly at the interface of the original amorphized layer and the underlying substrate.

However, there are other possible fates for the excess interstitials: many may recombine at the surface, or they may diffuse deeper into the wafer bulk. Spreading resistance measurements have shown that interstitials can migrate several microns deep at room temperature, before being trapped by native defects<sup>5</sup>. At high anneal temperatures, thermal de-trapping should allow much deeper penetration of silicon interstitials. In principle then, during high temperature annealing, at least some small fraction of the interstitials could avoid being bound in loops or recombining at the surface, and consequently be injected

deep into the wafer bulk. Carrier lifetime measurements provide a path for studying such deep-lying defects. These techniques are, by their very nature, extremely sensitive to localised states acting as recombination centres, and have the added advantage of sensing the entire depth of a sample, rather than a shallow surface region.

In this study, 500-micron thick 1Ωcm boron-doped p-type float zone (FZ) <100> oriented silicon wafers were implanted with 36keV Si<sup>28</sup> ions. The wafer surface was offset by 7° from the beam line to avoid ion channelling. The depth of peak ion damage was revealed to be around 50nm by simulations with the software TRIM<sup>6</sup> (Transport of Ions in Matter).

Ion doses of either 1×10<sup>14</sup> or 3×10<sup>15</sup>cm<sup>-2</sup> were implanted with the wafers held at 100°C. These conditions result in buried amorphous pockets rather than a continuous amorphous zone extending to the surface. The samples were then conventionally annealed at either 900 or 1000°C for 60 minutes in nitrogen. Such implant and anneal conditions are known to result in a large concentration of end-of-range dislocation loops<sup>4</sup>.

The wafer surfaces were passivated for lifetime measurements by plasma silicon nitride films, which are known to provide excellent surface passivation for the material used in this study<sup>7</sup>. Effective lifetime measurements were performed using the Quasi-Steady-State PhotoConductance technique (QSSPC)<sup>8</sup>.

Figure 1 plots injection-dependent lifetime measurements for some of the samples annealed at 900°C. The control sample was not implanted, but was subject to the same annealing, etching and cleaning treatments. As such, the lifetime measurement on this wafer determines the sensitivity limit of the study. It allows the net impact of surface and Auger recombination, as well as possible background contamination from the furnaces, to be quantified.

The lifetimes of the implanted and annealed samples in Fig 1 are well below the control. In these cases, the measured lifetime reflects a combination of residual defects

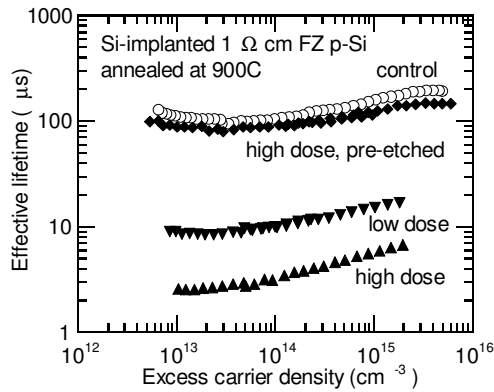


FIG 1. Measured injection-dependent lifetimes of samples annealed at 900°C with low and high implanted Si doses. The control sample was not implanted, and the pre-etched sample had the implant etched before annealing.

near the surface, primarily end-of-range dislocation loops, and any other defects propagated more deeply. The heavier ion dose resulted in a greater amount of residual damage and hence lower lifetime.

Figure 2 summarises the results for all samples annealed at either 900 or 1000°C, in the form of lifetimes measured at an excess carrier density of  $1 \times 10^{14} \text{ cm}^{-3}$ . More complete damage annealing at the higher temperature results in a longer carrier lifetime. In fact for the lighter ion dose, the higher anneal temperature removes the damage to the extent that it can no longer be detected.

Fig 1 and 2 also show data for implanted samples that were etched to a depth of 5μm directly after implantation, but prior to annealing, and are labelled 'pre-etched'. These samples yielded lifetimes comparable to the controls, and are confirmation that defects caused directly during implantation do not extend more than 5μm into the wafer prior to annealing. Of course, end-of-range dislocation loops would not be present in these wafers, but it is possible that more deeply migrating defects could penetrate beyond the etch depth. However, a recent study of 40keV Si implant damage<sup>9</sup> using spreading resistance and deep level transient spectroscopy measurements showed that interstitials migrated only up to 0.9μm deep prior to any annealing. The pre-etch applied in this study should then be ample to remove all of these defects, resulting in an undamaged substrate prior to annealing.

The depth of the residual defects after annealing in those samples that were not pre-etched can be revealed by lifetime measurements after repeatedly etching and re-passivating the sample. These are shown in Figure 3 for the samples annealed at 900°C. As expected, the control wafer remains practically unaffected by the etching. In contrast, there is a pronounced increase in lifetime of the implanted samples after etching the first 15μm. This increase reflects the removal of the end-of-range dislocation loops, which act as a strong recombination region. It is likely therefore that a much shallower etch would achieve the same result. The important observation, however, is that the lifetime after etching still remains significantly lower than the control lifetime. This can only be explained by the presence of other, more deeply penetrating, defects.

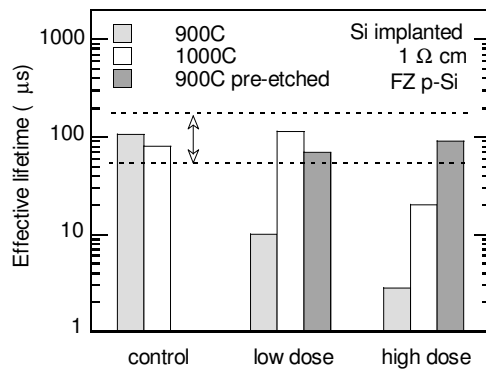


FIG 2. Measured effective lifetimes at an excess carrier density of  $1 \times 10^{14} \text{ cm}^{-3}$  for two anneal temperatures and two Si doses ( $1 \times 10^{14}$  and  $3 \times 10^{15} \text{ cm}^{-2}$ ). Samples that fall between the dashed lines have too little damage to be detected.

Upon further etching of the implanted samples, the lifetimes remain at a constant level well below that of the control wafer. This plateau indicates that the depth profile of these deeply propagated recombination centres is approximately uniform up to 100μm deep, possibly extending throughout the entire wafer thickness, implying a very high diffusivity at the anneal temperatures.

These conclusions are corroborated by spectrally resolved photoconductance data, shown in Figure 4. The different illuminating wavelengths, achieved with 10nm band-pass filters, result in different generation depths, as shown on the figure. To allow direct comparisons between the controls and the damaged samples, the values have been normalised at 1000nm.

The control sample had very little spectral dependence, except for a strongly reduced photoconductance at the poorly absorbed wavelength of 1100nm. In this case, the uniform bulk lifetime and good surface passivation result in a photoconductance that is insensitive to the point of generation (ie illuminating wavelength). By contrast, the implanted samples, prior to etching and when illuminated from the front, display a strong spectral dependence, revealing a region of higher recombination activity near the front surface. When measured from the rear however, the response of these samples was similar in shape to that of the control sample.

Figure 4 also shows data for the heavily implanted sample measured a second time with illumination from the front, but after etching 15μm from each surface and re-passivating. The strong wavelength dependence then largely disappears, reflecting low recombination at the front surface. This fact implies that the etching process itself does not inadvertently propagate surface defects, which could otherwise distort the results. The magnitude of the photoconductance remained lower than the controls however, reflecting the reduced, but spatially uniform, bulk lifetime.

A likely candidate for the cause of the deeply propagating defects is silicon interstitials. They are extremely mobile and could easily diffuse many times through the wafer thickness at the anneal temperatures used, resulting in a uniform distribution. Also, the FZ material

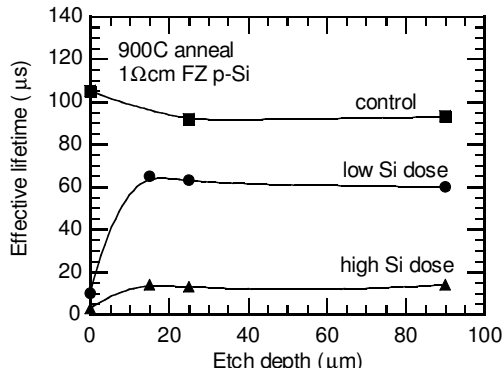


FIG 3. Effective lifetime as a function of the depth of silicon etched from the front surface.

used in this study is relatively free of traps that could markedly slow the diffusion of interstitials.

Higher doses result in a greater initial concentration of interstitials, and so a higher concentration is likely to escape into the bulk during annealing, consistent with the lifetime results here. In the extreme case in which *all* of the interstitials diffused deep into the bulk, the highest dose used in this study would, according to the +1 model, result in a volume concentration of  $6 \times 10^{16} \text{cm}^{-3}$ . However, many of these interstitials will of course be bound in end-of-range dislocation loops, which have been shown to ripen conservatively during annealing<sup>4</sup> (that is, maintaining an approximately constant number of interstitials). On the other hand, even if only 1% of these interstitials is not bound by dislocation loops or annihilated at the surfaces, this still leaves a relatively large defect concentration. By comparison, the amount of interstitial Fe required<sup>10</sup> to reduce the carrier lifetime of this material to 10 $\mu\text{s}$  at an excess carrier density of  $10^{14} \text{cm}^{-3}$  is only  $1 \times 10^{12} \text{cm}^{-3}$ .

The results also suggest that annealing at higher temperatures causes a reduced concentration of interstitials deep in the wafer. This could be explained by the more frequent encounters with the surfaces, where they may recombine. However, the diffusivity of interstitials at these temperatures is so high that this process should be driven to completion very quickly, in the absence of marked slowing of diffusion by trapping. This suggests that the source of the interstitials may be the dislocation loops, which slowly dissolve after ripening. The reduced concentration of interstitials deep in the bulk at higher temperature may then reflect the more complete annihilation of the dislocation loops, leading to a reduced rate of interstitial injection.

Initial implants were performed with a tantalum aperture to define the implanted region. This raised the concern that sputtering of metal ions from the aperture rim may contaminate the wafer surface. As a consequence, the experiments were repeated with a silicon aperture. The results, however, were unchanged, within measurement uncertainty.

The deeply penetrating defects detected in this study may be detrimental to the performance of devices that rely on the properties of the wafer bulk, such as imaging devices, photodetectors and solar cells. They should also be

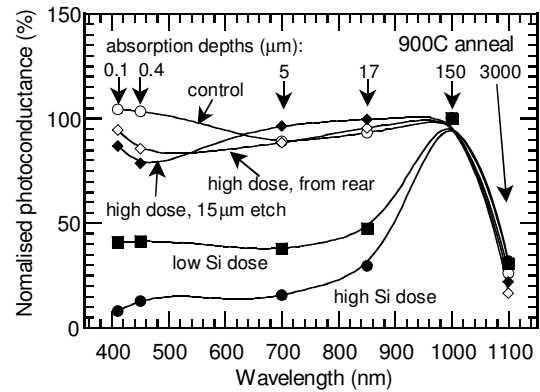


FIG 4. Spectral dependence of the steady-state photoconductance, normalized at 1000nm, for the samples annealed at 900°C. For the high dose sample, three measurements are shown: with illumination from the front (solid circles), with illumination from the rear, and after etching 15 $\mu\text{m}$  from the front surface.

considered when using ion implantation for lifetime studies of metal contaminants<sup>10</sup>. In such cases, it is desirable that the propagated defects have little impact on the lifetime measurements. Fortunately, the doses required for many metals are relatively low: for example, typically below  $10^{12} \text{cm}^{-2}$  for Fe.

In summary, the lifetime measurements reported here show that for relatively high ion doses, both surface and deeply propagated defects remain after annealing even at 1000°C. The high recombination region at the surface is attributed to end-of-range dislocation loops, which are known to occur under the conditions used. The deeply penetrating recombination centres, which are distributed uniformly up to a depth of at least 100 $\mu\text{m}$ , may be caused by silicon interstitials. Anneal temperatures above 1000°C could lead to more complete removal of these deep defects.

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