Formation of plasma induced surface damage in silica glass etching for optical waveguides

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Ge, B, P-doped silica glass films are widely used as optical waveguides because of their low losses and inherent compatibility with silica optical fibers. These films were etched by ICP (inductively coupled plasma) with chrome etch masks, which were patterned by reactive ion etching (RIE) using chlorine-based gases. In some cases, the etched surfaces of silica glass were very rough (root-mean square roughness greater than 100 nm) and we call this phenomenon plasma induced surface damage (PISD). Rough surface cannot be used as a platform for hybrid integration because of difficulty in alignment and bonding of active devices. PISD reduces the etch rate of glass and it is very difficult to remove residues on a rough surface. The objective of this study is to elucidate the mechanism of PISD formation. To achieve this goal, PISD formation during different etching conditions of chrome etch mask and silica glass was investigated. In most cases, PISD sources are formed on a glass surface after chrome etching, and metal compounds are identified in these sources. Water rinse after chrome etching reduces the PISD, due to the water solubility of metal chlorides. PISD is decreased or even disappeared at high power and/or low pressure in glass etching, even if PISD sources were present on the glass surface before etching. In conclusion, PISD sources come from the chrome etching process, and polymer deposition on these sources during the silica etching cause the PISD sources to grow. In the area close to the PISD source there is a higher ion flux, which causes an increase in the etch rate, and results in the formation of a pit. © 2004 American Institute of Physics. [DOI: 10.1063/1.1739525]

I. INTRODUCTION

Due to their low loss and inherent compatibility with optical fibers, silica (usually doped with Ge, B, P, etc.) glass films are widely used in planar lightwave circuits (PLCs). The potential applications of these devices range from optical communications to automotive control systems. Dry etching of silica glass for semiconductor applications is a well-established and routine process. Although basically similar, the silica films used in planar waveguides have several differences, which influence the development of a suitable dry etching process. First, the required etching depth of silica in waveguide devices can range from a few microns to 50 μm , as opposed to typically less than 1 μm in integrated circuit technology. A few microns is common in most waveguide patterns, but a few tens of microns are needed in hybrid integration with active devices and bio-electronic applications such as fluid handling and optical bio-sensing.¹ This places extra demands on mask thickness and/or material selectivities, as well as on the silica etch rate, which should be high enough to obtain reasonable throughput. Hard masks such as amorphous silicon² and chromium³ have been used, because the photo-resist (PR) mask that is generally used in semiconductor processes has not enough selectivity to etch tens of microns of silica. To obtain a higher silica etch rate without degrading mask selectivity, high density plasma

(HDP) systems like inductively coupled plasma (ICP),^{3,4} hollow cathode reactive ion etching (RIE),² or electron cyclotron resonance (ECR) RIE,⁵⁻⁷ have been utilized because plasma density and ion energy can be controlled independently in these equipments. Second, the roughness of the etched walls of the waveguide structures or light turning mirror should be as small as possible in order to reduce the loss due to light scattering.²

Samples exposed to a glow discharge always show surface damage. For silica layer in C-F based plasma, the damage can be categorized as (a) a deposited Teflon-like top layer; (b) roughening of the substrate surface; (c) implanted ions and neutrals; and (d) lattice distortion.⁸ It was known that surface damage categorized as (c) and (d) has little influence on the optical properties of fabricated waveguides. Both Teflon-like film deposited on the etched surface and the roughening of the substrate surface can, however, complicate following a silica dry etching process. Therefore, these two types of surface damage are the main focus in this study.

Under some process conditions, the etched surface of silica glass was very rough and we call this phenomena "plasma-induced surface damage (PISD)." From a quantitative point of view, the degree of surface roughness can be represented by the root mean square roughness (R_q), which is measured using an optical profiler. R_q 's of etched surfaces vary from a few to above a hundred nanometers depending on their process conditions, as compared to a few nm on the un-etched surface. PISD formation etched on the surface has some detrimental effects. First, the silica etch rate is dependent upon the extent of roughness. When severe PISD is

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formed on the etched surface, no more etching is possible. This behavior—etching rate dependency on the extent of PISD—hinders us from predicting the etching depth precisely. Second, the rough etched surface cannot be used as a platform for hybrid integration with opto-electronic devices, or some other components. Metallization, which is needed to pattern the bonding pad or electrical wire line, cannot be processed properly on a rough surface. Furthermore, vertical (y-axis) alignment between the silica waveguide facet and active device, which is obtained from a precise etching depth, would be impossible, thus increasing the optical coupling loss. Third, thick Teflon-like layer is deposited on a roughened surface, and this layer is not easily removed during the subsequent processes. The resultant residues of polymer constituents on the etched surface act as impurities. This fact will be discussed in more detail in the main body of this paper.

There have been a few reports regarding the roughening of etched silica surface,^{3,8} but no systematic study on the causes and effects of this phenomenon. The objective of this study is to elucidate the mechanism of PISD formation and to present the method to obtain a smooth etched surface. First, the chemical analyses of etched surfaces both with and without PISD were performed using x-ray photoelectron spectroscopy (XPS). We reached a conclusion that the quantity and composition of polymer on etched surface are dependent on the extent of PISD. Then, the changes in PISD formation behaviors, when different etching parameters were applied in ICP silica and RIE chromium etching, were investigated. Finally, a PISD formation mechanism was proposed based on the above investigations.

II. EXPERIMENTAL PROCEDURES

Si wafer with 15 μm -thick thermally grown oxide acting as a buffer layer was used as the substrate. Ge, B, P-doped silica soot was deposited on the substrate by a flame hydrolysis deposition (FHD) method and sintered in a furnace at a high temperature ($>1000^\circ\text{C}$) to form a transparent glass layer. The thickness of this doped silica (core layer) was around 7 μm . Chromium (Cr) was chosen as the etch mask material for its high resistance to ion bombardment during deep silica etching. Etch rate ratio (selectivity) of silica to Cr was generally above 30, though it changed widely with the process conditions of silica etching. 500 nm-thick Cr film was deposited on core layer by dc sputtering, and PR (Dong Woo Fine-Chem Co., PFI 91B1, 1.2 μm thick) waveguide patterns were formed on the Cr layer using the conventional photolithographic process. The Cr layer was etched in a commercial RIE system (Plasma-Therm SLR-720) using a Cl_2/O_2 gas mixture. To investigate the effects of Cr etching parameters on the PISD formation, different rf power and gas pressure and/or substrate holder materials (Al_2O_3 or Si covered Al) were applied. The average Cr etching rate and selectivity to PR were 40 nm/min and 1, respectively. Normally, 30 seconds over-etch was applied after the exposed Cr layer was removed completely.

Silica layer etching was carried out using an ICP system (Plasma-Therm SLR-770), and C_4F_8 was used as reactive

FIG. 1. The XPS survey spectra measured on the etched surface without PISD. The three curves represent the XPS spectra taken after each stage of surface preparation; (a) after the sample was etched in ICP, (b) then the sample was cleaned in a Cr-etchant and BOE, and (c) followed by argon (Ar) ion sputtering. The Ar-sputtering was done *in situ* in an XPS chamber and the sputtered depth was 5 nm.

gas. The variable parameters of the etching experiments were bias power, operating gas pressure, wafer temperature, and wafer clamp materials (Al_2O_3 or Si). Herein, the wafer temperature was controlled by adjusting the helium pressure for wafer backside cooling. The etching rate of the doped silica layer was above 0.5 $\mu\text{m}/\text{min}$, and the etch depth was around 8 μm . After the etching, the remaining Cr mask was removed by dipping the substrate in Cr-etchant (Cyantek, Cr-7SK). Most of the polymer on the etched surface and side-wall was also eliminated in this process. Then, the wafer was etched in a buffered oxide etchant (BOE) for 10 seconds to get rid of any residue on the etched surface.

The chemical compositions of the etched surfaces were investigated using XPS. The sampling volume was 200 μm in diameter and 5 nm in depth. The Gaussian–Lorentzian and Shirley method were applied for curve fitting and background calculation, respectively. The morphology of etched surface and the etch residues on the surface were observed using a scanning electron microscope (SEM) and optical profiler.

III. RESULTS AND DISCUSSION

A. The analyses of the etched silica surfaces both with and without PISD

The chemical compositions and bonding states of the constituents on the etched silica surfaces both with and without PISD were analyzed using XPS. The silica etching conditions of both samples were the same; 30 sccm C_4F_8 flow rate, 10 mTorr chamber pressure, 200 W bias power, and 990 W induction power. The presence of PISD on etched surface is determined by the previous processes—Cr etching and post metal etch treatments, which will be described in detail in the next sections.

Figure 1 shows the XPS survey spectra measured on the etched surface without PISD. This graph can be used to verify the presence of other elements on the surface except for the constituents of the silica layer. The three curves represent the XPS spectra taken after each stage of surface preparation: (a) after the sample was etched in ICP, (b) then

FIG. 2. High-resolution C 1s spectrum obtained for the sample in Fig. 1(a). The spectrum data was deconvoluted to several overlapping peaks by Gaussian and Lorentzian fitting. Prior to this, the nonlinear background of a secondary electron was subtracted from the data.

the sample was cleaned in Cr-etchant and BOE, and (c) followed by argon (Ar) ion sputtering. The Ar-sputtering was done *in-situ* in an XPS chamber and the sputtered depth was 5 nm. The roughness (R_q) of the etched surface was below 10 nm, which is the same as that of the core layer surface before etching. This means that the silica etching itself does not degrade the roughness of the etched surface, if no PISD is formed during etching. Except the constituents of silica layer, carbon and fluorine were observed, which are the main components of the polymer that is commonly generated in the fluoro-carbon plasma. Any trace of aluminum, which could be sputtered from the ICP and RIE chamber walls and wafer clamps,⁸⁻¹⁰ was not detected. From Figs. 1(a) and 1(b), we can find that C and F are eliminated completely during the Cr-etchant and BOE processes. A small C 1s peak in Fig. 1(b) is due to the C contamination from air exposure, before the sample was loaded in an XPS chamber. This peak disappears after the surface was sputtered by an Ar ion in XPS [Fig. 1(c)].

Figure 2 is the high-resolution C 1s spectra, which was obtained for the sample in Fig. 1(a). The spectrum data were de-convoluted to several overlapping peaks by Gaussian and

FIG. 3. The XPS survey spectra measured on the etched surface with PISD. The remaining descriptions are the same as the caption in Fig. 1.

FIG. 4. High-resolution C 1s spectrum obtained for the sample in Fig. 3(a). The remaining descriptions are the same as the caption in Fig. 2.

Lorentzian fitting. Prior to this, the nonlinear background of the secondary electrons was subtracted from the data. Carbon compounds gave rise to a large asymmetric peak centered at ~ 285 eV, and a broader peak which is shifted to a larger binding energy and extended to 292 eV. The ~ 285 eV component is due to the C-C and peaks at larger binding energies are due to the C-F, C-F₂, and C-F₃ species.³ As a result of the C 1s peak analysis, even though it was not fully analyzed, it can be concluded that the carbon compounds with a low F/C ratio are dominantly formed on the etched silica surface with no PISD formation. [The F/C ratio, which is obtained by measuring the areas of C 1s and F 1s peaks in Fig. 1(a), is about 0.4.] From the above conclusion, it can be inferred that the silica sample with a PISD-free surface was etched at a high dc bias voltage and the deposited polymer is induced by ion-assisted polymerization.^{5-7,11}

The XPS survey spectra measured on the etched surface with PISD are depicted in Fig. 3. The high-resolution C 1s spectra, which are obtained for the sample in Fig. 3(a), are also in Fig. 4. The remaining descriptions of Figs. 3 and 4 are identical to the caption in Figs. 1 and 2, respectively. Figure 5 is the SEM image showing the etched surface morphology of the sample in Fig. 3(b), i.e., after the sample was etched in ICP and cleaned in Cr-etchant and BOE. A large amount of pits that are the results of PISD are seen, and the R_q of this surface is above 200 nm. The dimension of the pits, which increases with etching depth, ranges from sub-

FIG. 5. SEM image showing the etched surface morphology of the sample in Fig. 3(b). A large amount of pits that are the results of a PISD are seen.

microns to a few microns in diameter and depth. If there is a source of PISD on the etched surface, it can develop into needle-like structures or pits, depending on the etch conditions. Only pits, however, were observed on the etched surfaces when samples were etched at a normal gas pressure (5–15 mTorr). More details will be discussed in Sec. IV.

In Fig. 3(a), a large quantity of C and F was observed due to the thicker polymer layer deposited on the etched surface. It was impossible to remove C and F completely through the Cr-etchant and BOE processes. This is because the aqueous solutions (Cr-etchant and BOE) are not easy to penetrate through the deposited thick polymer due to the hydrophobic nature of the C–F polymer. The residues, mainly in the bottoms of the pits, act as impurities during the following process. In fact, the polymer on the etched surface and sidewall was the source of bubble-generation during the overlapping process. The measured F/C ratio from Fig. 3(a) was 1.8, and this high ratio means that the deposited polymer was formed at a low dc bias voltage.^{5–7} Two aluminum peaks (Al 2s and Al 2p) were detected on the etched surface, but eliminated after the cleaning processes. The peak position of Al 2p was 77.06 eV. From the database of XPS peak positions,¹² Al is supposed to exist as AlF₃ and/or Al₂O₃. It was reported in Ref. 8 that nonvolatile metal fluoride, e.g., AlF₃, CuF₂, or NaF, from etch mask and electrode can act as chain initiator for polymer growth. From Fig. 4, the species with higher binding energies are observed in large amounts in the deposited polymer. Especially, C–F₂ (the peak centered at around 291 eV), a known polymer precursor,¹¹ is the most plentiful one. These observations also account for the high F/C ratio of the polymer.

From the XPS observations and analyses of etched silica surfaces both with and without PISD, several conclusions, listed below, can be drawn.

(i) Although the same silica etching conditions were applied, samples both with and without pits resulting from PISD appeared. Therefore, it can be concluded that the sources of PISD are produced on the silica surface before the silica etching process.

(ii) The main polymer components, C and F, are detected on the etched surface. If no PISD is present on the surface, the F/C ratio of the polymer is low. On the contrary, the polymer with a high F/C ratio is observed on the damaged surface. And these facts imply that the polymers on the etched surfaces with and without PISD are deposited at low and high dc bias voltage, respectively.

(iii) The wet cleaning processes after silica etching remove the polymer on the etched surface. However, as the residues on the damaged surface cannot be eliminated completely, they complicate the following processes.

(iv) A trace of aluminum is detected on the damaged surface, and the possible form of it is AlF₃ and/or Al₂O₃. Al, which is supposed to be from the etching chamber wall and wafer holder, acts as a catalyst for polymerization.

B. PISD behaviors according to the changes in ICP silica etching parameters

In the previous section it was concluded that the sources of PISD are produced on the surface before the silica etching

process. Then, growth of these sources into pits occurs during the silica etching step. We propose that the sources of PISD, for their catalytic function, enhance the polymer deposition on them, and the grown PISD sources act as micro-masks during the silica etching. By investigating the variations of PISD patterns with the changes in ICP silica etching parameters, in this section, our proposal for PISD formation mechanism will be confirmed. The other source of PISD and the development into pits are also investigated. Herein, the etching parameters include gas composition, bias power, operating pressure, wafer temperature, material of wafer clamp, and etching depth or time. Before silica etching, all the samples were prepared through the same process and condition. The applied RIE Cr etching condition was 40 sccm Cl₂ + 10 sccm O₂ gas flow, 150 mTorr chamber pressure, and 150 W bias power.

CF₄, CHF₃, and C₄F₈ gases were used to etch the silica layer. At the same etching condition, except for the gas used, the thickness of deposited polymer and the selectivity to Cr decreased with a F/C ratio of the gas. This result agrees with the reports⁵ that the polymer formation is enhanced in gas with a low F/C ratio and polymer protection on the Cr mask from ion bombardment increases the etch selectivity. PISD forms as a result of the polymer deposition on the PISD source and its micro-masking action. Because the thickness of the deposited polymer decreases with the F/C ratio of etch gas, the extent of PISD would also decrease with this ratio. However, the observed roughness of etched silica was not according to the F/C ratio, but C₄F₈ > CF₄ > CHF₃ in the order of R_q . In the case of CHF₃, the reduced roughness could be related to the decreased density of PISD sources. Metal or metal compound residues on silica layer, as will be discussed in the next section, act as PISD sources when they are not removed completely before silica etching. It is reported that a hydrogen atom and/or radical in CHF₃ etching plasma react with metal to form volatile metal-hydride.¹³ This report supports our reasoning. Also, adding O₂ gas to C–F plasma reduces the degree of PISD by means of scavenging the polymer,¹⁰ but does not completely eliminate PISD.

The extent of PISD increases with the operating pressure, and this is due to the enhanced polymer deposition on PISD sources at higher pressures. At very low pressures (below 5 mTorr), no PISD was observed, regardless of the conditions of Cr etching. This is a result of two contributions. First, the reduced polymer deposition at low pressure hinders PISD sources from evolving. Second, PISD sources can be sputtered from the silica surface, because high dc bias voltage and a longer mean free path at low pressures enhances the sputtering of the sources and prevents the sputtered sources from re-depositing on the surface, respectively. The sputtering of PISD sources can also explain the observed reduction of roughness on the etched surface at high bias powers.

At very high pressures (higher than 30 mTorr), however, an extraordinary phenomenon occurred. Figure 6 is the SEM image showing the surface morphology of etched silica, when the silica layer was not patterned before (i.e., bare silica) and etched at 40 mTorr. Micro-masks of 2 or 3 μ m in

FIG. 6. SEM image showing the surface morphology of etched silica, when the silica layer was not patterned before (i.e., bare silica) and etched at 40 mTorr gas pressure.

diameters and heights were generated on the etched surface. On the other hand no micro-masks or pits were observed, if the bare silica was etched at an operating pressure lower than 30 mTorr. A large quantity of C and F, along with Si, O, and Al, was detected on these micro-masks by energy dispersive spectroscopy (EDS). When this sample was annealed at 400 °C for 1 h, no C and F was observed. The sputtered Al and/or Al_2O_3 from the wafer clamp are supposed to be the sources of PISD at very high pressures. Once there exist PISD sources on the etched surface, they can be developed into micro-masks, instead of being sputtered due to the high polymer deposition rate on them.

As described previously, the wafer temperature was controlled in a range between 100 and 230 °C, by adjusting the helium pressure for wafer backside cooling. The degree of PISD decreases with the wafer temperature. This is owing to the reduced polymer deposition on PISD sources, because the sticking coefficient of the polymer gets lower at higher wafer temperatures.

The purpose of the clamp material change to Si (from Al_2O_3) is to remove PISD sources originating from the wafer clamp. It was reported^{3,8–10} that sputtered and re-deposited particles from the alumina clamp can be PISD sources. Therefore, a metal-free clamp, like quartz, Teflon, and graphite, should be used to eliminate them. There was no detected Al on the etched silica surface, and this means Al is hardly sputtered from the etching chamber walls. When the silica layer with a Cr mask was etched at a normal pressure range (5–15 mTorr) in ICP, the clamp material did not affect the density of pits. This also supports the fact that the sources of PISD are produced before the silica etching process. There were no pits or micro-masks when bare silica layer was etched in Si-clamp-equipped ICP at 40 mTorr. This observation, if compared with the case in Fig. 6, also accounts for the advantage of a Si-clamp. The use of a Si wafer clamp also had some side effects. Though the silica etching rate is reduced about 20% because some radicals or ions in plasma are consumed in an etching Si clamp, the etched sidewall gets smoother. (By changing the clamp from alumina to Si, R_q of the sidewall is reduced to 20 nm from 35 nm.) This will be discussed fully in Sec. IV.

FIG. 7. SEM images showing the development of PISD into pits on the surface with etching time. Note that three SEM images were taken at the same magnification, except Fig. 7(a). Some micro-masks [white spots in Fig. 7(a)] can be seen at an early stage of etching, but they disappear at later stages.

Figure 7 depicts the development of PISD into pits on the surface with respect to etching time. Note that the three SEM images except Fig. 7(a), were taken at the same magnification. Some micro-masks [white spots in Fig. 7(a)] can be seen at the early stage of etching, but they disappear at later stages. From Fig. 7, it can be concluded that the density of pits does not change but the dimension of each pit increases with etching time. This means that no additional pits are generated during the ICP silica etching process. In reference to Fig. 7, the PISD formation mechanism will be proposed in Sec. IV.

C. PISD behaviors according to the changes in RIE Cr mask etching parameters

In this section, the causes and elimination methods of PISD are investigated. First, a series of experiments were performed to clarify at which step PISD sources are produced. Five silica samples (S#1–S#5) with different preparation histories were etched simultaneously in the ICP system. The ICP etching condition for silica layers was 30 sccm C_4F_8 flow rate, 15 mTorr chamber pressure, 200 W bias power, 990 W induction power, and 20 minutes etching time. The condition of RIE Cr etching, if applied, was the same as described in Sec. II. The preparation methods are as follows: S#1: Bare silica (the results of this sample was already mentioned in Sec. II).

S#2: Bare silica which was exposed to the Cr etching plasma ($\text{Cl}_2 + \text{O}_2$) in RIE for 20 minutes.

S#3: Only PR patterns on bare silica.

S#4: Cr mask patterns on silica formed by the lift-off method.

S#5: Normally prepared silica (i.e., Cr dry etching in RIE).

TABLE I. Roughness data of etched silica surfaces according to the applied Cr etching system and post-metal etching treatments.

Exp. No.	Cr etching system	Cr etching conditions	Post-metal etch treatment	R_q (nm)
1	RIE	150 W	No treatment	≥ 200
2	with Si wafer holder	150 mTorr	Ar sputtering	5.4
3		40 Cl ₂ + 10 O ₂	Water rinse	165
4			No treatment	≥ 200
5	with Al ₂ O ₃ wafer holder		Ar sputtering	4.9
6			Water rinse	175

PISD was generated only on S#5. The absence of PISD on S#2 indicates that “halogenated layer”^{14,15} on the silica surface, which is formed by the reaction with Cl₂ plasma and silica, is not the source of PISD. In addition, Al and/or Al-compound sputtered from the RIE chamber wall and wafer holder is not the source of PISD, if there is no Cr mask being etched. PR cannot act as PISD sources, either (from the result of S#3). By comparing the results of S#4 and S#5, it can also be concluded that the presence of a Cr mask in a RIE system is the only way that PISD sources can be formed on a silica surface. From the result of S#4, it can also be confirmed that Cr sputtering and re-deposition during silica etching in ICP cannot be the cause of PISD.

The above experiments confirm that the dry etching of the Cr mask in RIE is the step that produces PISD sources on a silica layer. To eliminate these sources, therefore, the modifications of Cr etching system (wafer holder materials) and post-metal etching treatments (water rinse and Ar sputtering) were applied and compared. Table I shows the roughness of the etched silica surfaces with and without the applied Cr etching system and post-metal etching treatment. All six silica layers were etched simultaneously under the same ICP etching condition; 30 sccm C₄F₈ flow rate, 10 mTorr chamber pressure, 200 W bias power, 990 W induction power, and 15 minutes etching time. “Ar sputtering” was carried out to completely eliminate any possible residue on the silica surface by means of physical sputtering. The applied “Ar sputtering” condition was a 30 sccm Ar flow rate, 3.5 mTorr chamber pressure, 100 W bias power, 950 W induction power, and 1 minutes etching time in an ICP system. Approximately, 100 nm of silica was sputtered using this process. No PISD is formed on sample (#2 and #5), which experienced “Ar sputtering.” Therefore, it can be concluded that residues on silica surface after Cr mask etching are the sources of PISD.

PISD were generated on the surfaces of samples without a post-metal etching treatment (#1 and #4), regardless of the wafer holder materials in the RIE system. The etched surfaces, like in Fig. 5, were so rough that an interference microscope could not measure the roughness quantitatively. Therefore, it is difficult to know whether the wafer holder materials in the RIE system affect the density of PISD. The silica etching rates of these samples were lower by around 20% than those of all other samples. This is because PISD formation impedes silica etching.

The “water rinse” is to wash the substrate with water (5 minutes at room temperature) after Cr etching. It is obvious from Table I that “water rinse” reduces the roughness of the

etched surface to a certain extent. This is supposed to be the result of removing the PISD source by washing. When detecting the surface residues before silica etching by XPS, the Cl 2*p* peak around 200 eV that is present on sample #4 (no treatment), disappears after a water rinse (#6). We propose that metal-chlorides, which are formed by the reaction of metals in Cl₂ plasma, are the sources of PISD. Herein, metals are thought to be originating from a Cr mask and its impurities (in Cr sputter target), wafer holder, and chamber walls. As most metal-chlorides (e.g., AlCl_x, FeCl_x, and CuCl_x) are soluble in water,¹⁶ a “water rinse” can reduce the PISD sources on the surface. However, washing with water cannot remove perfectly the PISD sources because there are insoluble chlorides, such as CrCl_x.¹⁷

In summary, PISD sources are formed on the silica surface during Cr dry etching, and the compositions of them are metal-chlorides. A “water rinse” can reduce them due to their solubility in water and make the etched surface smoother. However, the presence of insoluble chlorides prevents the etched surface from being PISD-free.

D. The proposal for PISD formation mechanism

Until now, the cause, development, and influence of PISD were investigated from the experimental observations and analyses. To summarize these results, in this section, we propose the PISD formation mechanism on an etched silica surface. The proposed mechanism also matches well with the experimental results. Some other issues, such as the evolution of PISD into pits and the relationship between PISD and the sidewall roughness of an etched trench, are also discussed.

It was concluded in Sec. III that the PISD source is formed on the silica surface during Cr dry etching, and the composition of the sources is supposed to be metal-chlorides. Metals are originating from the Cr etch mask and its impurities from a Cr sputter target, wafer holder, and chamber walls. The variations of the RIE Cr etching parameters, e.g., input power and gas pressure, have little influence on the density of PISD. At high gas pressures (>30 mTorr) high polymer deposition during ICP silica etching makes PISD sources grow into a micro-mask (like in Fig. 6). However, the suppressed polymer formation and sputtering of PISD sources at very low pressures result in the PISD-free surface. PISD behaviors according to the changes in ICP silica etching parameters, described in Sec. II, agree well with the above hypothesis.

FIG. 8. Schematics showing the mechanism of pit development from a micro-mask with etch time ($t_1 < t_2 < t_3 < t_4$). Black spots and the arrows in (a) and (b) denote a micro-mask consisting of a PISD source and deposited polymer, and the trajectory of ions.

Figure 7(a) shows the development of the PISD source into pits. White spots, located on the top of the pits, can be seen in that image, but they disappear at later stages of etching. Figure 8 depicts the mechanism of pit development with silica etch time at normal gas pressure (5–15 mTorr). Black spots and the arrows in Figs. 8(a) and 8(b) denote a micro-mask consisting of a PISD source and a deposited polymer, and the trajectory of ions. The etching rate is enhanced at a foot of a micro-mask due to increased ion flux from the reflection of ions from the island's sidewall, like a micro-trenching effect.^{4,18,19} We can also observe this effect in Fig. 6 (the trench along the bottom perimeter of the micro-mask), in which the sample was etched at a very high pressure (40 mTorr). Even though silica is etched at a neutral-limited (i.e., ion flux abundant) condition, the corner of an open area, due

to the shadowing of ion flux, can be etched at an ion-limited condition. This is the reason trenching effect, which occurs at an ion-limited condition, is observed over a wide range of silica etching pressures. As silica etching proceeds, a micro-mask is sputtered at normal gas pressure. After a micro-mask disappears, the depth of pit does not change (i.e., the pit depths in t_3 and t_4 are the same) because of the same flux of etching species arrives at the bottom of pit and the upper silica surface. Therefore, the depth of pit after silica etching is determined by the lifetime of a micro-mask, which is dependent on the initial micro-mask size and the preference of polymer deposition. However, the lateral dimension of the pit increases because of a high etching yield of ions at the edge region.¹⁰ As shown in Fig. 8(e), the etching yield varies with ion incidence angle and the sidewall angle of growing pit fixes at Θ_m .

The above-proposed mechanism for PISD formation is similar to that for the modification of sidewall roughness on an etched waveguide.^{12,10} Polymer buildup on a sidewall that is initiated by metal-compounds, acts as a micro-mask increasing the roughness of the sidewall. Smoothing of the sidewall with wafer temperature and when etched in a Si-clamp equipped ICP is a result of a thinned sidewall polymer. Therefore, a smooth sidewall, which is necessary in order to reduce the optical scattering loss in a waveguide, is also obtained from the process to reduce PISD on an etched surface.

IV. CONCLUSIONS

A mechanism is proposed to account for the PISD formation on an etched silica surface, which can also explain the roughness variations of an etched surface when RIE Cr mask and ICP silica etching parameters are changed. Metal-compounds, which are generated on a silica surface during the Cr dry etching in RIE, are verified as seeds for PISD. During silica etching, depending upon the applied etching conditions—especially gas pressure, PISD sources can grow. Pits are formed at the bottom of PISD sources as a result of the micro-trenching effect. “Water rinse” or “Ar-sputtering” before silica etching decreases the number of PISD sources and results in a smooth etched surface. The low-pressure process during ICP silica etching can also be beneficial for obtaining a PISD-free surface.

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