

CHARACTERIZATION OF DIELECTRIC LAYER, LASER DAMAGE AND EDGE RECOMBINATION IN MINIATURE SILICON SOLAR CELLS

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ABSTRACT

Miniature silicon solar cells ($8 \times 2.0 \text{ mm}^2$) are being fabricated for use in tandem-cell concentrator systems. Several factors combine to make the achievement of high efficiency problematical. These include surface, bulk and edge recombination. The latter is relatively important because the surface area of the edge of a small cell is a large fraction of the total surface area. Surface recombination in the cells is caused by the loss of passivating hydrogen beneath a conformal LPCVD SiN_x coating, induced by high temperature annealing. Bulk carrier lifetime degradation mechanisms that we have encountered include silicon crystal damage induced by laser scribing of the cells, which affects a relatively large proportion of the volume of the cell.

The Quasi-steady state photoconductance (QSSPC) measurement technique was used for the carrier lifetime degradation study. Firstly, a detailed study was undertaken of the carrier lifetime degradation due to the loss of hydrogen in conformally deposited LPCVD silicon nitride grown samples and the effect of hydrogenation on these layers, when subjected to various anneal times and temperatures. Additionally, LPCVD nitride was studied to determine whether it can be used as a layer that can prevent or resist possible contamination, induced by prolonged high temperature anneals. Secondly, a comparison was made between reference samples and samples that were exposed to laser scribing and dicing to determine whether laser scribing is suitable for the shaping of miniature silicon solar cells. Finally, cells with different pn junction designs were fabricated and tested to study edge recombination.

Keywords: QSSPC, carrier lifetime degradation, LPCVD nitride, laser-induced damage and edge recombination.

INTRODUCTION

Monocrystalline silicon solar cells, having a dimension of $8 \times 2.0 \text{ mm}^2$ are being developed for an intended application of mobile battery charging [1]. These silicon solar cells, to be used in conjunction with wider and narrow bandgap solar cells in a tandem stack, have to optimally harvest photons in the infrared light spectrum. The cells need to be thick and untextured. The best performing silicon solar cells we have fabricated previously had an open-circuit voltage of 602 mV, short-circuit current of 4.9 mA, and fill-factor of 77% under 1 sun illumination [2]. However, one-dimensional PC1D and numerical modeling predicts that

untextured $500\mu\text{m}$ thick silicon solar cells can reasonably achieve a short-circuit current (I_{sc}) of 5.3mA and open-circuit voltage (V_{oc}) of 680mV under one sun full-spectrum illumination [3, 4]. The biggest shortfall in the performance of fabricated silicon solar cells is the open-circuit voltage while the short-circuit current and the fill factor are comparable to modeled results. The fundamental mechanism that determines open-circuit voltage is carrier recombination. In the fabrication of the above-mentioned silicon solar cells, passivation and anti-reflection coating is realized by an oxide and overlying LPCVD nitride stack; formation of individual cells on the substrate wafer is by laser scribing; and contact window formation is by dry etching (RIE) [5]. RIE-induced carrier lifetime degradation, leading to poor performance of silicon solar cells, had been studied and the results have been presented elsewhere [6, 7]. Cells fabricated, having used the methods recommended by RIE-induced carrier lifetime degradation study, have gained a sharply increased performance but not up to the results, predicted by the modeling [2]. In this paper, we investigate the carrier lifetime degradation associated with the application of the oxide and LPCVD nitride stack and laser scribing; and the degree of edge recombination, contributed by certain types of cell, including the current cell design.

LOSS OF HYDROGEN IN NITRIDE LAYER

As discussed elsewhere [5], a stack of oxide and LPCVD nitride can be used in the fabrication of silicon solar cells. LPCVD nitride is used because it is hard and scratch-resistant; is conformal; is an excellent barrier for diffusion and selective oxide etch; is resistant to most acid and alkali silicon etchants; and is a good antireflection coating [8]. LPCVD nitride is particularly useful for our silicon solar cells because a series of acid and alkali etching steps occur after the deposition of the passivation and antireflection coating. McCann studied the effect of hydrogenation of LPCVD nitride films after annealing at 1000C for 60mins, and showed that the loss of hydrogen from the LPCVD nitride during a high temperature anneal can be restored by hydrogenation in forming gas annealing at 840C for 30mins [9]. A temperature of 840C was used in FGA because nitride is a good barrier to hydrogen at low temperature.

In our cell processing, a number of high temperature processes are involved after the deposition of LPCVD nitride. Therefore, the behavior of carrier lifetime of Oxide/LPCVD nitride stack with respect to extended high temperature anneal time will be studied and discussed.

P-type float zone <100> low resistivity 100 mm diameter silicon wafers were used in the experiments. They were etch-polished, cleaved into quarter-piece samples, cleaned and thermally oxidized to a thickness of 60 nm, followed by forming gas annealing (FGA) at 400°C for 30mins. Samples were then deposited with nitride (30nm) in the LPCVD furnace. Effective carrier lifetime of the samples was measured at an injection level of 10^{15} carriers per cm^3 using photoconductance decay [10, 11]. Samples were then annealed in nitrogen at 1000C for 180 mins. Following the nitrogen anneal, samples were hydrogenated in forming gas anneal at 840C for 30 mins first, followed by 60 mins of FGA at 840C. Carrier lifetime of these samples were measured after annealing in N_2 and hydrogenation steps. As shown in figure 1, the carrier lifetime of oxide/nitride stack samples, annealed at 1000C for 3 hrs was degraded drastically. The cause of the degradation is an increased surface recombination following the loss of hydrogen at the oxide-silicon interface. Hydrogenation of these samples in forming gas environment at 840C for 30 mins and 60 mins subsequently failed to regain the initial carrier lifetime.

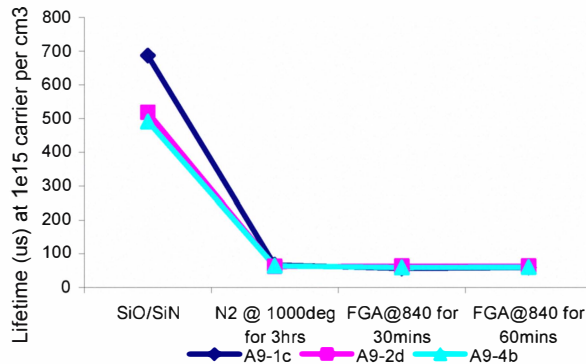


Figure 1: Behaviour of oxide/LPCVD nitride stack after high temperature anneal and hydrogenation.

It can be concluded that if oxide/nitride stack samples were annealed at 1000C for 3 hrs or more, the loss of carrier lifetime in these samples cannot be recovered by an 840C FGA anneal. The behavior of carrier lifetime of samples, having removed the nitride layer in hot phosphoric acid (170C for 10 mins, etch rate of ~ 3 nm per min) but leaving the underlying oxide, was explored. Following the nitride removal, samples were then subjected to forming gas annealing at 400C for 30 mins. As shown in figure 2, a recovery of carrier lifetime was observed for these samples. The likely reason of this recovery is the reintroduction of hydrogen to passivate the interface defects between the silicon and oxide, which can be realized by FGA, unhindered by a densified nitride coating.

A further experiment compared the carrier lifetime behavior of samples grown with oxide only with samples having oxide/nitride stacks, when subjected to lengthened high temperature anneals. P-type float zone <100> low resistivity silicon wafers were again etch-polished, cleaved

into quarter-piece samples, cleaned and thermally oxidized to a thickness of 60 nm, followed by forming gas annealing (FGA) at 400°C for 30 mins. Some of the samples were deposited with LPCVD nitride at a thickness of 30 nm. Following the nitride deposition, all samples were annealed at 1000C for 6 hrs in a nitrogen environment. The total anneal hour was increased by two fold, compared to the previous experiment, for the purpose of observing how the samples behave under an aggravated condition. Following the annealing, samples grown with nitride were processed in hot phosphoric acid to remove all of nitride. All samples were then annealed in forming gas at 400C for 30 mins. Carrier lifetime measurement was conducted after each processing steps and lifetimes of these samples were compared as shown in figure 3.

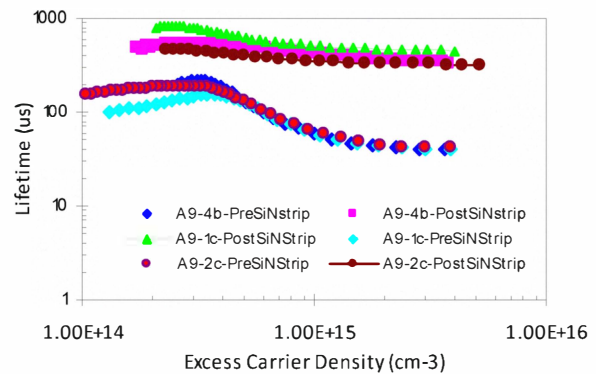


Figure 2: Stripping off the post-annealed nitride layer in H_3PO_4 followed by FGA.

Carrier lifetime of samples after the deposition of oxide or oxide/nitride stack is high as shown in figure 3. All samples suffered a substantial lifetime loss when subjected to high temperature anneal for 6 hrs. However, oxide/nitride stack samples regained their lifetime after stripping the nitride layer, followed by hydrogenation. The oxide samples suffered permanent lifetime degradation.

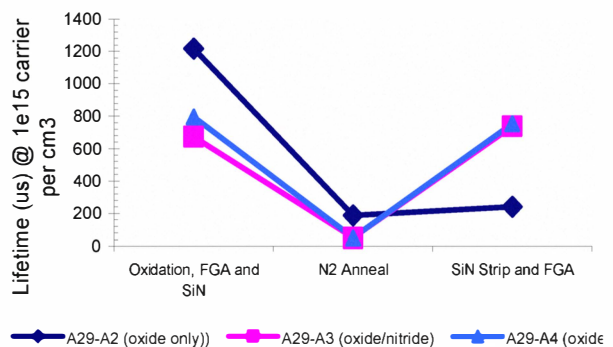


Figure 3: Carrier lifetime of oxide grown and oxide-nitride grown samples after prolonged high temperature annealing.

To identify if the oxide samples are associated with iron contamination, a technique of light soaking of the samples,

followed by measuring the carrier lifetime at different time intervals, was employed. This technique uses the illumination to dissociate possible Fe-Boron pairs in the sample first, and allowing dissociated Fe and B to recombine at a certain time interval after the illumination stops. Measurement of carrier lifetimes of samples at dissociated and associated Fe-B states allows capturing a well-defined characteristic crossover point between two lifetime curves, which is a clear indication of Fe contamination in the silicon bulk [12, 13]. Oxide samples were illuminated with light from a halogen lamp (0.5 W/cm² intensity) for 2 mins. The sample is placed on a cooled aluminium block (~ 10°C) to avoid a significant temperature increase, resulting in a faster association after switching off the light source. Carrier lifetime was measured immediately after the illumination and at 1 hr after the illumination was switched off. As shown in figure 4a, the carrier lifetime of oxide sample was increased sharply immediately after illumination, but decreased when carriers relaxed and recombined to the initial low lifetime after switching the illumination off. Figure 4b also indicates a clear characteristic crossover point (~ 1e14 carrier injection) between the dissociation and association states, which is the indication of association of Fe contamination in the samples. Subsequent work identified the presence of iron in the furnace. The conclusion is that LPCVD nitride is effective in blocking the diffusion of iron into silicon at elevated temperatures.

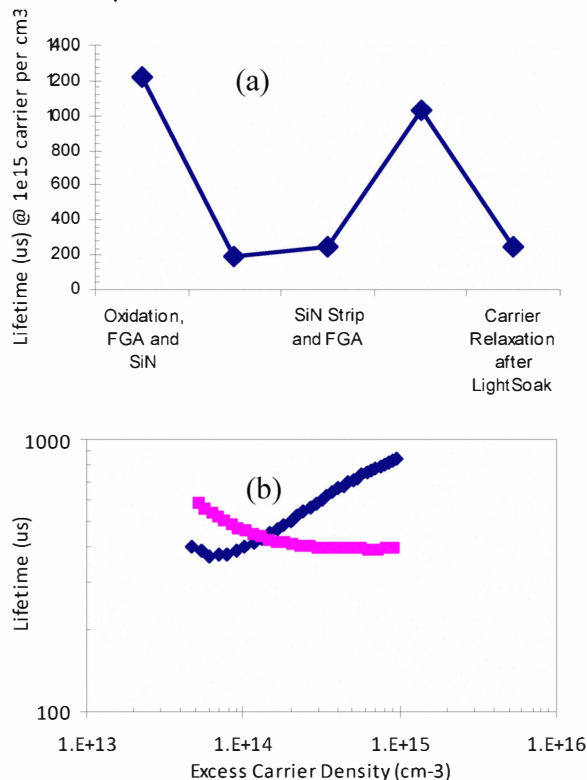


Figure 4: a) Carrier lifetime of oxide samples before and after light soaking, b) A graph, demonstrating a characteristic crossover (indication of iron

contamination in the sample) of pre-light soak and post-light soak curves.

LIFETIME DEGRADATION BY LASER-INDUCED DAMAGE

Shaping of our silicon solar cells [5] was by infrared laser scribing. Laser based processing has been incorporated into the development of several solar cell technologies – buried contact solar cell, laser-fired back contacts and emitter wrap through (EWT) for years [14, 15, 16]. In addition, lasers have been applied to p-n junction formation [17], laser doping of selective emitter contacts [18], isolation of shunted regions by laser [19] and patterning in large thin film solar cell modules [20, 21]. Laser process induces crystal damaged defects that propagate into the bulk of the crystalline silicon, sometimes leading to carrier lifetime degradation in the bulk [22]. Other researchers have shown that laser-induced defects can be minimized by the incorporation of a damage etch following laser processing [23, 24].

Laser processing was used in our cells as it offers the capability to form the desired shape of cells on the wafer in a faster and more convenient way than alternatives such as wet etching or a dicing saw. However, cells fabricated using laser scribing had performance lower than expected [2]. We used Nd:YLF (1047nm) pulsed laser to form individual solar cells in the wafer, as shown in the figure 5. As shown in the figure, individual solar cells were formed in the wafer by laser scribing from one side to the other side, while leaving only a tiny portion of each cell, attached to the host wafer (to be cleaved at the end of processing to separate the cell from the wafer). The reason for this was to minimize the area of unpassivated surface – the laser scribed regions could be passivated during processing. Following laser scribing, cells were etched to remove damage (TMAH at 80-90°C for 30 mins), which removed approximately 30 micron of silicon. Those cells, attached to the host wafer, were processed from the start until the metallization, followed by dicing to form individual cells for IV testing. The laser scribed edges cover almost 20% of the cell's surface area, and so any residual carrier lifetime degradation due to silicon crystal damage induced by the laser scribing would be significant.

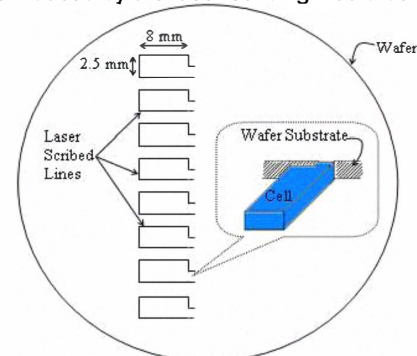


Figure 5: Formation of solar cells in the wafer by laser scribe technique. The laser scribe separates the cells

and host wafer completely. Non-laser scribe portion on the cell is the area that is still attached to the host wafer.

An experiment to analyze if there is substantial carrier lifetime degradation, associated with the application laser scribe method in the cells, was conducted by comparing the carrier lifetime of laser-scribed samples against reference samples that did not receive any laser scribing. In addition, the alternative technique of dicing with a high speed mechanical saw was explored. P-type float zone <100> low resistivity silicon wafers were first etch-polished and cleaved into quarter-piece samples. Samples were then divided into groups – reference samples, laser-scribed samples and diced samples. The scribed lines, the depths of which are the same as the samples' thickness, were equivalent to approximately 20% of total surface of the sample. Samples were then etched in TMAH ((CH₃)₄NOH) at 80-90°C for 30mins (~30 micron of silicon etched) for the removal of damage, induced by the laser and dicing. All samples, including the reference sample, were then cleaned and light-phosphorus diffused, followed by oxidation to passivate the surfaces. The carrier lifetimes of all samples were measured at the injection level of 1e15 carriers per cm³, as shown in figure 6. Of the samples, carrier lifetime of the laser-scribed samples was observed to be the lowest. Although both laser-scribed and diced samples received 30 mins of damage etch in TMAH, the damage induced by the laser scribe appears to have propagated deeply into the silicon crystal. A further experiment ("Diced Reference") was conducted using the reference samples. Formation of diced lines (~20% of total surface of a sample) was performed on the reference samples and the diced surfaces were left un-passivated (as it was diced). This condition is to mimic cells that are diced out of host wafer after the final passivation step.

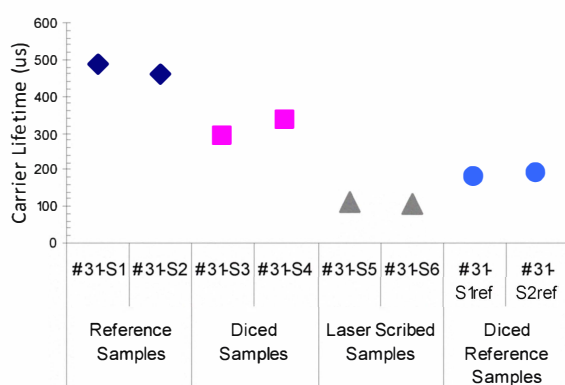


Figure 6: Comparison of carrier lifetime for reference, laser-scribed and diced samples.

As shown in the figure 6, "Diced Reference" samples had significantly higher lifetime than laser-scribed samples, but lower than diced samples that were etched and passivated.

EDGE RECOMBINATIONS

Edge recombination in small solar cells is a problem since small cells need to be processed in the host wafer before detachment for practical reasons of wafer handling. Edge recombination is particularly significant if the pn junction extends to the cell's edge, where the edge cut occurs, resulting in high dark saturation current, which is an equivalent of ideality factor 2. Catchpole showed that the loss in cell efficiency due to edge recombination in small cells where the emitter extends the final diced edge is significant [25]. McIntosh also reported that edge recombination caused an 18% decrease in fill factor from 0.77 to 0.63 for a 2 cm² buried contact cell [26]. Guo also discussed that the efficiency losses due to edge recombination, and incorporation of junction isolation technique in the fabrication of n-type Interdigitated Backside Buried Contact (IBBC) solar cells achieved the improvement in FF from 0.77 to 0.79, and efficiency from 19.2 to 19.9% [27]. Catchpole recommended that to make efficiency losses, due to edge recombination, negligible in the small cells the cut or diced edge should be kept 0.1 to 1 um away from the pn junction [25], in order to avoid cutting through the depletion region (which causes particularly large recombination rates).

The silicon solar cells that we developed are rather small. In this experiment, we fabricate cells with different pn junction designs that minimize the chances of the edge cut occurring on the pn junction, where the significant recombination exists. The designs of cell with different pn junctions are as shown in figure 7.

Fabrication of cells started with saw damage etch in HF:HNO₃, followed by making cell structures in the host wafer by laser scribing, as shown in figure 8. Following the laser scribe, samples were subjected to laser damage repair etch in TMAH at 80°C for 30 min. Samples were then phosphorus diffused, followed by growing an oxide/nitride stack. Samples were later processed in RIE using a mask to etch away n-diffusion at certain locations of the cells for the formation of cells with different pn junction designs. Following the RIE, cells were etched in TMAH to remove n-diffusion from RIE-processed regions, and stripping of the oxide/nitride stack completely. Samples were then re-grown with a new oxide/nitride stack that passivates the entire surface of the cells. Subsequently, samples were processed in RIE to make windows for n+ contacts formation at one side, followed by heavy doping of n+ diffusion. RIE processing continued on another side of samples to make windows for p contacts formation. For the process simplicity, no heavy doping on p contacts was performed. Samples were finally evaporated with metals, followed by dicing them out of the wafer to form individual cells for IV testing for comparing the edge recombination effects.

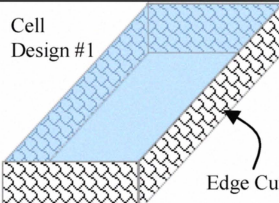
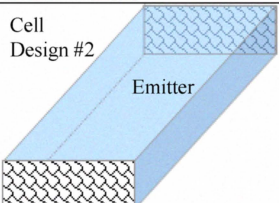
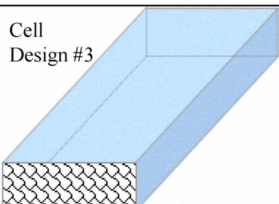
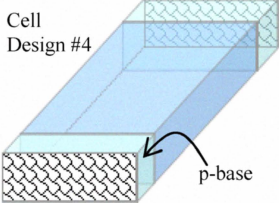
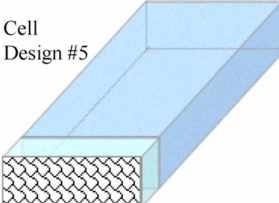
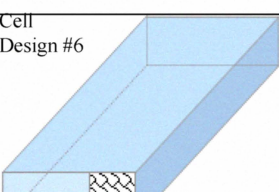
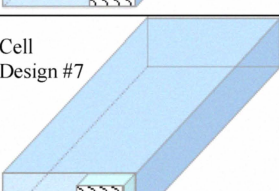
 <p>Cell Design #1</p>	<p>In this cell design, the emitter extends to the edges of the cell. The edge cut occurs on all lengths and widths of the cell.</p>
 <p>Cell Design #2</p>	<p>In this design, it is similar to cell design #1 except that the edge cut occurs only on two sides of the cell.</p>
 <p>Cell Design #3</p>	<p>The cell design #3, similar to the cell design #1 and #2 except that the edge cut occurs only on one side of the cell.</p>
 <p>Cell Design #4</p>	<p>In this design, the emitter, wrapped around the cell, is confined by keeping 1 mm away from the cell's cut edge. The edge cut does not lie on the pn junctions.</p>
 <p>Cell Design #5</p>	<p>This design is similar to cell design #4 but the emitter confinement is located only one side of the cell, where the edge cut takes place.</p>
 <p>Cell Design #6</p>	<p>This design of cell is similar to cell design #3, but the amount of edge cut, occurring on the pn junction is limited to a tiny area.</p>
 <p>Cell Design #7</p>	<p>Similar to the cell design #6 but the edge cut occurs only on a tiny area, which is kept 1 mm away from the pn junction.</p>

Figure 7: Silicon solar cells with different edge cut designs for edge recombination comparison study.

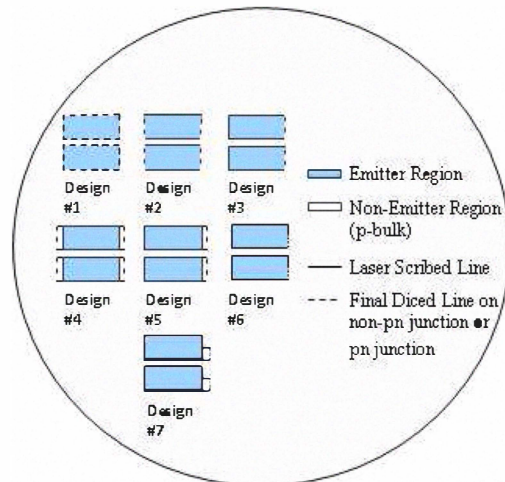


Figure 8: Samples with different pn junction designs formed by laser scribe and RIE. Non-emitter region were formed by processing of RIE on samples, followed by TMAH etch. Laser scribe line indicates that the laser scribe separated the cells and the host wafer totally. Dotted lines represent diced lines after the final processing to detach cells from the host wafer for IV testing and edge recombination comparison.

CONCLUSION

Samples grown with oxide/LPCVD nitride stack, when subjected to high temperature anneal at 1000°C for 3 hrs or more, result in irreversible carrier lifetime degradation unless the overlying nitride is stripped in hot phosphoric acid, followed by hydrogenation in forming gas annealing. Oxide only grown samples, when subjected to prolonged high temperature anneals (1000°C for 6 hrs or more), suffered permanent lifetime degradation (due to diffusion of iron, induced by the furnace, into the silicon). The degraded lifetime of oxide/LPCVD nitride stack samples, subjected to the same extended high temperature anneal as oxide grown samples, can be recovered by subsequent hydrogenation, following the removal of the densified nitride in hot phosphoric acid. The LPCVD nitride can be used as a barrier to stand off potential iron contamination into silicon at elevated temperatures.

Different shapes or designs of solar cell can be formed on the wafer by means of laser scribe or dicing. A comparative study, undertaken on the laser-scribed, diced and reference samples, highlighted that laser-scribed samples suffered the highest lifetime degradation among all samples. The likely reason of this degradation is the damage, induced by the laser scribe, penetrated deep into the silicon crystal, leading to bulk carrier lifetime degradation.

Edge recombination in small solar cells, where the edge cut occurs on the pn junction (depletion region recombination), is alarming due to the detachment of finished cells out of host wafer. Different Cell designs that

circumvent the edge cut occurring on the pn-junction are expected to give a clear comparison of the degree of edge recombination, associated with the cells. The fabrication of the cells, followed by testing of IV of these cells would reveal that which cell design is best suited for the least edge recombination occurrence (the results are expected to be presented in later publications).

The results that we achieved for the surface recombination induced by the loss of passivating hydrogen beneath a conformal LPCVD SiN_x coating due to high temperature anneals, and bulk recombination caused by laser-induced crystal damage; coupled with forthcoming results from the edge recombination study on different cell designs, we believe that a subsequent batch of cells fabricated would match the modeled results.

ACKNOWLEDGEMENTS

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