Nanostencil Lithography for fabrication of III-V nanostructures

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ABSTRACT

Nanostencil Lithography (NStL), while comparatively still in infant stages, is proving to be a viable option for low-cost and high resolution fabrication. An ideal stencil for NStL consists of a low-stressed silicon nitride membrane supported on a silicon chip with required patterned features in nanometer range that become apertures. The stencil is used as a shadow mask and placed in close contact on top of a substrate/wafer. This pair is then ready for either depositing metal through the apertures in the stencil using variety of deposition techniques or etching the substrate using dry etching techniques with stencil acting as a mask. The nanostencils were fabricated using focused ion beam writing on a silicon nitride window/membrane. We made well-ordered array of 700 nm diameter and 15 nm thick gold and chromium nanodots on III-V substrate. Metal layers were deposited using e-beam evaporator. The formed gold nanodots can be used for vapor-liquid-solid nanowire growth (bottom-up), while the chromium nanodots were used as a mask for reactive ion etching of GaAs structures, for instance, fabricating nanowires (top-down approach). We used the nanostencil directly as a mask for dry etching of InP substrate for making nanoholes array. Making these types of nanoholes in silicon oxide layer deposited on the top of III-V substrate opens the possibility to use in selective area growth of nanowires. Additionally, we fabricated optical nanoantenna structures to demonstrate other possible usage of NStL.

Keywords: Nanostencil Lithography, III-V fabrication, nanodots, nanopillars, nanoholes, e-beam evaporation, dry-etching

1 INTRODUCTION

Whilst Electron Beam lithography (EBL), Focused Ion Beam lithography (FIB), Nanoimprint Lithography (NIL) and Nanosphere Lithography (NSpL) are still popular choices for patterning high-resolution nanostructures, many alternatives are being developed to overcome the drawbacks of these techniques such as low-throughput (EBL, FIB), high cost (EBL, NIL) and repeatability (NSpL). One promising alternative is NStL[1-3]. While comparatively still in infant stages, NStL is proving to be a viable option for low-cost and high resolution fabrication especially, for proof-of-concept devices. A distinctive advantage of this technique is that it does not involve any resist, lift-off or other chemical processes and hence, can be applied to a variety of substrates. Being resistless means that NStL can be used to easily fabricate nanopatterns on curved topology as well as those requiring high temperature deposition processes. As it does not involve any chemicals, there is wide range of substrates that can be used[4], for example, plastic, glass, metal etc. without worrying about the compatibility of chemicals used for a particular developing-removing cycle. Furthermore, as this technique does not need lift-off for patterning, significant processing steps are reduced, thereby, speeding up the fabrication process. Another noticeable advantage of NStL is that a single stencil can be used for either etching or deposition. For example, metal can be deposited through the openings in the stencil, while the same openings can be used as a mask for reactive-ion etching. Additionally, the nanostencil can be used many times without significant damage to the openings. In the event of damage to the nanostencil due to repeated use, it is easy to clean the nanostencil using wet-etching techniques

Stencil printing has been used since ancient times for painting caves, stones, for art and craft. A significant use of the stencil printing has been in textile industry to make patterns on fabrics. The stencil consists of openings cut according to the design to be printed. This stencil is then placed on the fabric and a dye/pigment is applied. The dye/pigment will penetrate the openings and form the desired pattern on the fabric after removal of the stencil. Depending on the use, the stencil materials can be plastic, wood, paper or metal. This simple, fast and low-cost technique can be transferred to

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nano-regime with some modifications to fabricate nanostructures. As the patterns would be in nanometer scale, it would be impossible to use any mechanical milling tools to cut the openings. Furthermore, the stencil would also have to be thin to fabricate these small openings and at the same time robust for repeatable use. An ideal stamp for NStL consists of a patterned, low-stressed silicon nitride membrane that is supported on a silicon substrate. The substrate and stencil are placed in contact such that the silicon nitride membrane is touching the layer to be patterned. The pair is ready to either deposit a metal/dielectric using variety of physical or chemical vapor deposition techniques or etch the top layer using wet or dry etching with stencil acting as a mask. The stencil stamp can be fabricated using either EBL or focused ion beam (FIB). Figure 1 shows schematic of a typical NStL process.

In this paper our main aim is to fabricate well-ordered array of gold nanodots that can be used for growing nanowires using vapor-liquid-solid (VLS) growth technique. There are other potential applications of these nanodots structures such as plasmonic solar cells, biosensing applications, nanofluidics etc. Alternatively, instead of depositing, we also investigated NStL for dry etching III-V substrates to make top-down nanowires/nanopillars and nanoholes. Furthermore, we have also demonstrated the fabrication of nano-antenna.

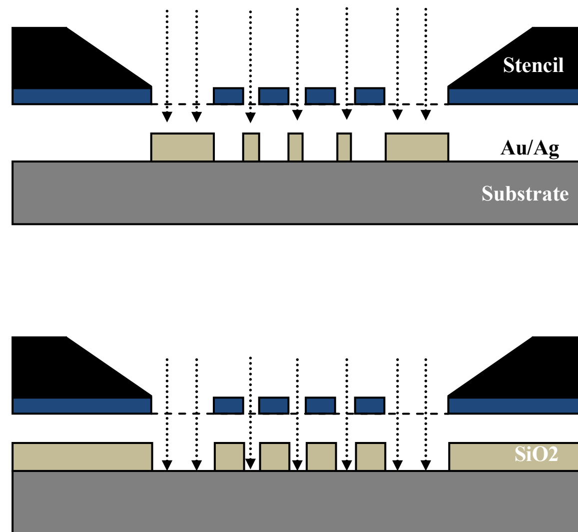

Figure 1: Schematic of NStL. Top: Using stencil for Au/Ag nanodots deposition, Bottom: Etching SiO2 layer to create nano holes

2 EXPERIMENTAL

2.1 Nanostencil Fabrication

A typical nanostencil fabrication involves two major steps:

- First step is the fabrication of silicon nitride window. Fabrication of silicon nitride window involves depositing a 100nm low-stress silicon nitride layer using either LPCVD or PECVD on a silicon substrate. The substrate is then patterned on the back side using photolithography and then etched in potassium hydroxide solution to obtain 0.5 mm square silicon nitride window. The silicon substrate is then diced into small pieces of 5 mm x 5 mm with the nitride window in the centre. This completes the fabrication of silicon nitride window.

- The second step involves making apertures in the membrane using either EBL or FIB. For EBL, a positive resist (PMMA or ZEP) is spun on the substrate and baked. The area where the aperture is required is exposed using electron beam. The resist is then developed to obtain openings in the resist. Afterwards, the silicon nitride is etched by reactive ion etching followed by resist removal to obtain apertures in the silicon nitride windows,

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thereby, completing the nanostencil fabrication. Using FIB is relatively easy as the openings are directly milled in the nitride membrane by using high energy gallium ions. However, FIB is not suitable for very high resolution and large area patterning and EBL is the only viable option in those situations.

In this work, we used readily available (SPI supplies) 100 nm thick low-stress silicon nitride TEM grids with a 1000 x 1000 µm square membrane supported on a silicon chip of 200 µm thickness instead of fabricating the same in-house. The main reason we went this path was that the TEM grids we bought were big enough to accommodate all our test structures and they are of very high quality. Having said that, it would be more appropriate to fabricate the window in-house if there is a need for large area patterning[5]. The apertures in the nitride membrane were patterned using FIB. A thin layer (1.5 nm) of gold was sputter coated using an SEM sputter coater (Denton Desk V) to avoid charging of the sample during FIB imaging. The grids were then loaded in FIB system (FEI Helios 600 NanoLab) for patterning. A 14 x 12 array of 300 nm holes with a pitch of 1.5 µm were fabricated in the nitride membrane using gallium ions at 30 kV and beam current of 28 pA. We also fabricated nanostencils consisting of 12 x 20 arrays of 300 nm holes using the same conditions for dry etching of III-V substrates. Figure 2(a) shows the fabricated nanostencil. Same nanostencil fabrication process was also used to fabricate optical nanoantennas.

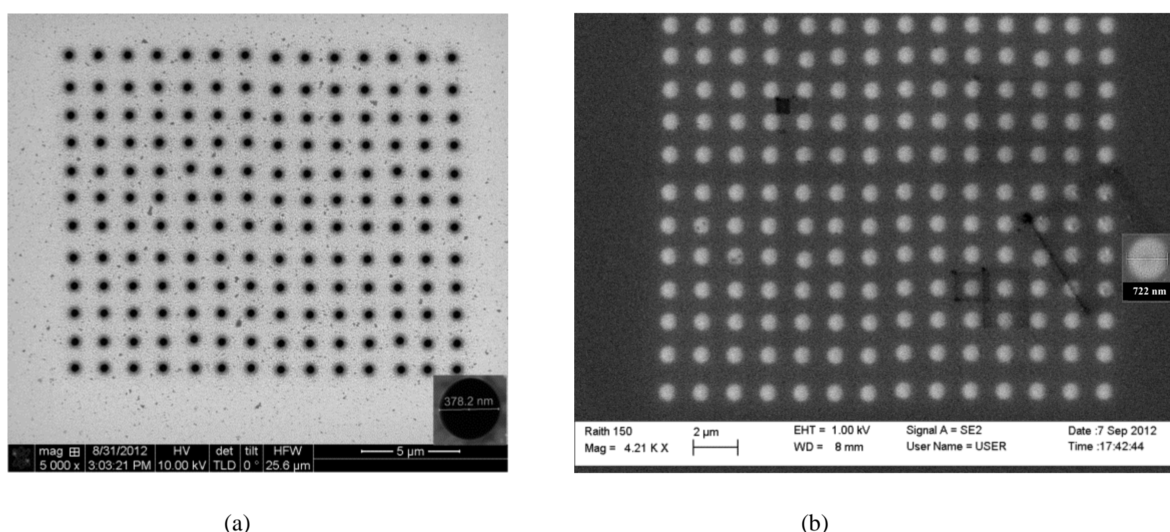

Figure 2: (a) Nanostencil fabricated using FIB having 12 x 14 array of 300 nm holes (b) 15 nm gold nanodots deposited using e-beam evaporator and patterned using nanostencil as in (a).

2.2 Metal Deposition

All metal deposition in this work was carried out using e-beam/thermal evaporator system (Temescal BJD-2000). The nanostencil was positioned in close contact to the GaAs substrate using a kapton tape in such a way that the patterned nitride membrane was touching the GaAs surface. This assembly was loaded into the evaporator and pumped to a base pressure of 5.0 E-6 Torr. A 15 nm thick gold layer was then deposited at a rate of 2 A^{o}/s. The deposition was done at a power of 3.5 kW. The nanostencil acts as a shadow mask and deposition would occur only in the openings, resulting in well-ordered gold nanodots. Following deposition, the nanostencil was carefully removed from the substrate to obtain the final nanostructures on GaAs samples. Figure 2(b) shows the resulting gold nanodots using nanostencil as in Figure 2(a). We also fabricated 15nm chromium nanodots using the same process. These chromium nanodots were then used as a mask for fabricating GaAs nanowires/nanopillars by dry etching. We also deposited 10 nm gold layer using nanostencil having apertures corresponding to optical nano-antennas.

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2.3 GaAs dry etching

The chromium nanodots were used as a mask for dry etching GaAs substrate to obtain nanowires/nanopillars. The nanostencil was also used directly as a mask for dry etching to obtain holes in InP substrates. All the dry etching was done using a load-locked inductively coupled plasma (ICP) reactive ion etching (RIE) system (Versaline LL). The GaAs and InP layers were etched using chlorine, hydrogen and argon chemistry. The flow rates were 10, 15 and 4 sccm respectively. The chamber pressure was 4 mT while the electrode and ICP powers were 100 and 1000 W respectively. The electrode temperature was set to 60°C and 160°C for GaAs and InP etching respectively. The etching was carried out for one minute. The etch rate of GaAs and InP using these conditions is 800 and 1100 nm/min respectively.

3 RESULTS AND DISCUSSION

We fabricated variety of nanostructures by e-beam evaporation and dry etching techniques using NStL. Initially, we patterned well-ordered gold nanodots using nanostencil shown in Figure 2(a). The resulting gold nanodots are shown in Figure 2(b). It can be seen clearly, that the resulting gold nanodot array is replica of the nanostencil. The diameter of gold nanodots is slightly bigger than the holes in the nanostencil. This enlargement can be possibly due to some gap between the stencil and the surface. The gap results in diffraction like effect during the evaporation and the resulting structures are blurred image of the apertures in the nanostencil[6]. This can be used as an advantage for fabricating larger nanodots than in the stencil by controlling the gap using spacers. The gold nanodots patterns shown here can be used for vapour-liquid-solid growth of III-V nanowires[7]. Traditionally, for VLS growth, gold nanoparticles are spin coated on the substrate. Though it is a simple technique, the gold nanoparticles are always randomly distributed on the surface and hence, it is not possible to grow well-ordered nanowires. Well-ordered nanodots are also required for various other applications such as plasmonic solar cells[8], DNA detection[9], etc. Plasmonics solar cells have received significant attention as the metal nanostructures at the top of the cell have proven to increase the efficiency of the device[8]. These plasmonic structures are typically silver particles on top of the solar cells having well-ordered distribution. Using NStL, it is also possible to fabricate such structures by evaporating silver through the nanostencil on the top surface of the solar cell. While researchers are using EBL for patterning well-ordered metal nanodots, this technique has the disadvantage of low-throughput and high cost. NStL is thus a better alternative for fabricating such structures.

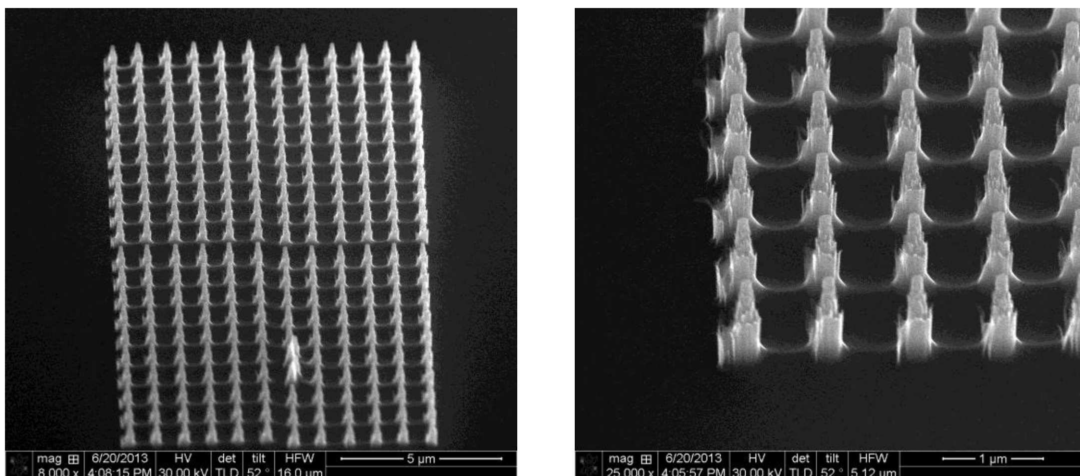

Figure 3: SEM images of GaAs nanopillars fabricated using NStL with chromium as etch mask.

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We fabricated a 12 x 20 array of chromium nanodots using NStL on GaAs substrate. We then used these nanodots as a mask for dry etching GaAs to form nanowires/nanopillars as shown in Figure 3. The resulting nanopillars were rough and more like nanoneedle shape, mainly due to mask erosion. This can be avoided by using probably nickel nanodots, depositing thicker chromium layer or with an intermediate silicon dioxide layer. However, it is important to note here that we were successful in using NStL for rapidly fabricating nanopillars in GaAs substrate. The thickness of the mask can be tuned to vary the sidewall profile, from vertical with thicker mask as needed for nanowires to tapered shape with thinner mask to fabricate nanoneedle. We also used the nanostencil directly to dry etch InP substrate. The resulting nanoholes are shown in Figure 4(a). The nanoholes are bigger than the openings in the stencil, again, likely due to gap between the surface and stencil.

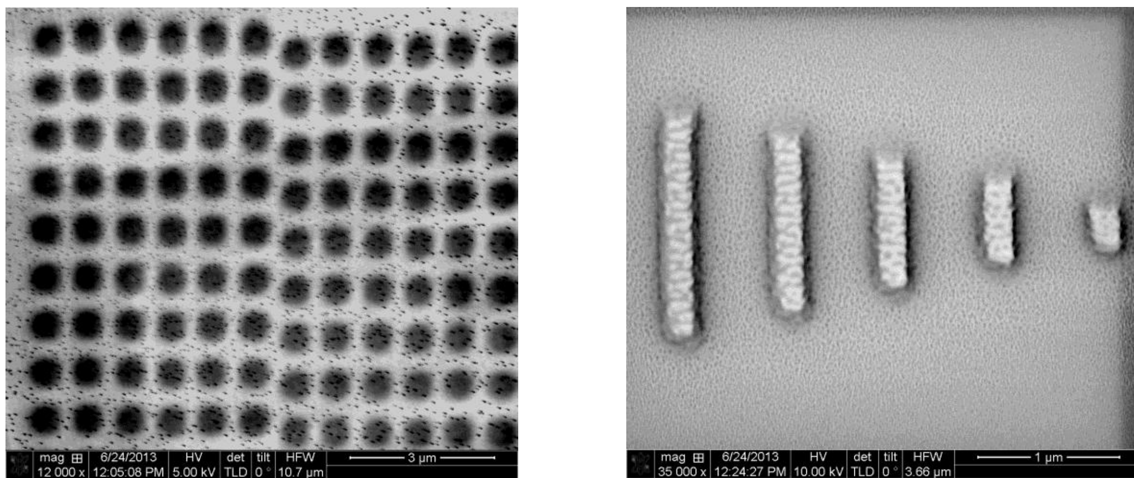

Figure 4: SEM images of (a) nanoholes etched in InP substrate with nanostencil and (b) Yagi-Uda nanoantenna made up of 10 nm evaporated gold layer.

Well-ordered nanoholes have a wide range of applications such as photonic crystals[10], surface plasmon resonance chemical and bio-sensors[11], focussing optics[12], optofluidics[13] to name a few. We are more interested in fabricating nanoholes array on a 30 nm thick silicon oxide film for growing core-shell III-V nanowires[14]. Core-shell nanowires have potential applications in semiconductor solar cells that can give better efficiency than traditional silicon solar cells[15]. Using our nanostencil, we can easily transfer the nanohole pattern to the silicon oxide layer by dry etching. However, to use the nanostencil directly as a mask, we need to coat a thin layer of chromium on the back side of the stencil to protect the silicon nitride membrane during dry etching. The reason being that the selectivity of nitride and oxide is nearly 1:1 and hence, by the time we etch 30 nm oxide, 30 nm nitride would also be etched resulting in thinner nanostencil. This idea will be exploited in near future. We also made nanostencil having optical Yagi-Uda nanoantenna[16] structure and transferred it onto GaAs substrate as a gold layer using e-beam evaporation as seen in Figure 4(b). Such nanostructures have potential applications in wireless optical communications, photovoltaics, nanosensing, optical metamaterials etc. There are few variations to the nanoantenna designs such as different structure and size; all of which can be easily fabricated and characterized with one step NStL.

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4 CONCLUSIONS

We have demonstrated the potential use of NStL as a way of fast and low-cost patterning of III-V nanostructures. We fabricated well-ordered gold nanodots on GaAs substrate for VLS nanowire growth. Instead of gold, silver, chromium and nickel nanodots are other options and can be deposited for applications in plasmonic solar cells and dry etching. Further, we made nanopillars and nanoholes arrays in GaAs and InP substrate respectively. We have shown that the same stencil can be used for deposition and etching. III-V nanopillars have variety of applications in photonics and photovoltaics, while nanoholes have potential applications from growing core-shell nanowires to biosensing and optofluidics. We also fabricated Yagi-Uda antenna to exhibit the possibility of fabricating wide range of nanostructures using NStL. The application of NStL is however, not limited to III-V nanostructures and can be applied to a variety of substrates such as silicon, glass, polymer, metal etc.

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