Aspects of Silicon Solar Cells:
Thin-Film Cells and LPCVD Silicon Nitride

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Declaration

This thesis is an account of research undertaken between April 1998 and July 2002 at The Centre for Sustainable Energy Systems, The Department of Engineering, Faculty of Engineering and Information Technology, The Australian National University, Canberra, Australia.

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and has not been submitted in whole or part for a degree in any university.

Michelle J. McCann
July, 2002
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Abstract

This thesis discusses the growth of thin-film silicon layers suitable for solar cells using liquid phase epitaxy and the behaviour of oxide/LPCVD silicon nitride stacks on silicon in a high temperature ambient.

The work on thin film cells is focussed on the characteristics of layers grown using liquid phase epitaxy. The morphology resulting from different seeding patterns, the transfer of dislocations to the epitaxial layer and the lifetime of layers grown using oxide compared with carbonised photoresist barrier layers are discussed. The second half of this work discusses boron doping of epitaxial layers. Simultaneous layer growth and boron doping is demonstrated, and shown to produce a 35µm thick layer with a back surface field approximately 3.5µm thick.

If an oxide/nitride stack is formed in the early stages of cell processing, then characteristics of the nitride may enable increased processing flexibility and hence the realisation of novel cell structures. An oxide/nitride stack on silicon also behaves as a good anti-reflection coating. The effects of a nitride deposited using low pressure chemical vapour deposition on the underlying wafer are discussed. With a thin oxide layer between the silicon and the silicon nitride, deposition is shown not to significantly alter effective lifetimes.

Heating an oxide/nitride stack on silicon is shown to result in a large drop in effective lifetimes. As long as at least a thin oxide is present, it is shown that a high temperature nitrogen anneal results in a reduction in surface passivation, but does not significantly affect bulk lifetime. The reduction in surface passivation is shown to be due to a loss of hydrogen from the silicon/silicon oxide interface and is characterised by an increase in $J_{oc}$. Higher temperatures, thinner oxides, thinner nitrides and longer anneal times are all shown to result in high $J_{oc}$ values. A hydrogen loss model is introduced to explain the observations.

Various methods of hydrogen re-introduction and hence $J_{oc}$ recovery are then discussed with an emphasis on high temperature forming gas anneals. The time necessary for successful $J_{oc}$ recovery is shown to be primarily dependent on the nitride thickness and on the temperature of the nitrogen anneal. With a high temperature forming gas anneal, $J_{oc}$ recovery after nitrogen anneals at both 900 and 1000°C and with an optimised anti-reflection coating is demonstrated for chemically polished wafers.
Finally the effects of oxide/nitride stacks and high temperature anneals in both nitrogen and forming gas are discussed for a variety of wafers. The optimal emitter sheet resistance is shown to be independent of nitrogen anneal temperature. With textured wafers, recovery of $J_{oc}$ values after a high temperature nitrogen anneal is demonstrated for wafers with a thick oxide, but not for wafers with a thin oxide. This is shown to be due to a lack of surface passivation at the silicon/oxide interface.
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<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>AIC</td>
<td>Aluminium Induced Crystallisation</td>
</tr>
<tr>
<td>AR</td>
<td>Anti-Reflection</td>
</tr>
<tr>
<td>ARC</td>
<td>Anti-Reflection Coating</td>
</tr>
<tr>
<td>a-Si</td>
<td>amorphous Silicon (no crystal structure)</td>
</tr>
<tr>
<td>BSF</td>
<td>Back Surface Field</td>
</tr>
<tr>
<td>BSR</td>
<td>Back Side (or Surface) Reflector</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
</tr>
<tr>
<td>APCVD</td>
<td>Atmospheric Pressure CVD</td>
</tr>
<tr>
<td>cat-CVD</td>
<td>Catalytic CVD</td>
</tr>
<tr>
<td>CC CVD</td>
<td>Closed Chamber CVD</td>
</tr>
<tr>
<td>EBEP CVD</td>
<td>Electron Beam Excited Plasma</td>
</tr>
<tr>
<td>ECR CVD</td>
<td>Electron Cyclotron Resonance CVD</td>
</tr>
<tr>
<td>ECR PACVD</td>
<td>Electron Cyclotron Resonance Plasma Assisted CVD</td>
</tr>
<tr>
<td>HR CVD</td>
<td>Hydrogen Radical CVD</td>
</tr>
<tr>
<td>HW CVD</td>
<td>Hot Wire CVD</td>
</tr>
<tr>
<td>LPCVD</td>
<td>Low Pressure CVD</td>
</tr>
<tr>
<td>PACVD</td>
<td>Plasma Assisted CVD (also called Plasma CVD)</td>
</tr>
<tr>
<td>PCVD</td>
<td>Plasma CVD (also called PECVD and PACVD)</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced CVD (also called plasma CVD)</td>
</tr>
<tr>
<td>remote PECVD</td>
<td>Plasma CVD with a remote plasma source</td>
</tr>
<tr>
<td>RF PECVD</td>
<td>Radio Frequency Plasma Enhanced CVD</td>
</tr>
<tr>
<td>RTCVD</td>
<td>Rapid Thermal CVD</td>
</tr>
<tr>
<td>SA CVD</td>
<td>Sub-atmospheric CVD</td>
</tr>
<tr>
<td>Cz</td>
<td>Czcholaski grown silicon</td>
</tr>
<tr>
<td>Dessis</td>
<td>a 2 dimensional computer program for solar cell simulation</td>
</tr>
<tr>
<td>DLARC</td>
<td>Double Layer Anti-Reflection Coating</td>
</tr>
<tr>
<td>EBIC</td>
<td>Electron Beam Induced Current</td>
</tr>
<tr>
<td>efficiency</td>
<td>(for solar cells) output energy/input energy</td>
</tr>
<tr>
<td>EFG</td>
<td>Edge-defined Film-fed Growth</td>
</tr>
<tr>
<td>ELO</td>
<td>Epitaxial Layer Overgrowth</td>
</tr>
<tr>
<td>EQE</td>
<td>External Quantum Efficiency</td>
</tr>
<tr>
<td>EWT</td>
<td>Emitter Wrap Through</td>
</tr>
<tr>
<td>FF</td>
<td>Fill Factor, equal to $I_{sc}V_{oc}/P_{max}$</td>
</tr>
<tr>
<td>PGA</td>
<td>Forming Gas (5% hydrogen in argon) Anneal</td>
</tr>
<tr>
<td>FZ</td>
<td>Float Zone</td>
</tr>
<tr>
<td>IAD</td>
<td>Ion Assisted Deposition</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>$I_{sc}$</td>
<td>Short Circuit Current</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium Tin Oxide, commonly used as an anti-reflection coating</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>i-type</td>
<td>intrinsic (undoped)</td>
</tr>
<tr>
<td>IQE</td>
<td>Internal Quantum Efficiency</td>
</tr>
<tr>
<td>J_em</td>
<td>emitter saturation current density</td>
</tr>
<tr>
<td>J_sc</td>
<td>short circuit current density</td>
</tr>
<tr>
<td>LBL</td>
<td>Layer-By-Layer</td>
</tr>
<tr>
<td>L_diff</td>
<td>diffusion length</td>
</tr>
<tr>
<td>LPE</td>
<td>Liquid Phase Epitaxy</td>
</tr>
<tr>
<td>L/W</td>
<td>the ratio of diffusion length to wafer width</td>
</tr>
<tr>
<td>mc-Si</td>
<td>multi-crystalline Silicon, the non-crystalline material with the largest grains</td>
</tr>
<tr>
<td>MG-Si</td>
<td>Metallurgical Grade Silicon</td>
</tr>
<tr>
<td>μc-Si</td>
<td>micro-crystalline silicon, grain sizes smaller than poly-crystalline silicon, but larger than nano-crystalline silicon</td>
</tr>
<tr>
<td>MIRHP</td>
<td>Microwave Induced Remote Hydrogen Passivation</td>
</tr>
<tr>
<td>n^+</td>
<td>heavily doped n-type</td>
</tr>
<tr>
<td>n^++</td>
<td>very heavily doped n-type</td>
</tr>
<tr>
<td>n-type</td>
<td>doped with atoms with single electron in their valance band, eg. phosphorous, arsenic or antimony</td>
</tr>
<tr>
<td>nc-Si</td>
<td>nano-crystalline silicon</td>
</tr>
<tr>
<td>ONO</td>
<td>a triple stack; SiO_2, SiN_x, SiO_2</td>
</tr>
<tr>
<td>p^+</td>
<td>heavily doped p-type</td>
</tr>
<tr>
<td>p^++</td>
<td>very heavily doped p-type</td>
</tr>
<tr>
<td>PC1D</td>
<td>a 1 dimensional computer programme for solar cell performance simulation [32]</td>
</tr>
<tr>
<td>P_max</td>
<td>the maximum operating power output</td>
</tr>
<tr>
<td>poly-Si</td>
<td>poly-crystalline Silicon, grain sizes in between multi and micro-crystalline silicon</td>
</tr>
<tr>
<td>p-type</td>
<td>doped with atoms with a single hole in their valance band, eg. boron, aluminium or gallium</td>
</tr>
<tr>
<td>QMS</td>
<td>Quasi Mono-crystalline Silicon, mono crystalline silicon that has been electrochemically etched to form porous silicon</td>
</tr>
<tr>
<td>R_ui</td>
<td>sheet resistance, typically measured after a diffusion or drive-in step using a 4-point probe</td>
</tr>
<tr>
<td>PRTP</td>
<td>Pulsed Rapid Thermal Processing</td>
</tr>
<tr>
<td>RGS</td>
<td>Ribbon Grown on Substrate</td>
</tr>
<tr>
<td>RTP</td>
<td>Rapid Thermal Process</td>
</tr>
<tr>
<td>sc-Si</td>
<td>single (or mono) crystalline Silicon</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>S_{front}</td>
<td>front surface recombination velocity</td>
</tr>
<tr>
<td>Si:H</td>
<td>Hydrogenated Silicon (usually amorphous or very small grained)</td>
</tr>
<tr>
<td>SiO_2</td>
<td>Silicon Oxide</td>
</tr>
<tr>
<td>SiN</td>
<td>Silicon Nitride</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon On Insulator</td>
</tr>
<tr>
<td>SPC</td>
<td>Solid Phase Crystallisation</td>
</tr>
<tr>
<td>S_{rear}</td>
<td>rear surface recombination velocity</td>
</tr>
<tr>
<td>SRH</td>
<td>Schottky-Read-Hall</td>
</tr>
<tr>
<td>SRV</td>
<td>Surface Recombination Velocity</td>
</tr>
<tr>
<td>SSP</td>
<td>Silicon Sheets from Powder</td>
</tr>
<tr>
<td>τ</td>
<td>lifetime</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>$\tau_{\text{eff}}$</td>
<td>effective lifetime</td>
</tr>
<tr>
<td>UHV sputtering</td>
<td>Ultra-High Vacuum sputtering</td>
</tr>
<tr>
<td>UMG-Si</td>
<td>Ugraded Metallurgical Grade Silicon</td>
</tr>
<tr>
<td>VHF-GD</td>
<td>Very-High Frequency Glow Discharge</td>
</tr>
<tr>
<td>$V_{\text{oc}}$</td>
<td>open circuit voltage</td>
</tr>
<tr>
<td>ZMR</td>
<td>Zone Melt Recrystallisation</td>
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Chapter 1

Introduction

World-wide energy usage recently reached $1.1 \times 10^{11}$ MWhours leading to the release of 6.1 billion metric tons of carbon equivalent [3]. In the developed world, we have grown to be reliant on a continuous supply of energy. Today, almost all of our energy needs are provided unsustainably by fossil fuels. Yet growth in the renewable energy sector has never been higher. In 2001, world-wide production of solar cells for terrestrial applications grew 40% to 402MW, with a predicted production of 620MW for 2002 [273].

Solar cells convert photons into electricity using the photovoltaic effect. Approximately 90% of solar cells produced worldwide are made from crystalline silicon, and the remainder from amorphous silicon and other materials. Crystalline silicon is more expensive than amorphous, but has a higher efficiency potential. The advantages of crystalline silicon are that it is an abundant material; non-toxic; shares research and infrastructure costs with the integrated circuit industry and has a relatively high efficiency potential. Significant research and development is also done on CIGS (Cu(In,Ga)(Se,S)$_2$) and CdTe cells, but the market penetration is currently low (less than 1% of total shipped power [63]). The main drawback of CdTe cells is the toxicity of the cadmium. The main drawback of CIGS cells is the relative rarity, and therefore cost, of the indium and the gallium. Organic solar cells, including cells based on the dye sensitised cells developed by Gratzel et al. [125] are another emerging technology.

Most commercial silicon cells are made using wafers produced by wire sawing from a crystal ingot and are approximately 200–500μm thick. The cost of the silicon is approximately 40% of the cost of a finished module. Thin-film silicon solar cells are typically 1–50μm thick and significant gains in efficiency can usually be realised with thinner cells. Thin-film silicon solar cells therefore show great potential to realise high efficiency cells at a lower cost than cells currently on the market. Most thin-film silicon cells are made by depositing or growing silicon either onto a permanent supporting substrate or onto a high quality silicon layer from which they are detached.

One of the reasons why there is not a higher usage of solar cells is the perceived cost compared with conventional forms of energy. The cost of solar cells is strongly influenced
by the efficiency. To date, the maximum solar cell efficiency reported at 25°C and under Global AM1.5 spectrum is 34.0% for a 1cm² GaInP/GaAs/Ge cell produced by Spectrolab. For single crystalline silicon, the efficiency record is 24.7% for a 4cm² cell, produced at the University of New South Wales using the Passivated Emitter, Rear Locally diffused (PERL) cell design [131]. The efficiency of commercially available solar cells is significantly lower than the high efficiency cells generally produced in a laboratory.

1.1 Silicon Solar Cells

Silicon is the second most abundant element in the Earth’s crust. It must be purified before it can be used to make solar cells. The first step is to produce Metallurgical-grade silicon (MG-Si), which is obtained by reacting silicon dioxide with carbon. This is further purified to produce poly-crystalline semiconductor grade silicon (SeG-Si). The production of SeG-Si is relatively energy and cost intensive. It involves firstly, generation of SiHCl₃ gas using a copper catalyst via the reaction;

\[
\text{Si} + 3\text{HCl} \rightarrow \text{SiHCl}_3 + \text{H}_2. \tag{1.1}
\]

The SiHCl₃ gas is then reacted with hydrogen gas at high temperatures to deposit silicon. This proceeds via the reaction [129];

\[
\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}. \tag{1.2}
\]

It is this second step that is particularly energy and cost intensive. To produce Czochralski (Cz) silicon, which can be used by both the integrated circuit and solar cell industry, a silicon seed crystal is dipped into a molten stockpile of SeG-Si. The seed is slowly pulled from the melt and continuously turned, to produce a single crystalline, cylindrical ingot [129].

Figure 1.1 shows the structure of a typical, high efficiency silicon solar cell. The top surface has an anti-reflection coating (ARC) and is textured to reduce reflection losses and to provide light trapping. The cell has a p-type base and an n-type emitter. In this cell design, the n⁺ region under the metal contacts is more heavily doped than the n-type region and is called a selective emitter. Use of a selective emitter means that doping levels under the metal contacts can be chosen to reduce contact losses between the metal and the silicon while doping levels elsewhere can be chosen to minimise recombination losses. The cell has metal contacts on both the front and back surfaces. By connecting these through an external circuit, power can be drawn from the cell, provided light is incident
on the front surface.

Figure 1.2 illustrates how a typical solar cell works. In part a) the p and n type materials are shown. The n-type material contains electrons that are not bound to the crystal lattice and are free to move. The p-type material contains holes that can effectively move around the crystal. The net charge in the material is zero, but the free carriers have the charge indicated. The n-type material is shown as thinner than the p-type to illustrate the case of an n-type dopant diffusion into a p-type wafer.

Part b) shows the p and n-type material in contact. The free carriers at the edge of the n-type material move into the p-type material, thereby forming the depletion region. By diffusing an n-type dopant such as phosphorous into a p-type wafer, a p-n junction is established.

In part c) of figure 1.2 a photon enters the cell. If it has energy greater than the band gap (1.1eV) of silicon, it may lose this energy to an electron and thereby create an electron/hole pair. The electron and hole are free to in about the cell, unless they come close to the junction, where the electric field will separate the carriers. This process is illustrated in part d) of figure 1.2. Also in part d) the metal contacts are shown. If these are connected through a load, current will flow and power can be extracted from the cell.
Figure 1.2: Operation of a typical solar cell. In part a) the p and n type regions with positive and negative free carriers are shown. In part b) the p and n type material are shown in contact, whereupon an electric field is established across the junction region. In part c) a photon enters the cell and creates an electron/hole pair in the p-type region and in part d) these carriers diffuse through the cell. If they reach the junction, the electron will be swept through and the hole repelled.
Silicon Solar Cells

Figure 1.3: The equivalent circuit for a solar cell: a current source, $I_{sc}$, in parallel with a diode with shunt ($R_{SH}$) and series ($R_S$) resistance as shown. The current from the light source is equivalent to the light generated current and is assumed equal to the short circuit current.

A solar cell may also be represented with the circuit diagram shown in figure 1.3 and can be described by a modified diode equation, assuming that the light generated current is equal to the short circuit current:

$$I = I_0 \left[ \exp \left( \frac{qV}{nKT} \right) - 1 \right] - I_{sc} \quad \text{(1.3)}$$

where $I_{sc}$ is the short circuit current, $I_0$ is the saturation current, $k$ is Boltzmann’s constant, $T$ is the temperature, $q$ is the charge on an electron and $n$ is the ideality factor, which varies between 1 and 2. Equation 1.3 is often written with $I$, $I_0$ and $I_{sc}$ replaced with $J$, $J_0$ and $J_{sc}$ where $J$ indicates a current density, or current per unit area. Equation 1.3 can be modified to include series and shunt resistances [345]:

$$I = I_0 \left[ \exp \left( \frac{V - IR_S}{nkt/q} \right) - 1 \right] - \left( \frac{V - IR_S}{R_{SH}} \right) - I_{sc}. \quad \text{(1.4)}$$

Figure 1.4 shows the IV curve of a typical solar cell with negligible series resistance and very high shunt resistance. $I_{mp}$ and $V_{mp}$ are the current and voltage at maximum power, respectively.

A solar cell is characterised by the short circuit current, $I_{sc}$, open circuit voltage, $V_{oc}$, fill factor, FF, and efficiency, $\eta$. The fill factor, FF, is defined by:

$$FF = \frac{V_{mp}I_{mp}}{V_{oc}I_{sc}}. \quad \text{(1.5)}$$
Figure 1.4: IV curve of a typical, 1cm² solar cell. The open circuit voltage, $V_{oc}$, is 600mV and the short circuit current, $I_{sc}$, is 37mA.

The efficiency, $\eta$, of a solar cell is defined as the ratio of output to input solar power, $P_{in}$:

$$\eta = \frac{V_{mp}I_{mp}}{P_{in}} = \frac{FF \times V_{oc}I_{sc}}{P_{in}}.$$ 

(1.6)

There are many sources of power loss for a solar cell. Losses in current may occur due to reflection from the surface, surface shading by the metal fingers, the loss of weakly absorbed, long wavelength light and due to recombination at the surfaces and in the bulk. Losses in voltage mainly occur through recombination. The fill factor is reduced by high series and low shunt resistances. Sources of series resistance include the bulk resistance of the cell material (both emitter and base), the bulk resistance of the metallic contacts and interconnects and the contact resistance between metallic contacts and the silicon. Shunt resistances are caused by leakage across the p-n junction.

Losses in reflection can be minimised by using an anti-reflection coating on the front surface and by texturing the cell. The probability of long wavelength light escaping from the cell can be minimised by including a light trapping scheme. This is particularly important for thin-film cells. Recombination is characterised by the minority carrier lifetime, $\tau$, which is the average amount of time a minority carrier survives before it recombines with
a majority carrier and is effectively lost to the cell. Thin-film cells can tolerate a lower minority carrier lifetime than thicker cells because the distance to the junction is smaller. Recombination at the surfaces is increasingly important for thin-film solar cells because the surface to volume ratio is reduced.

1.2 Thesis Outline

This thesis discusses the growth of thin-film silicon layers suitable for solar cells using liquid phase epitaxy and the behaviour of wafers with an oxide/nitride stack in a high temperature ambient.

Chapter 2 is a review of thin-film, crystalline (single-, multi-, poly- and micro-crystalline) silicon solar cells. Fabrication of a thin-film silicon solar cell requires deposition or growth onto a foreign or native substrate, optional recrystallisation and cell fabrication. Lift-off technologies also have a separation step that may be done before or after cell fabrication. Firstly, the merits of various deposition techniques are discussed. The subject is then divided into techniques that use native substrates and techniques that use foreign substrates. Research on foreign substrates is further divided into deposition above and below the melting point of commercially available glass. Research on native substrates is divided into ribbon growth, low cost silicon substrates and lift-off techniques. Cell designs, including optical and electronic considerations, that are of particular relevance to thin-film crystalline silicon solar cells, are discussed.

The greatest advantage of thin-film crystalline silicon solar cells is the reduced material usage and therefore the potential to lower costs. Chapter 3 introduces the Epilift technique, which is a lift-off technique developed by Weber and Blakers [337]. In this chapter, various aspects of layer growth are discussed, including the morphology resulting from different seeding patterns, the transfer of dislocations into the epitaxial layer and the lifetime of layers grown using oxide compared with carbonised photoresist barrier layers. The second half of the chapter discusses boron doping of epitaxial layers with a view to simultaneous layer growth and formation of a doping profile useful for solar cells.

Chapter 4 discusses oxide/nitride stacks on silicon where the silicon nitride is formed using low pressure chemical vapour deposition (LPCVD). An oxide/nitride stack on silicon can be applied to both thin-film and wafer-based silicon solar cells. The aim of this work was to determine if a nitride could be deposited in the early stages of a high-efficiency cell fabrication sequence. If so, then advantage can be taken of the properties of silicon nitride throughout cell processing, and the nitride can be used as an anti-reflection coating for the finished cells. Theoretical reflection losses from an oxide/nitride stack are calculated
as a function of both oxide and nitride thickness and the influence of nitride deposition on effective lifetime for high resistivity, p-type, (100) orientated wafers is discussed.

In chapter 5, the effect on surface passivation and on bulk recombination of annealing an oxide/nitride stack on silicon in a high temperature nitrogen ambient is discussed. High resistivity, p-type, (100) orientated wafers with a very light diffusion were used and the anneal was found to affect mainly the surface of the wafer. The effects of anneal temperature, anneal time and oxide and nitride thickness are discussed. A hydrogen-loss model is introduced to explain these observations.

The model developed in chapter 5 is applied for the results discussed in chapter 6 where the merit of various methods of re-introducing hydrogen to the silicon/oxide interface through an oxide/nitride stack are discussed. The methods are assessed by comparing emitter saturation current, $J_{sc}$, values. There is an emphasis on high temperature forming gas anneals. Other methods of recovering $J_{sc}$, including hydrogen plasmas, anneals, wet oxidations and second LPCVD depositions, are also discussed.

Chapter 7 discusses the effects of high temperature treatments of oxide nitride stacks on wafers with parameters (such as emitter sheet resistance) and features (such as texturing) likely to be useful for solar cell fabrication. The model developed in chapters 4-6 is used to explain the effects of high temperature treatments on these wafers.
Chapter 2

Review of Thin-Film Silicon Solar Cells

This chapter discusses thin-film, crystalline (single-, multi-, poly- and micro-crystalline) silicon solar cells. Firstly, the merits of various deposition techniques are discussed. The subject is then divided into techniques that use native substrates and techniques that use foreign substrates. Research on foreign substrates is further divided into deposition above and below the melting point of commercially available glass. Research on native substrates is divided into ribbon growth, low cost silicon substrates and lift-off techniques. Optical and electronic considerations for cell design are also discussed.

This section forms the basis of a review paper that was written jointly with Kylie Catchpole [84, 213] and updated comprehensively after the 17th European Photovoltaic Solar Energy Conference and Exhibition in October 2001. The sections discussing deposition on foreign substrates below the melting point of commercially available glass, ribbon growth, lift-off techniques and light trapping are primarily my own work. The sections on growth techniques, deposition on foreign substrates above the melting point of commercially available glass, deposition on low cost silicon substrates and cell designs are primarily the work of Catchpole.

2.1 Introduction

Thin-film crystalline silicon solar cells offer the potential for a reduction in cost of a finished photovoltaic module. For this reason, they are a strong contender for the next generation of commercially available solar cells. Crystalline silicon solar cells have the advantages of market dominance, non-toxicity, material abundance, stability, high efficiency potential and the ability to share research and infrastructure costs with the integrated circuit industry. Presently about half the cost of a finished module is due to the material itself. Furthermore, only about half the silicon in a Cz ingot is processed, the remainder is lost as sawdust. The potential for cost reduction when using material that does not require
slicing is therefore substantial. Thin film technologies reduce the amount of silicon used and hopefully the cost per watt of output power. Another advantage of thin-film silicon is that it may allow the use of poorer quality material for a given efficiency.

Cell efficiencies depend strongly on the details of cell fabrication and are often a poor guide to fundamental material properties. A relatively poor material combined with a sophisticated cell processing sequence may result in a substantially higher cell efficiency than a better material with a rudimentary cell processing sequence. Open circuit voltage, $V_{oc}$, is often the best measure of overall material quality since it incorporates recombination rates, including bulk, grain boundary and surface recombination. For thin cells made from good quality material, where surface recombination is more important than bulk, the ranking of materials on the basis of $V_{oc}$ is less certain.

Thin-film silicon cell fabrication techniques generally require deposition or growth on a foreign or native substrate, optional recrystallisation and then cell fabrication. Lift-off technologies also have a separation step which may fall before or after cell fabrication, and may mean that the deposition or growth step is avoided.

2.2 Silicon Layer Formation

Silicon layers may be formed from vapour or liquid phase silicon. The main techniques are chemical vapour deposition (CVD) and liquid phase epitaxy (LPE). LPE only occurs on the exposed silicon surface and not on masked regions of the wafer or on parts of the epitaxy reactor, so there is the potential for high chemical yields. CVD deposition is difficult to mask and can also occur on the reactor walls, so the growth process must be optimised to ensure high chemical yields. Temperature ranges of 350–1000°C have been used with LPE, and growth rates of up to 4µm/min have been achieved [154]. Processing temperatures for CVD range from a minimum of about 200°C, for plasma enhanced (PE) CVD, to a maximum of around 1200°C, for atmospheric pressure (AP) CVD. Deposition rates range from about 10nm/min for low pressure (LP) CVD up to about 10µm/min for rapid thermal (RT) CVD [110]. CVD is a commonly used commercial process, but LPE has only been used commercially in some specialised applications. Other deposition techniques that are used to produce thin-film silicon include ion-assisted deposition and sputtering.

2.2.1 Liquid Phase Epitaxy

Liquid phase epitaxy (LPE) is capable of producing high quality layers. It has been found that mobilities in LPE grown layers are only slightly lower than those in similarly
doped bulk silicon [18]. Layers with high minority carrier lifetimes can be grown, so LPE grown layers can be used to produce high efficiency solar cells. LPE is an attractive growth method because the layers are grown so that the silicon is always close to thermal equilibrium and consequently layers generally show a low density of structural defects and a low recombination activity at grain boundaries [323].

To make LPE commercially viable it is likely that growth rates and throughput will need to be increased. Rapid LPE has been pursued at the University of Konstanz [244]. A hole in the heating tube directly above the sample causes heat loss via radiation and therefore a strong temperature gradient at the substrate/growth interface. Growth rates of 2µm/min were achieved with a large tin melt for layers of 20–30µm with a resistivity of 1–2Ωcm. (Without the hole in the tube to cause the temperature gradient the growth rate was 0.2µm/min). Minority carrier diffusion lengths were 30–40µm if the furnace was unloaded directly after growth or 50–60µm if the furnace was cooled slowly before unloading. Self-supporting wafers have also been grown from a silicon seed. The same apparatus has also been used to achieve high growth rates with an indium melt [154]. Strong temperature gradients, the large melt and sonic agitation of the melt resulted in growth rates of 2–4µm/min at 930°C. Layers on (100) single crystalline silicon (sc-Si) had a pyramidally textured surface. A cell efficiency of 4.5% was achieved with a layer grown on a heavily doped sc-Si substrate. There was a low Voc, probably caused by shunting in the gaps between the pyramids.

It has been shown that LPE can be used to grow silicon on large areas. Layers of fairly uniform thickness have been grown on 5 inch wafers using LPE with a growth rate of 0.3–1µm/min [237]. An average minority carrier lifetime of 7µs was achieved over the whole of the epitaxial layer.

One of the features of LPE is that the incorporation of dopants depends on the temperature at which the layer is grown. Normally the thermodynamic driving force in LPE is the cooling of the melt, so LPE layers with a doping gradient and hence a drift field or pn-junction can be grown in one deposition step. At the University of New South Wales (UNSW) the aluminium content in a Sn/Al melt was adjusted to produce drift fields [39]. LPE can also be used to produce sharp dopant profiles (compared with diffusion, which results in error-function doping profiles) by changing the growth solution after each layer [187]. Multilayers were grown at Max-Planck-Institut für Festkörperforschung using an LPE centrifuge to move solutions from one chamber to the next. Growth rates were 0.2–2µm/min. A sharp p-type diffusion profile has also been obtained in a single growth step using boron and a tin melt at the Australian National University (ANU) [214] and is discussed in more detail in section 3.5.
Another implementation of LPE is the temperature difference method. With this method, the source is held at a higher temperature than the substrate to create a concentration gradient in the melt. Unlike conventional LPE, this is a steady state process and the temperature dependence of the element solubility does not affect the layer composition. A temperature gradient of 10°C/cm allowed a growth rate of 0.3μm/min at Institut für Kristallzüchtung [310]. Layers grown on multi-crystalline silicon (mc-Si) had a roughness of 2–6μm for a layer thickness of 30μm, mostly due to grooves at the grain boundaries. Lifetimes on layers grown on mc-Si were 5–10μs.

A comparison of tin (Sn) and indium (In) as solvents and gallium (Ga) and aluminium (Al) as dopants for LPE has been done at UNSW using single crystal substrates [282]. A sliding LPE system was modified so that layers using two different solvents could be grown on one substrate. Better performances were obtained with In than with Sn and with Ga than with Al. It was found that layers grown with Sn solutions or doped with Al had reduced mobility and lifetime. In contrast, at Institut National des Sciences Appliquées de Lyon, a Sn melt was used and the diffusion length was found to increase with the addition of Al and decrease with the addition of Ga [254]. A diffusion length of 280μm was achieved for an Al concentration of 0.9%.

2.2.2 Chemical Vapour Deposition

Chemical vapour deposition (CVD) is a costly and complex method for deposition of silicon. The cost of precursor and dilatant gases used in a CVD process is substantial. The advantages of CVD are that it is scalable and high quality layers can be produced.

CVD of silicon occurs generally either in a mass transport or kinetically limited regime [151, 246, 279]. The mass transport regime occurs at higher temperatures and deposition is not as uniform, but a cold wall reactor design can be used. In a cold wall reactor, the substrates are heated directly and as a result, deposition takes place on the substrate, while the walls of the reactor, which are cooler, remain uncoated. This has the advantage of improved chemical yield. The kinetically limited regime occurs at lower temperatures and deposition uniformity is better. Temperature control is critical in the kinetically limited regime, so a hot wall reactor, which is essentially an isothermal furnace, is required.

With atmospheric pressure (AP) CVD, deposition is generally mass transport controlled, so wafers must be in a low packing density configuration to allow access of gases to the wafer surfaces. With low pressure (LP) CVD, deposition is kinetically controlled and wafers can be vertical, with a high packing density. This can lead to lower costs than with APCVD, but, deposition rates are generally lower. The degree of crystallinity obtained
with LPCVD depends on the temperature. Films are fully crystalline at around 580–620°C; below this temperature range they are partly crystalline or amorphous [151, 198]. Pressures in the range 1–100 Pa are used for LPCVD and although these pressures are three to four orders of magnitude lower than in APCVD systems, deposition rates are typically only one order of magnitude lower at similar temperatures. This is because the precursor gas is diluted in APCVD systems, so the partial pressures of the precursor gas differ by only an order of magnitude or so between APCVD and LPCVD systems.

Rapid thermal (RT) CVD has been investigated at Fraunhofer ISE using an optically-heated APCVD system [110]. A special quartz wafer carrier is used that holds two layers of wafers and forms a volume that is separate from the rest of the reactor and into which the precursor can be injected. This avoids deposition on the walls of the reactor and allows a high chemical yield. Chemical yields of 76% have been achieved with a growth rate of 4μm/min. Thickness and doping non-uniformities are about 10% over 15cm. The quality of the deposited layers has been demonstrated with the achievement of an efficiency of 17.6% on an epilayer deposited on a heavily doped Cz wafer with the RTCVD system.

LPCVD is a suitable technique to deposit thin-film silicon on foreign substrates because it produces large grain sizes [36] and can be used to coat large substrates [215, 261]. When polycrystalline silicon deposited by LPCVD is compared with polycrystalline silicon formed at low temperatures by plasma enhanced (PE) CVD and RF sputtering, the Hall mobility is higher and strain inside grains is lower [261]. Other advantages are the possibility for simultaneous deposition on a large number of substrates, uniformity, possibility of in-situ doping and that LPCVD deposition leads to a low level of surface damage (compared with PECVD and sputtering) [215]. A disadvantage is that the material is highly defective, leading to low diffusion lengths [36]. In general, optical and electrical properties of in-situ doped LPCVD polycrystalline silicon are similar to those of polycrystalline silicon obtained by CVD and doped by implantation or thermal diffusion [193]. An increase in deposition time has been found to lead to an increase in both resistivity and grain size [193].

A general feature of CVD is that it allows the fabrication of high quality layers. At low temperatures (<600°C) the deposition rate is generally low [91]. The deposition rate can be increased by plasma activation of the precursor gas. With PECVD some of the energy required to break chemical bonds is provided by the plasma, so the temperature required to achieve a given growth rate can be lower. The high energy electrons in the plasma collide with and dissociate gas molecules, initiating the deposition reaction. In addition, bombardment of the wafer surface by positive ions from the plasma can change the surface chemistry, resulting in different film structures and growth rates. RF glow
discharges, which result in weakly ionised plasmas, are most commonly used for PECVD. Depending on the reactor configuration, substrates are either within or downstream of the plasma. If the substrate is downstream of the plasma, improved control of the reaction chemistry can be achieved, but it is often only possible to deposit on one substrate at a time. A disadvantage of PECVD is that the plasma can cause surface damage during deposition [158]. When PECVD is performed at 200-300°C the result is relatively high quality silicon with a high hydrogen content (10% atomic) [215]. This is a drawback in the process as bubbles appear in the film during the high temperature hydrogen evolution and this leads to macroscopic defect creation in the bulk. Low hydrogen content is beneficial to suppress spontaneous nucleation during deposition. Therefore, temperatures of about 500°C are used [215].

The plasma used in Electron Beam Excited Plasma (EBEP) CVD is formed by collision of energised electrons and gas molecules when a high current, accelerated electron beam is introduced into a pressure controlled gas chamber [159, 168]. The chamber is under vacuum at about 3.5 Pa. The collisions allow a highly dense plasma to be formed and this aids in the deposition of crystalline films [168]. The electron energy is controlled by varying the accelerating voltage. Deposition rate and structure strongly depend on the SiH₄ flow rate, but not on the substrate temperature. Hydrogen atoms play a key role in the formation of hydrogenated micro-crystalline silicon (μc-Si:H) [269].

It has been found that plasma-induced damage by EBEP-CVD can be reduced by depositing at temperatures over 420°C or annealing at temperatures over 500°C, and avoided altogether by making the electric potential of the substrate zero [240].

Hydrogen-radical (HR) CVD uses hydrogen radicals, generated by a microwave discharge of hydrogen gas, to decompose a source gas such as silane. The process takes place under a vacuum of about 80Pa. Hydrogen radicals are thought to promote crystallisation at the growing surface during deposition [185].

Electron Cyclotron Resonance (ECR) CVD is a form of PECVD that uses ECR to produce the plasma. Cyclotron resonance occurs when the frequency of an alternating electric field matches the frequency of electrons orbiting the lines of force of a magnetic field. The plasma densities are higher with ECR CVD than those achieved with conventional RF PECVD [332]. A specific advantage of ECR CVD is that it causes relatively little layer damage since the plasma source and substrate are well separated, and the operation pressure and plasma potential are low [220, 332]. In addition, substrate biasing allows for separate variation of plasma current and particle energy; there is the possibility of in-situ substrate pre-treatment and layer post-treatment; there are no hot filaments or active electrodes; a higher proportion of the process gas is used; and there is the possibility for
up-scaling [220]. A limitation of ECRCVD is the need for a very low pressure (0.1–1 Pa) and a high intensity magnetic field, which increases the cost of the system.

Hot wire (HW) CVD is a simple and low cost procedure [209, 252]. Source gases such as \( \text{SiH}_4 \) and \( \text{H}_2 \) are pyrolytically decomposed on a filament catalyst that is heated to about \( 1300–2000^\circ\text{C} \) and located several centimetres from the surface of the substrates. Gas-phase reactions and thin-film deposition take place from the atomic and molecular precursors generated at the filament surface. The process takes place under high vacuum (around 10 Pa). Doping can be readily achieved by adding \( \text{B}_2\text{H}_6 \) or \( \text{PH}_3 \) to the source gas [209]. Single step fabrication of poly-Si [252] and reasonable deposition rates with good doping control are achievable [77, 88, 335]. Large area deposition is achievable by optimised superposition of precursors in a multiple filament configuration [335].

### 2.2.3 Recrystallisation

Once a silicon layer has been deposited, there are several improvements in quality that can be made by further crystallisation. The most common high temperature recrystallisation technique is zone melting recrystallisation (ZMR). Low temperature crystallisation techniques include laser crystallisation, solid phase crystallisation (SPC), rapid thermal processing (RTP) and vacuum and furnace annealing. Although crystallisation adds another step to the process, it allows the use of a lower cost, lower quality initial silicon deposition.

The advantages of doing SPC on amorphous silicon (a-Si) are that it is simple and cost effective, requires a low process temperature, produces a relatively high quality active layer, is easy to scale up [21] and allows the possibility of in-situ phosphorous doping [202]. SPC may be performed at temperatures above 500°C, and produces large grain sizes but the throughput is limited [265]. Pulsed rapid thermal processing, PRTP, is a very fast method of SPC [363] as is aluminium-induced crystallisation (AIC).

The grain size obtained with all random nucleation and growth crystallisation processes is inversely related to the nucleation rate [280]. The rapid temperature changes achievable with pulsed laser illumination allows nucleation to occur near the melting point of silicon without melting a glass substrate. Since the nucleation rate is low near the melting point of silicon, grain sizes obtained with laser crystallisation tend to be large.

For all growth temperatures and crystallisation techniques, there is generally a log-normal distribution of grain sizes [40]. The average grain size is a factor of 3–5 smaller than the maximum grain size. This is important because the open circuit voltage of a cell decreases significantly if even a small proportion of the grains have a diffusion length that is small compared to the majority of grains in the cell.
2.3 Foreign Substrates: Low Temperature Deposition

Glass is the most widely used foreign substrate for low temperature deposition. Kaneka have reported a maximum cell efficiency of 10.1% [356]. Most other groups are still working on layer deposition.

The deposition of crystalline silicon onto substrates at low temperatures is advantageous in that it can reduce stress in the silicon film due to thermal expansion mismatch, diffusion of impurities into the active layer from the substrate may be reduced, and a wide variety of substrates, including glass, can be used. Successful commercial application requires an inexpensive substrate, a high deposition rate and a methodology that may be transferred to large area fabrication. The effective diffusion length must be greater than the width of the cell for high carrier collection probability. This may be achieved by either having a grain size greater than the cell width or by ensuring grain boundaries are electrically inactive.

Commercial glass substrates are limited to temperatures less than 600°C [47], or 500°C for borosilicate glass [77]. Glass is an obvious substrate candidate for low temperature deposition, having advantages of low cost, transparency, electrical insulation, chemical stability, weather resistance and easy recycling [9, 47, 222, 283]. The thermal expansion coefficient is dependent on the type of glass. At lower temperatures, it is generally closer to silicon.

The two main drawbacks of low temperature deposition are that it leads to small grain sizes, and hence lower quality material, and that deposition rates are usually low. Deposition rates are typically around 10 Å/s, however rates of 47 Å/s and 50 Å/s for the deposition of μc-Si:H have been demonstrated by Saitama University [285] and Electrotechnical Laboratory respectively [119]. Specific disadvantages of glass include a lack of surface passivation at the glass/silicon interface (especially when compared with multi-crystalline silicon (mc-Si) substrates) [222], the possibility of impurities diffusing from the substrate into the deposited layer and that the thermal expansion mismatch is a potential problem [47].

Grain size is a particularly important consideration for deposition at low temperatures [41] and tends to dominate electrical properties for low grain size material. Deposition at temperatures below the melting point of glass, tends to result in micro-crystalline (μc)- or nano-crystalline (nc)-Si, while higher temperatures allow the formation of poly-Si. The difference between these two forms has been comprehensively explored by Bergmann [40, 41]. In essence, nc- or μc-Si results in material with a lifetime that is dominated by recombination or trapping and it is often necessary to use a p-i-n cell structure with this material. The intrinsic region of p-i-n cells is used to separate regions of
high recombination from the region where charge separation occurs [40]. Poly-Si allows p-n-junction cells to be fabricated and these tend to allow higher $V_{oc}$ values than p-i-n cells [41]. P-n junction cells can be used when recombination is not dominated by the potential barriers at the grain boundaries. The height of these barriers is dependent on trap density, intra-grain doping density and again, grain size.

Many groups have optimised/investigated deposition at low temperatures by depositing on silicon. In addition, a number of other substrates have been used for low temperature deposition. The motivation for use of these substrates is varied. Metal coated glass, SnO$_2$ coated glass, or metal only substrates such as stainless steel, have the advantage of providing electrical contact to the silicon. SnO$_2$ is a transparent conductor and hence may be used on either the substrate or superstrate surface. Silicon oxide, or quartz, (SiO$_2$) is often used as a deposition surface, as an intermediate step between silicon and glass. Quartz allows high temperature steps after deposition to improve material quality or fabricate cells. Quartz generally contains less impurities than glass. Other substrates that have been investigated are ZnO and Mo.

This section has been divided into groups reporting cell results (section 2.3.1), groups reporting on crystallographic nature and characteristics of silicon layers on foreign substrates (section 2.3.2) and groups who are experimenting with low temperature deposition techniques on silicon substrates (section 2.3.3).

### 2.3.1 Foreign Substrates: Cell Results

Kaneka Corporation have developed the STAR structure (naturally Surface Texture and enhanced Absorption with a back Reflector) [354, 355]. The cell structure is shown in figure 2.1 and is glass/back reflector/n-i-p poly-Si/ITO/Ag. To form the cells, silicon seeding layer is deposited and undergoes an excimer laser anneal (ELA) [352]. Deposition of the active layer is by plasma CVD, which allows hydrogen passivation of the grain boundaries [352, 354, 356]. A 10.1% efficient cell has been demonstrated [356]. This cell had a $V_{oc}$ of 539mV, was 2.0µm thick and had an area of 1.2cm$^2$. The highest $V_{oc}$ recorded to date is 549mV [357]. The 10.1% cell was made using the second generation STAR design. This includes a textured back reflector, which improves light trapping, particularly in the long wavelength range. Grain orientation is generally (110) preferred and parallel to the growth direction. No clear grain boundaries have been observed [352].

The maximum processing temperature is 550°C. Increasing the cell thickness was found to lead to a decrease in $V_{oc}$ and FF, and a rise in $J_{sc}$. STAR cells are generally characterised by high $J_{sc}$, FF and low $V_{oc}$. The low $V_{oc}$ may be due to carrier recombination in the i-layer [355]. Maximum deposition rates achieved to date are 10–15Å/s, and Kaneka are
aiming for 25–30Å/s [357]. As an indication of the rate at which the cell results have been improving, efficiencies (and cell thickness) reported in the past were 1995 - 5.9% (4µm thick) [227], 1996 - 6.8% (6µm thick) [353] and 1997 - 9.8% (3.5µm and 2.5µm thick) and 9.3% (1.5µm) [355, 354]. The 10.1% efficient cell was reported in 1998 [356]. Kaneka have also demonstrated a uniform efficiency; 5×5 mm² cells were cut with a laser scribe from a 100×100mm² cell and efficiency was around 10% for each sub cell. Plasma CVD deposition over an area of 300×400mm² has demonstrated a uniform thickness (±5%) [357].

The micromorph tandem cells developed at the Institut de Microtechnique (IMT) at Université de Nuechâtel have resulted in an 8.5% efficient cell with a \( V_{\text{oc}} \) of 531mV. A \( V_{\text{oc}} \) of 592mV has also been reported [207, 208]. The silicon was deposited at 220°C, is \( \mu c\)-Si:H and has been developed as the bottom cell of a tandem cell. Deposition has been onto a sodium-free, glass substrate that is maintained at about 350°C [207]. Also at Université de Nuechâtel, moderate deposition rates (26Å/s) have been achieved by using a combination of hotwire deposition and the very high frequency glow discharge (VHF-GD) technique, which allows a low defect density. The hydrogen dilution ratio was found to influence the crystallographic orientation [208].

PECVD has been used at Forschungszentrum Jülich (FZJ) to deposit \( \mu c\)-Si:H on ZnO coated glass. The deposition temperature was 200°C, and the rate was 1.5Å/s. A cell efficiency of 7.5% (\( V_{\text{oc}} \) of 499mV) was achieved for a 2µm thick cell, and a \( V_{\text{oc}} \) of 540mV for a 0.5µm thick cell. The ZnO was applied using magnetron sputtering and chemically
textured to aid light trapping properties [322]. FZJ have also worked with IMT on ‘Inverted’ or ‘substrate’ cells with an n-i-p structure, made using the VHF-GD technique [114]. The n-i-p structure allows higher deposition temperatures for the n and i-layers which are not as sensitive to high temperatures as the p-type layer. The material is μc-Si:H and cells of 2μm thickness with 7.3% efficiency (V_{oc} of 517mV) and of 4μm thickness with 6.9% efficiency (V_{oc} of 481mV) have been achieved at deposition rates of 6.8Å/s and 10Å/s, respectively. ZnO/Ag on glass and on stainless steel have been used as substrates. The ZnO is deposited using sputtering and may then be etched to create a textured rear surface [114]. FZJ have also used RF PECVD to deposit μc-Si:H p-i-n cells on ZnO coated glass. An efficiency of 7.1% and a V_{oc} of 464mV were achieved for a 1.6μm thick cell deposited at 6Å/s. At a deposition rate of 9Å/s, an efficiency of 6.2% and a V_{oc} of 507mV was achieved for a 1.1μm thick layer. The cells had a p-i-n structure and deposition rates and thicknesses were quoted for the i-layer. An increase in deposition pressure and in H₂ dilution led to an increase in both fill factor and V_{oc} [257]. The substrate temperature was kept at less than 200°C.

Pacific Solar, a spin-off company from the University of New South Wales, have developed a technology called CSG (crystalline silicon on glass). Layers are less than 2μm thick and all component layers of the cell and ARC can be deposited in a single vacuum deposition step. Modules, rather than single cells are fabricated. The highest reported module efficiency is 7.25%, for a 480cm² area. The V_{oc} was 21.4V [31].

At the Debeye Institute, University of Utrecht, stainless steel (SS) has been used as a substrate, and a 1.5μm thick i-poly-Si:H layer deposited by HWCVD resulted in a cell with an efficiency of 3.7% [251]. Two different deposition regimes are used: poly1 and poly2. Poly1 uses high hydrogen dilution and results in the immediate nucleation of grains and porous layers. Poly2 uses a lower hydrogen dilution and results in fewer nucleation sites and consequently larger grain sizes. Deposition in the poly2 regime does not become crystalline until the thickness is greater than 50–80nm [277]. For a cell structure of SS/n-type μc-Si:H (RF CVD)/i-type poly-Si (HWCVD)/p-type μc-Si:H (RF CVD)/ITO grid, results were 0.6% (658mV) for a poly2 layer only and 3.7% (343mV) for a poly1/poly2 combination layer [277].

At Osaka University, Al is evaporated at room temperature onto a glass substrate with an ITO film, and a-Si is deposited by PCVD. A vacuum anneal is done at 500°C for 2 hours which dehydrogenates the sample, a further 20 minute anneal is then done at 700°C which allows for the eutectic reaction to take place. PCVD is used to deposit microcrystalline p and n-layers and a poly-Si layer on the Al-Si seed layer at 250°C. The cell structure is p-i-n and individual layer thicknesses are 20nm, 2.5μm and 30nm. The
p and n layers are \( \mu c\)-Si and are deposited by PCVD at 220°C. The seed layer has been found to lead to larger grain sizes, about 200–400nm on the seeded layer, which is 2–3 times larger than grain sizes grown on non-seeded layers. A 2.6% efficient cell with a \( V_{oc} \) of 340mV was demonstrated using this process and a glass substrate [302].

At Laboratoire de Physique des Interfaces et des Couches Minces (LPICM) and Laboratoire de Génie Electrique de Paris (LGEP), an efficiency of 2.1% and a \( V_{oc} \) of 370mV have been demonstrated for cells deposited by HWCVD onto SnO\(_2\) coated glass. The cell structure was; SnO\(_2\) coated glass/p-i-n/Al and the thickness of the p-i-n layers was 500Å/1.5\( \mu m \)/500Å [132]. The unusual aspect of this work is that a low filament temperature (1500°C) was used. It was found that at high filament temperatures, impurities can contaminate the growing films. LPICM and LGEP have also deposited \( \mu c\)-Si onto glass using the HWCVD technique [132]. The filament temperature and concentration of silane in H\(_2\) were optimised to 1500°C and 3.5% respectively. This gave a crystalline fraction of 95%, a crystallite size of around 500Å and a deposition rate of 1.8Å/s at a substrate temperature of 300°C.

A 4.5\( \mu m \) thick \( n^+pp^+ \) structure has been deposited onto glass at the Institut für Physikalische Hochtechnologie. Deposition was by PECVD with simultaneous laser irradiation from either a ~Ar\(^{+}~ or KrF excimer laser. A maximum cell efficiency of 1.6% (370mV) was achieved [12].

\( \mu c\)-Si has been deposited onto both glass and SnO\(_2\) by groups at Sharp and The Electro technical Laboratory. A balance must be struck between texturing for light trapping and maintaining good quality crystal growth. A conductive ZnO layer was used that influences the texturing. At substrate temperatures of 250°C, PECVD was used to deposit layers of 0.5–1.5\( \mu m \). Increasing the thickness of the ZnO layer on a SnO\(_2\) substrate resulted in an increase in both \( V_{oc} \) and fill factor. A \( V_{oc} \) of 445mV was achieved with a 1\( \mu m \) thick ZnO layer [351].

An initial \( V_{oc} \) value of 200mV has been reported by Groupe de Microélectronique et Visualisation (GMV) and Laboratoire de Génie Electrique de Paris (LGEP) who have used LPCVD to deposit silicon onto Corning 7059 glass [261]. Layers were 5\( \mu m \) thick and deposited at 1.9Å/s. A vacuum anneal at 600°C was used to crystallise the layers which were amorphous when deposited [261].

At the State University of New York and the Biota Corp., the pulsed laser technique has been used to crystallise a-Si:H films [329]. A 7\( \mu m \) thick layer of a-Si:H deposited by DC glow discharge onto a Mo substrate at 300°C was crystallised with a Nd:glass pulsed laser and resulted in grain sizes in excess of 0.2\( \mu m \) and a maximum minority carrier diffusion length of 22\( \mu m \). The high diffusion length was due to hydrogen passivation of the grain
Table 2.1: Summary of foreign substrates: Cell results. The results column shows efficiency and/or $V_{oc}$. Lifetime ($\tau$) and diffusion length ($L_{\text{diff}}$) have been quoted when cell results were not available.

Deposition temperatures of 190–275°C have been reported by the Universität Wien and the Universitat de Barcelona. The HWCVD technique has been used to deposit 1µm thick layers of silicon on glass substrates. Higher temperatures were found to increase the grain size and number of deep defect levels within the bandgap. A mobility lifetime product equating to an equivalent minority carrier diffusion length of 1.6µm was reported [77].

Deposition of poly-Si on SiO$_2$ at 300°C has been demonstrated at Japan Advanced Institute of Science and Technology (JAIST), using the HWCVD technique [158]. Generally, the crystalline fraction is about 80% and growth occurs in narrow (nm diameter), columnar grains, surrounded by thin a-Si regions. Preferential growth is in the (200) direction and there are few microtwin [143]. One particular film had a large optical absorption, a lifetime of 0.6–0.75µs and a carrier diffusion length of 5µm. The ratio of a-Si/poly-Si was controlled by varying the flow rate ratio of SiH$_4$ to H$_2$ and the maximum crystalline fraction achieved was over 90% [158]. Also at JAIST, catalytic CVD has been used to deposit poly-Si on fused quartz. Deposition temperatures of 350°C and rates of 10Å/s were achieved [149].

Table 2.1 shows a summary of cell results for layers deposited on foreign substrates at low temperatures.
2.3.2 Foreign Substrates: Crystallographic Structure

Low Temperature (≤300°C)

Low temperature deposition is advantageous because it avoids a high thermal budget. It is usually associated with lower quality material and very low deposition rates. In spite of this, a moderate deposition rate of 11.5Å/s has been achieved in a cooperation between Fuji Electric Corporation and Kawasaki Heavy Industries whereby μc-Si:H has been deposited by Electron Beam Excited Plasma (EBEP) CVD onto Corning 7059 glass substrates at temperatures of 185–240°C [269]. A higher SiH₄ flow rate was found to result in an increase in deposition rate but a decrease in both crystalline fraction and grain size. The deposition rate was achieved using no H₂ dilution, and therefore at lower cost. The substrate temperature was found not to strongly influence deposition rate or film structure [269].

ZnO coated glass has been used as a substrate and deposition rates of 1–2Å/s have been achieved at a low substrate temperature of 250°C in a collaboration between groups in Portugal and Bulgaria (ISEL, FCT/UNL, CL-SNES and IST). The deposition technique was closed chamber (CC) CVD and μc-Si:H was deposited [225].

Silicon for seeding layers has been deposited on c-Si and on SiO₂ using EBEP CVD in a collaboration between Toyota Technological Institute, Kawasaki Heavy Industries and Chubu Electric Power Company [159, 168]. Silane was used without hydrogen as the source gas to deposit films at a rate of 1Å/s and this resulted in grain sizes of around 10nm [159]. The hydrogen concentration of the grown layers was 19% (much greater than that obtained with RF plasma CVD). It was found that growth was crystalline over a wider range of growth conditions than with RF plasma CVD.

A substrate deposition temperature of 250°C has been used at the National Tsing Hua University where poly-Si:H was deposited by Electron Cyclotron Resonance (ECR) CVD onto Corning 7059 glass. H₂ and SiH₄ were used as deposition gases and the H₂ content was varied from 90% to 99%. At H₂ concentrations of about 95%, the deposited silicon became microcrystalline, rather than amorphous, with the largest grains being observed at a concentration of 98% hydrogen. Grain sizes in the order of microns and a crystalline fraction of close to 100% were achieved [156]. ⟨110⟩ and ⟨111⟩ were the preferred grain orientations with ⟨110⟩ becoming more dominant at larger grain sizes. In-situ phosphorous doping was demonstrated and found not to greatly affect the grain size, grain geometry or crystalline fraction [156].

Deposition of silicon by ECR CVD onto Corning 1737 glass at a temperature of 120°C has been demonstrated by the Pennsylvania State University [22]. Argon (instead of
Table 2.2: Summary of foreign substrates: Deposition at temperatures ≤300°C. The results column shows deposition rate (in Å/s), the type of material that resulted or grain sizes (gs).

<table>
<thead>
<tr>
<th>Group</th>
<th>Substrate</th>
<th>Result</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fuji &amp; Kawasaki</td>
<td>glass</td>
<td>μc-Si:H</td>
<td>[269]</td>
</tr>
<tr>
<td>ISEL, FCT/UNL CL-SNES &amp; IST</td>
<td>ZnO coated glass</td>
<td>1–2Å/s, 10nm (gs)</td>
<td>[225]</td>
</tr>
<tr>
<td>TTI, KWI &amp; CEPC</td>
<td>c-Si &amp; SiO₂</td>
<td>μm (gs)</td>
<td>[159, 168]</td>
</tr>
<tr>
<td>NTHU</td>
<td>glass</td>
<td>poly-Si</td>
<td>[22]</td>
</tr>
<tr>
<td>PSU</td>
<td>glass</td>
<td>220Å (gs)</td>
<td>[185]</td>
</tr>
<tr>
<td>TUAT</td>
<td>glass</td>
<td>4.2Å/s</td>
<td>[217]</td>
</tr>
<tr>
<td>KHU</td>
<td>–</td>
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</tr>
</tbody>
</table>

hydrogen) was used as a dilution gas for the silane, but the resulting films were non-crystalline. With a hydrogen to helium dilution ratio of 3:1 and a substrate temperature of 120°C, poly-Si was demonstrated.

At the Tokyo University of Agriculture and Technology, μc-Si:H has been deposited on glass at a substrate temperature of between 150–250°C using the hydrogen-radical CVD method [185], a form of remote PECVD [5]. Grain sizes of 220Å were achieved and the role of hydrogen radicals was investigated. The conductivity of the films was discovered to be a function of the film thickness [6]. Thin films of poly-Si were also formed using PECVD on laser crystallised seed layers. The seed layers were formed using a pulsed XeCl excimer laser to crystallise 100nm thick layers of μc-Si and PECVD was done at 250°C [7].

At Kyung Hee University, poly-Si has been formed using inductively coupled plasma CVD. A deposition rate of 4.2Å/s and grain sizes of 1200Å were achieved at a deposition temperature of 300°C [217].

Table 2.2 shows a summary of deposition on foreign substrates at temperatures below 300°C.

Moderate Temperature (300–500°C)

Much deposition of silicon onto glass substrates is done at a moderate temperature that is still well below the melting point of glass. This captures some of the advantages of higher temperature deposition while maintaining a fairly low thermal budget.

A deposition method termed the ‘hot wire cell method’ was used at the Tokyo Institute of Technology to deposit poly-Si on glass. The method involves the reaction of gases (SiH₄ or Si₂H₆) with a heated tungsten filament placed perpendicular to the substrate. Rates of 28Å/s and a (220) orientation preference were achieved at a substrate temperature of 325°C [157]. At the Tokyo Institute of Technology, silicon has also been deposited onto glass using the layer-by-layer (LBL) technique [5]. Deposition has been done at a substrate temperature of 360°C using fluorinated precursors, SiF₅H₃ (where n+m=3) [5].
technique involves deposition by hydrogen radical (HR) CVD of 4nm of silicon, exposure to atomic hydrogen and repetition of these two steps. Hydrogen is important for the crystallisation as it breaks Si-Si bonds at the substrate surface. Too much atomic hydrogen may cause degradation of the crystal structure and increased surface roughness.

A six filament HWCVD system has been used to achieve deposition rates of 10Å/s at the Universität Stuttgart for the deposition of µc-Si onto glass [335]. Optimisation of the temperature showed that 300–400°C allowed both good material quality and maximum grain size. This temperature range allowed a balance of hydrogen desorption and surface diffusion of the film-forming precursors. Atomic hydrogen treatment was found to improve the electronic quality due to defect passivation [335].

Moderate grain sizes have been reported by the University of Utrecht where poly-Si has been deposited on a Corning 7059 glass substrate by the HWCVD technique at a temperature of 430°C and a rate of 5.5Å/s [250, 252]. The resulting film had a crystal volume fraction of 95%, and an average grain size of 70nm. The film had a minority carrier diffusion length of 0.3µm [250, 252].

At the Hahn-Meitner Institut (HMI), deposition rates of 8Å/s and 0.8Å/s have been used to deposit undoped and doped µc-Si respectively at substrate temperatures of 340°C by ECRCVD on soda lime glass. Reducing the amount of SiH₄ (compared with H₂) led to an improvement in crystallinity as did increasing the plasma density and decreasing the deposition rate. A maximum grain size of 50nm and in-situ layer doping of up to 5×10²⁰/cm³ was achieved [220].

HMI have also worked in conjunction with Ferdinand-Braun Institut für Höchstfrequenztechnik and the Universität Wien to achieve deposition rates of 1.7Å/s and an average grain size of 20–30nm using temperatures around 350–450°C. For these results, µc-Si was deposited onto borosilicate float glass by microwave plasma-enhanced sputtering (MPES) [222], also called high density plasma vapour deposition (HDPVVD). MPES is the superposition of DC or RF magnetron sputtering process with independent excitation of a dense plasma by microwave electron cyclotron resonance. Some of the sputtered particles are in ionic form when deposited, which leads to increased surface mobility of the deposited material [222]. Low pressures of about 0.005–0.1 Pa are required [224].

The Korea Advanced Institute of Science and Technology (KAIST), have deposited poly-Si on glass by RF PECVD using SiF₄ and H₂ at a substrate temperature of 350°C [86]. Columnar grain sizes of about 100nm were observed on both glass and SiO₂. The surface roughness was found to be greater for the silicon deposited on glass and increased with increasing film thickness [86]. KAIST also used ECR plasma CVD in conjunction with the layer-by-layer (LBL) technique to deposit µc-Si on Corning 7059 glass [196]. Helium was
Table 2.3: Summary of foreign substrates: Deposition at temperatures between 300–500°C. The results shown are deposition rate (in Å/s) or grain sizes (gs).

<table>
<thead>
<tr>
<th>Group</th>
<th>Substrate</th>
<th>Result</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTT</td>
<td>glass</td>
<td>28Å/s</td>
<td>[157]</td>
</tr>
<tr>
<td>US</td>
<td>glass</td>
<td>10Å/s</td>
<td>[335]</td>
</tr>
<tr>
<td>UU</td>
<td>glass</td>
<td>5.5Å/s</td>
<td>[252, 250]</td>
</tr>
<tr>
<td>HMI</td>
<td>soda lime glass</td>
<td>8 &amp; 0.8Å/s, 50nm (gs)</td>
<td>[220]</td>
</tr>
<tr>
<td>HMI, FBIH &amp; UW</td>
<td>glass</td>
<td>1.7Å/s, 20-30nm (gs)</td>
<td>[222]</td>
</tr>
<tr>
<td>KAIST</td>
<td>glass</td>
<td>4.5Å/s, 100nm (gs)</td>
<td>[86, 196]</td>
</tr>
<tr>
<td>Fujitsu</td>
<td></td>
<td>40nm (gs)</td>
<td>[211]</td>
</tr>
</tbody>
</table>

used as the source gas in ECR and substrate temperatures varied between 180–550°C. The ratios of He:SiH$_4$ were 1:1, 4:1 and 9:1. At ratios of 4:1 and 9:1, the volume fraction of μc-Si increased with temperature and was greater than 90% for temperatures above 550°C. Deposition rates at a temperature of 410°C for ratios 1:1, 4:1 and 9:1 were 4.5Å/s, 1.9Å/s and 1.25Å/s respectively. Above 410°C, the deposition rate for a gas ratio of 9:1 remained unchanged, but increased for ratios of 1:1 and 4:1. At a gas ratio of 1:1, a deposition rate of 6.5Å/s was achieved at a substrate temperature of 550°C, but this resulted in amorphous silicon. It is believed that the change from amorphous silicon occurs during the long period of exposure to He plasma in the LBL deposition [196].

At Fujitsu Laboratories, UHV sputtering has been used for the formation of poly-Si on glass at substrate temperatures of between 350–500°C. Grains were mostly of (220) orientation with a size of 40nm [211].

Table 2.3 shows a summary of deposition on foreign substrates at temperatures of 300–500°C.

**Higher Temperature (500–600°C)**

Deposition at temperatures closer to the melting point of glass is advantageous in that higher deposition rates are allowed and larger grain sizes result. The higher temperatures also usually mean that the embodied energy content and costs are higher. A high deposition rate has been demonstrated by Groupe de Microelectronique et Visualisation, where a-Si has been deposited onto glass using sub-atmospheric CVD [267]. This involves thermal dissociation of silane molecules just below atmospheric pressure at temperatures of between 500–600°C. Deposition rates in excess of 28Å/s and a thickness uniformity better than 10% over a 25cm$^2$ area were achieved. The film was amorphous and required crystallisation to form poly-Si. At present, the deposition conditions have not been optimised and the quality is generally less than that of films deposited by LPCVD [267].

Large grain sizes of up to 25μm deposited at 2.8Å/s have been demonstrated in a
collaboration between the National Renewable Energy Laboratory (NREL) and the State University of New York, where poly-Si has been grown from a silicon-metal solution onto glass at substrate temperatures of 450–650°C [326]. Tin and indium were used for the metal. With a Ti wetting layer, grain sizes of up to 25μm and good hole mobility were achieved but the photoconductivity was limited. In comparison, layers grown without a wetting layer exhibited smaller grain size, poorer electron mobility but improved photoconductivity [326].

A high substrate temperature of 550°C has been used by groups at GMV, LGEP, and LPICM, where LPCVD was used to deposit poly-Si layers of 10–20μm thickness on glass [36]. Hydrogen passivation was achieved using hydrogen dissociation on a hot tungsten filament. This method was chosen because there is a high hydrogen production, no damage to the surface and the high quality of the silicon helps to increase the diffusion coefficient for hydrogen [36].

A thickness of 6.5–7.7μm and grain sizes of the same order were achieved at Universität Stuttgart using Ion Assisted Deposition (IAD) [45, 51, 239]. Seeded glass was used as the substrate and films had a (100) orientation preference. During IAD deposition, silicon is evaporated from a melt using an electron beam, and then partly ionised and accelerated towards the substrate. The deposition takes place under a high vacuum of 10⁻⁵ Pa and substrate temperatures of 550–700°C are used. The advantages of IAD include the possibility of high deposition rates on large areas and the use of low energy ions, which is beneficial to the structural quality at low temperatures [190].

High temperature deposition has also been demonstrated at the University of New South Wales using borosilicate glass as a substrate and solution growth of poly-Si [283]. Three methods of depositing silicon on glass from solution growth were investigated. The first method was silicon particle seeded growth, which was done at 550°C using a Sn/Al alloy. Growth was non continuous, but resulted in large grain, poly-Si. Crystals were of good quality, mostly (111) orientation and had reasonable adhesion to the glass substrate. The second method was growth on bare glass from solutions containing Al or Mg. This was done at substrate temperatures of 370–570°C. On bare glass only, silicon islands resulted with (111) preferred orientation. On sandblasted bare glass, a continuous poly-Si film from solutions containing Al and Mg was grown below 600°C. Rheotaxy (growth near the softening point of glass) enabled a 10cm² area of 30μm thickness and a grain size of 50–350μm to be realised. Adhesion was good and the preferred orientation was (110) [283].

Microcrystalline films with a crystalline fraction of almost 100% have been achieved at South Bank University. The substrate was metal coated Corning 7059 glass and the ECR PACVD technique was used with a substrate temperature of 510°C [332]. Films
Table 2.4: Summary of foreign substrates: Deposition at temperatures between 500–600°C. The results shown are deposition rate (in Å/s) and grain sizes (gs).

<table>
<thead>
<tr>
<th>Group</th>
<th>Substrate</th>
<th>Result</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMV</td>
<td>glass</td>
<td>28Å/s</td>
<td>[267]</td>
</tr>
<tr>
<td>NREL &amp; SUNY</td>
<td>glass</td>
<td>25μm (gs)</td>
<td>[326]</td>
</tr>
<tr>
<td>GMV, LGEP, &amp; LPICM</td>
<td>glass</td>
<td>-</td>
<td>[36]</td>
</tr>
<tr>
<td>US, ANTEC &amp; UE</td>
<td>seeded glass</td>
<td>6–7μm (gs)</td>
<td>[45, 51, 239]</td>
</tr>
<tr>
<td>UNSW</td>
<td>sand blasted glass</td>
<td>50–350μm (gs)</td>
<td>[283]</td>
</tr>
<tr>
<td>SBU</td>
<td>metal coated glass</td>
<td>μc-Si</td>
<td>[332]</td>
</tr>
</tbody>
</table>

were also deposited at 280°C and then given a 6 hour anneal at 580°C. On Pd/glass, Ni/glass and Ti/glass substrates, the grain sizes that resulted were 85nm, 34nm and 33nm respectively [332].

Table 2.4 shows a summary of deposition on foreign substrates at temperatures of 500–600°C.

Foreign Substrates: Recrystallisation

Grain lengths of 200μm have been produced at Columbia University using a technique called sequential lateral solidification (SLS) [291]. SLS involves LPCVD deposition of a-Si on SiO₂, and this is irradiated by an excimer laser through a patterned mask. After the exposed areas have melted, the film is moved relative to the mask and another laser pulse is used to irradiate the silicon. This process has several remarkable features. Firstly, the substrate is at room temperature. Secondly, it may lead to production of large sc-Si regions on glass and thirdly the log-normal distribution of grain sizes and random grain boundary positions is avoided. At present, the formed grain boundaries are essentially parallel. Since the less energetically favourable grains eventually die out, the grain width increases slightly as the distance from the crystallisation origin increases [291].

Crystal grains around 100μm long have been achieved using two laser crystallisation techniques developed at the Institut für Physikalische Hochtechnologie in conjunction with the Hahn-Meitner Institut. The techniques, lateral epitactic growth and lateral explosive crystallisation, have been used to crystallise a thin layer of amorphous silicon deposited on borosilicate glass [8, 9, 10]. The crystallised layer is to be used as a seed layer for an epitaxial thickening process. The principle of both techniques is to heat the silicon film, while avoiding direct heating of the substrate [9]. The resulting film has been thickened by simultaneous deposition of a-Si:H and epitactic crystallisation with repeated excimer laser pulses. The thicker film had a grain structure that was similar to the original layer [8]. Lateral epitaxial solidification involves a 700μs pulse from an Ar⁺ laser. The melt crystallises epitaxially after several hundred microseconds of exposure. Crystallisation begins
at the outer rim of the melt pool and the surface is corrugated with few defects [9, 8]. Lateral explosive crystallisation is done using both an Ar$^+$ and Nd:YAG laser. The aim is to reduce the thermal load on the substrate. A millisecond Ar$^+$ laser pulse is used to preheat the silicon to about 900°C [9] or 1000°C [8]. The silicon is then exposed to an 8ns frequency doubled Nd:YAG laser pulse and the melt exists for about 5ns. Both methods have resulted in crystal grains around 100μm long [9].

At the Institut für Physikalische Hochtechnologie, poly-Si has been formed on borosilicate glass using PECVD or IAD and crystallisation with an Ar$^+$ laser. Films were made by first depositing a-
Si by PECVD at 3Å/s or by ion assisted electron beam evaporation at 30Å/s at a substrate temperature of 200–400°C. The films were then scanned at 5cm/s with an Ar$^+$ laser. Layers were 1.3μm thick with a maximum grain length of 100μm and may be used for seed layers. Borosilicate glass and borosilicate glass coated with Mo have both been used as substrates and resulted in similar crystallisation [11].

Grains several tens of micrometers long and several micrometers wide have been obtained at the Universität Stuttgart, where the pulsed laser technique was used to crystallise 400nm thick layers of poly-Si deposited on glass [47].

Aluminium-induced crystallisation (AIC) has been used at UNSW to crystallise amorphous silicon layers deposited on glass [232]. The layers may be used as either a seed layer or base material of a cell. Layers are made by thermally evaporating Al to a thickness of 0.5μm and then depositing a 0.5μm layer of silicon by DC magnetron sputtering. Deposition rates are 5–100Å/s and 4Å/s for the Al and silicon, respectively [231]. AIC is done in a nitrogen gas ambient with the result that the aluminium and silicon layers interchange as the silicon crystallises, so that the structure is glass, poly-Si, Al+Si. At temperatures below 577°C, the silicon layer has a uniform thickness and forms separate crystals. Grains of 10–20μm in diameter were formed at a temperature of 480°C. At 500°C, it was possible to crystallise a 500nm thick layer in 30 minutes [232]. Lower AIC temperatures were found to result in larger grain sizes. The grain size and speed of crystallisation were also related to the average grain size of the Al [231].

The ‘gradient method’ of excimer laser crystallisation has been developed at the Tokyo Institute of Technology and grain sizes of ~ 5μm have been demonstrated on glass substrates [165]. The grains are produced using a single step process whereby the laser energy density is varied across the surface of the sample. A KrF laser and substrate temperatures of 500°C are used. Elongation of the grains is possible using repeated laser exposure and stepwise motion of the sample. The resultant grains are long, but only about 1μm wide [165].

Kyocera have developed the flux method for the deposition and crystallisation of seed-
ing layers onto glass. With this method, a glass substrate is first coated with a rear electrode and a 300nm layer of a-Si:H is deposited by plasma (P) CVD. A 200nm layer of Al is then deposited by electron beam evaporation and the sample is heated at 500–600°C to form poly-Si and a residual flux that may be removed with an acid etch. The seed films are mainly (111) oriented with crystal sizes in the order of microns. The film may be boron doped for use as a back surface field [235].

An average grain size of 2.3μm has been achieved on SiO₂ coated borosilicate glass in a cooperation between groups at the Max-Planck-Institut für Festkörperforschung, Universität Erlangen and Daimler Benz Forschungsinstitut. Solid phase crystallisation (SPC) (at 600°C) has been used to form poly-Si from LPCVD deposited a-Si [48]. The SPC film may be used as either an absorber layer or a crystalline seed for deposition of a thicker film to enhance light absorption. The average grain size was studied as a function of several parameters. It was found to increase as the deposition rate of the a-Si increased and to be strongly dependent on substrate type and weakly dependent on crystallisation temperature. The average grain size was independent of film thickness [48].

Smaller grain sizes of up to 1μm have been achieved on Corning 1737F aluminosilicate glass at UNSW, using DC magnetron sputtering techniques to form a-Si, and then SPC to form poly-Si [195]. Sputtering is done by bombarding a source in high vacuum (about 0.5–5 Pa) with gas ions that have been accelerated by a high voltage. Atoms from the source are ejected and move across the chamber to deposit on the substrate. The main drawback of sputtering is that deposition is line-of-sight. DC magnetron sputtering is advantageous in that it doesn’t use dangerous gases, there is good adhesion of a-Si onto the substrate, it is easily scalable, has high deposition rates and is simple and inexpensive [195]. The films made at UNSW were 100% crystalline [195]. Deposition temperature ranges of 25–600°C were used. At 25°C, the films peeled off before SPC and at 600°C there was a large crystalline volume fraction even before SPC. At deposition temperatures of less than 400°C, SPC was done at 610°C for 50–100 hours. No amorphous volume fraction was seen, but many defects. For deposition temperatures between 200–400°C, no difference in grain size after SPC was noticed. Lateral grain sizes were not limited by the film thickness.

The use of helium as opposed to hydrogen as a dilution gas in the PECVD of amorphous silicon and subsequent SPC of films deposited on SiO₂ has been studied at ENEA Centro Ricerche [2]. Helium and hydrogen resulted in grain sizes of 0.37μm and 0.56μm respectively. The time taken for crystallisation was found to increase with the hydrogen content of the a-Si:H [2].

Sharp Microelectronics Technology have used excimer laser annealing (ELA) to produce poly-Si from μc-Si deposited on Corning 1737 glass [324]. A potential for reduction
in the laser damage to the substrate was identified since the grain size of poly-Si films formed from $\mu$-Si layers was twice that of poly-Si films formed from a-Si layers at a given laser energy density. It was also found that using $\mu$-Si as a starting material led to an improved grain size uniformity. The maximum mean grain size achieved on a single sample was 149nm [324].

At the Chinese Academy of Science, pulsed rapid thermal processing (PRTP) has been used to form poly-Si from PECVD deposited a-Si on both Corning 7059 glass and fused quartz [363]. A mean grain size of more than 100nm, small lattice micro strain and a smooth surface have been achieved. PRTP consists of heating cycles; the sample is heated to 550°C for 60s over 10 cycles so that the film is said to be in a ‘critical state’. Rapid nucleation and grain growth are then triggered by a 1s thermal pulse at 850°C [363].

Double sided laser crystallisation of a-Si has been demonstrated by UNSW and Macquarie University using a copper vapour laser (CVL). A CVL has advantages of high power, higher pulse rates and better beam quality than an excimer laser. There is no need to heat the substrate and the relatively long wavelength allows crystallisation of thicker films. Crystallisation is done both directly above the sample and from below, through the glass substrate, which is mostly transparent to CVL wavelengths. The amorphous silicon layer is typically 0.5μm thick and deposited by PECVD onto a 1μm thick layer of SiO$_2$ on a glass substrate. The rear side, which is illuminated through the glass, receives approximately 50% of the intensity of the front side. Fully crystallised layers can be realised in 300ms [62].

At the Max Planck Institut für Festkörperforschung, crystallisation of a 410nm layer of a-Si has been demonstrated [315]. The a-Si layer was deposited at 450°C using LPCVD on SiO$_2$ coated borosilicate glass. An array of nucleation sites (with points separated by 10μm) were then crystallised using a cw Ar+- laser. This layer then underwent thermal annealing at less than 600°C which induced preferential crystallisation of the material in a radial region around the seeds [315].

Table 2.5 shows a summary of deposition on foreign substrates that required recrystallisation.

### 2.3.3 Silicon Substrates

The aim of low temperature deposition onto silicon substrates is usually to optimise deposition conditions and obtain some idea of the quality of material that can be expected before moving onto deposition on foreign substrates. Most groups who have investigated low temperature deposition of silicon onto silicon have also fabricated cells.

An efficiency of 14.7% and a $V_{oc}$ of 603mV has been reported by a collaboration
### Table 2.5: Summary of foreign substrates: Recrystallisation techniques. The results shown are grain sizes (gs) and grain lengths (gl). 

<table>
<thead>
<tr>
<th>Group</th>
<th>Substrate</th>
<th>Result</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CU</td>
<td>SiO$_2$ glass</td>
<td>200µm (gl)</td>
<td>[291]</td>
</tr>
<tr>
<td>IPH &amp; HMI</td>
<td>glass</td>
<td>100µm (gs)</td>
<td>[8, 9, 10]</td>
</tr>
<tr>
<td>IPH</td>
<td>borosilicate glass</td>
<td>100µm (gs)</td>
<td>[11]</td>
</tr>
<tr>
<td>US</td>
<td>glass</td>
<td>10'sµm x µm (gs)</td>
<td>[47]</td>
</tr>
<tr>
<td>UNSW</td>
<td>glass</td>
<td>10-20µm (gs)</td>
<td>[232]</td>
</tr>
<tr>
<td>Kyocera</td>
<td>glass</td>
<td>µm (gs)</td>
<td>[235]</td>
</tr>
<tr>
<td>MPIF, UE &amp; DBF</td>
<td>SiO$_2$ coated glass</td>
<td>2.3µm (gs)</td>
<td>[48]</td>
</tr>
<tr>
<td>UNSW</td>
<td>aluminosilicate glass</td>
<td>1µm (gs)</td>
<td>[195]</td>
</tr>
<tr>
<td>ENEA CR</td>
<td>SiO$_2$</td>
<td>0.56µm (gs)</td>
<td>[2]</td>
</tr>
<tr>
<td>Sharp</td>
<td>glass</td>
<td>149nm (gs)</td>
<td>[324]</td>
</tr>
<tr>
<td>CAS</td>
<td>glass &amp; fused quartz</td>
<td>1000Å(gs)</td>
<td>[363]</td>
</tr>
<tr>
<td>UNSW &amp; MU</td>
<td>glass</td>
<td>–</td>
<td>[62]</td>
</tr>
<tr>
<td>MPIF</td>
<td>glass</td>
<td>–</td>
<td>[315]</td>
</tr>
</tbody>
</table>

between the Hahn-Meitner Institut and Ferdinand-Braun Institut (HMI & FBI) [91]. PECVD at 450°C was used to deposit epitaxial layers 100–500nm thick for use as emitters in a 2x2cm$^2$ cell. A deposition rate of 4.2Å/s and phosphorous doping to 2x20$^{20}$/cm$^3$ have been achieved. The limiting factor was the poor electronic quality of the interface between the substrate and the layers [91].

At UNSW, a 14.4% efficient cell with a V$_{oc}$ of 627mV was achieved [364]. The deposited layer was processed into a cell, thinned to 25µm (most of which was the epitaxial layer), attached to glass using an adhesive and a double layer AR coating was added [364].

An efficiency of 13.7% and a V$_{oc}$ of 579mV was achieved using a 15µm p-type layer deposited on p$^+$ silicon at South Bank University. ECR PACVD and a deposition temperature of between 200–680°C were used [332]. The cell had hydrogen passivation and a SiN antireflection coating [332].

PCVD and a relatively low deposition temperature of 200°C were used by Tonen Corporation to achieve a cell efficiency of 11.4% and a V$_{oc}$ of 594mV. A 15µm film was deposited on n$^+$ silicon and a low temperature (all steps below 200°C) cell manufacturing process and a BSF were used. An 8.4% efficient cell was also made from a layer deposited on a plasma sprayed poly-Si substrate [118].

A µc-Si layer deposited as an emitter on a sc-Si substrate by ECRCVD has resulted in an efficiency of 11.2% at the HMI. Low temperature (340°C) and low deposition rates (0.8Å/s) were used. Cell performance was limited by layer quality [220].

Boron doped emitters deposited by ECRCVD onto n-type silicon by the HMI and CVD Products Inc, have resulted in cell efficiencies of 10–12%. The deposition temperature was 320°C and films were 150nm thick. The cells had an optimised thermal post-treatment
Deposition temperatures of 525°C have been used by a collaboration from Universität Stuttgart, ANTEC and Universität Erlangen to deposit layers by Ion Assisted Deposition (IAD) on sc-Si. A cell efficiency of 9.9% and maximum minority carrier diffusion lengths of 7–8μm were achieved. The cell had a thermal oxide ARC but no light trapping features and cell processing was done at high temperatures. Cells have also been made on mc-Si (SILSO material) at a deposition temperature of 600°C, and an efficiency of 3.9% was achieved [45]. A high deposition rate of 50Å/s was also demonstrated, and resulted in a minority carrier diffusion length of 4.5μm and a $V_{oc}$ of 600mV [45, 51, 239].

Canon have deposited μc-Si using plasma CVD and substrate temperatures of less than 350°C [266]. A deposition rate of 11Å/s resulted in grain sizes of 417μm and an efficiency of 8.7% (440mV) for a 2μm thick cell. Decreasing the deposition rate to 3Å/s resulted in an efficiency of 9.5%. The cell structure was p-i-n, the i-layer was deposited by HF PCVD, and the p and n-layers by RF PCVD [266].

Lower cell efficiencies have been achieved at the University of Utrecht using the HWCVD technique. A deposition temperature of 420°C and a deposition rate of 5.5Å/s were used to achieve a cell efficiency of 3.2%. The cell structure was n+ c-Si(0.01Ωcm)/i-poly-Si:H(1.5μm - HWCVD)/p-μc-Si:H/ITO and $J_{sc}$ was 18.2mA/cm² [252, 250].

A group from Toyota, Kawasaki and Chubu Electric Power Company achieved cell efficiencies of 2.3% (239mV) for nanocrystalline silicon deposited by Electron Beam Excited Plasma (EBEP) CVD at 420°C. Substrates were 1Ωcm p-type and the processing temperatures were high, at up to 1000°C, but the aim is to do in-situ layer doping. An advantage of EBEP CVD is that it does not use hydrogen [167].

Deposition of silicon onto silicon at low temperatures has also been achieved at Laboratoire de Physique des Interfaces et des Couches Minces, where both n and p-type μc-Si:H have been deposited on i-a-Si:H using the LBL technique and substrate temperatures of 150–190°C [140].

At the Tokyo Institute of Technology epitaxial films have been deposited by mercury sensitised photochemical CVD using a SiH₄/H₂ gas mix at substrate temperatures less than 200°C [241]. In photochemical CVD the chemical reaction is induced by UV radiation, generated by a lamp or laser.

The Solar Energy Research Centre in Western Australia and the Physics Division of Lucas Heights have reported the deposition of poly-Si onto silicon by sputtering and subsequent crystallisation with a solid phase sequence [265]. In this case, a-Si:H was first deposited to a thickness of 1.1μm. The last layer was deposited in a hydrogen-rich atmosphere so that the hydrogen concentration at the surface was higher than in the bulk.
Table 2.6: Summary of foreign substrates: Silicon substrates. The results shown here are efficiencies, $V_{oc}$ values, growth rates, grain sizes ($L_{diff}$), diffusion lengths ($L_{diff}$) and in one case, layer thickness.

Crystallisation then involved stepwise annealing at between 200 and 600°C with a cool to room temperature between each step. Grains sizes of more than 10μm were achieved. The aim is to use this layer as a seed layer for the growth of poly-Si [265].

A selective epitaxial growth by ECR plasma CVD has been investigated on sc-Si substrates at the Kanazawa University. Growth is selective due to simultaneous growth and etching with H$_2$ plasma. Usually, etching processes are unsuitable for selective growth at low temperatures, but a process that allows both deposition and etching at low temperatures has been developed [268]. Controlled etching is thought to allow rearrangement of the silicon atoms, effectively cleaning the surface. Selective epitaxial growth was obtained at 150°C but film thickness was limited to 40nm unless a thermal anneal and regrowth step was used. Selective film growth (no longer epitaxial) could be continued to a greater thickness. Epitaxial (non-selective) growth could also be obtained at 450°C [268].

Table 2.6 shows a summary of deposition on silicon substrates below the melting point of glass, where the intention is to switch to a foreign substrate.

2.4 Foreign Substrates: High Temperature Deposition

Deposition of silicon at high temperature on foreign substrates tends to result in larger grain sizes and higher growth rates. The increased surface mobility of adsorbed atoms at high process temperatures increases the nucleation and growth rate on foreign substrates [61]. At low deposition temperatures, atoms have reduced mobility on the sub-
strate. This promotes continuous nucleation of new crystal growth sites and hence smaller grain sizes.

High temperatures limit the choice of substrates. Requirements for a substrate for high temperature deposition of silicon include a thermal expansion coefficient similar to silicon, stability at high temperatures, low levels of mobile impurities (unless a diffusion barrier is used) and low cost. For some deposition techniques such as RTCVD, the substrate will also need to withstand fast heating and cooling cycles and high temperature gradients.

2.4.1 Examples of the High Temperature Approach

Substrates Without Diffusion Barriers

Alumina has been widely investigated as a substrate because it can be cheaply produced. Laboratoire PHASE have achieved grain sizes of about 10μm by RTCVD [14, 290] and LPE with a RTCVD seeding layer [65]. Alumina reflects about 85% of incident light and therefore makes a good back surface reflector. This means it can be difficult to deposit on alumina when using a lamp heating source such as that used for RTCVD. For this reason, 0.2μm of silicon was first evaporated to absorb the light from the lamps. Lifetimes of 0.3μs and diffusion lengths of 10μm were obtained for layer thicknesses of 11μm. Grain sizes of 5–10μm on alumina were achieved by RTCVD at IMEC [33, 34]. Effective lifetimes were 0.5μs after remote plasma hydrogenation at 400°C for grain boundary passivation. A grain size of 10μm and a diffusion length of 8μm were achieved on layers deposited by CVD on alumina substrates at Technische Universität Berlin [233].

Zone-defined growth, a new solution growth technique, has been demonstrated on alumina substrates at the University of Tokyo [184]. The technique involves a metal sheet and the zone-melting of silicon powder. Continuous, mainly (100) oriented films have been achieved using aluminium as the solvent metal. At present, scanning speeds are very slow (1μm/s).

The thermal expansion coefficient of alumina is approximately twice that of silicon between room temperature and 1100°C and this can cause stress in silicon layers grown on alumina [371]. Mullite substrates (aluminosilicates) have the advantage that the thermal expansion coefficient can be matched to that of silicon, but high-purity mullite is not yet commercially available. Silicon layers with grain sizes of 10–15μm have been deposited by RTCVD at Laboratoire PHASE on laboratory fabricated, 99.9% purity mullite substrates with no buffer layer [13]. The layers had an effective lifetime of 0.5μs. Low purity (90%), commercially available mullite substrates produced layers with voids. LPE has been used to grow layers on mullite substrates with a seeding layer deposited by RTCVD
but continuous layers have not been achieved [113].

Alumina and mullite are insulating and will probably require cell designs with both contacts on the front. Graphite and glassy carbon are conducting substrates that are compatible with conventional cell designs and which have similar thermal expansion coefficients to silicon. Continuous layers over 4cm² have been grown by LPE on glassy carbon with a seed layer formed by inductively coupled RF plasma decomposition in a collaboration between Max-Planck-Institut für Festkörperforschung, Max-Planck-Institut für Metallforschung and LSG Inc [133]. A two step process was used for growing the seed layer. The first layer was nanocrystalline with good adhesion to the substrate and the second layer was microcrystalline with a crystal size large enough (> 1µm) to be a good seeding layer for LPE. A low defect density was found in the LPE layer and there were no holes or inclusions between the seed layer and the LPE layer. The grain size was approximately 10µm. The active layer was grown 10µm thick and a 1.5µm thick emitter was grown to avoid short circuits caused by a rapid diffusion of dopants along grain boundaries.

Max-Planck-Institut für Festkörperforschung, Siemens and Technische Universität Hamburg have investigated a three step process to deposit silicon on graphite [242]. The process consists of deposition of 3–5µm of α-Si on graphite by sputtering or PECVD, ZMR by line electron beam in high vacuum, and thickening of the silicon layer by epitaxial CVD to 20–40µm. It was found that a capping layer of SiO₂ was not necessary during the ZMR. The epitaxial layer showed a columnar grain structure originating from the seed layer with grain sizes of 100µm by several millimetres after recrystallisation. A higher scan velocity (28mm/s) resulted in a predominantly (110)-texture, while a lower scan velocity (4mm/s) led to a more random distribution of crystal orientations. High scan velocities are possible with a line electron beam because of the high power available but the necessity for high vacuum with a line electron beam is a significant disadvantage.

A plasma spraying technique has been investigated by several groups. This involves heating silicon powder in a high temperature plasma and depositing it on heated substrates. Growth rates of up to 10µm/s and a cell efficiency of 4.3% and a $V_{oc}$ of 426mV have been achieved at Tokyo Institute of Technology [306]. Atmospheric plasma spraying (APS) of silicon on SiAlON-Si substrates can improve nucleation and provide a diffusion barrier for silicon subsequently deposited by LPE or CVD. SiAlON has a higher thermal shock resistance than mullite, which is important for APS and CVD. LPE on substrates of silicon-enriched SiAlON (Si/SiAlON) with and without a plasma-sprayed Si seeding layer, and free-standing plasma-sprayed silicon have been investigated at ECN [272]. Closed layers of 1cm² on plasma-sprayed silicon (as a seeding layer on Si/SiAlON and free-standing)
have been achieved with grain sizes of 10–100\,\mu m. A melt of In/1\%Al was used; a pure indium melt did not result in closed layers. Plasma-sprayed silicon as a seeding layer has also been recrystallised with ZMR to reduce the porosity and increase grain size in a collaboration between ECN and Technical University Delft [177, 178].

High-temperature glasses are another option as substrates. Transparent glass-ceramics resistant to temperatures up to 950\,\degree C and with a coefficient of thermal expansion matched to silicon have recently been developed [234]. They are suitable for fabrication of thin silicon solar cells if out-diffusion of glass components from the substrate is suppressed with a PECVD SiO$_2$/SiN$_x$ barrier.

LPE has been used to grow continuous layers of 10\,cm$^2$ with a Sn/Al melt using a seeding layer of a-Si on borosilicate glass at 750\,\degree C at the University of NSW [283]. Grain sizes of 30\,\mu m with a (111) preferential orientation were achieved with a layer thickness of 30\,\mu m. The same group also grew continuous films on unseeded glass substrates at around 750\,\degree C with an average grain size of 100\,\mu m [281].

At the Laboratoire d’Analyse et d’Architectures des Systèmes du Centre National de la Recherche Scientifique and ENSIGC, layers of poly-Si of about 0.6\,\mu m thickness were deposited on SiO$_2$ using LPCVD. Deposition was done at temperatures of 600\,\degree C or 660\,\degree C and the dopant concentration and resistivity were uniform over the surface [193]. The minority carrier lifetime was very low; 40\,ns [194].

Silicon has been deposited on high-temperature glass by a group at Max-Planck-Institut für Festkörperforschung and Universität Erlangen [42, 43]. First, a thin a-Si layer was deposited on the glass substrate by LPCVD. This was followed by solid phase crystallisation for 10–12 hours at around 600\,\degree C to form the seeding layer with a grain size of 1–2\,\mu m. APCVD was then used to deposit an active layer several microns thick with a growth rate of 1\,\mu m/min at temperatures up to 1000\,\degree C. Columnar grains were formed with a preferential (110) orientation. Smoother layers were formed with seeded growth than with direct deposition. An average grain size of about 2\,\mu m and a minority carrier diffusion length of 2\,\mu m were measured (compared with a minority carrier diffusion length of 0.6\,\mu m for unseeded growth [69]). The dislocation density was high; 10$^9$/\,cm$^2$. Modelling showed that if a pyramidally-structured glass substrate was used, then the layers had an efficiency potential of 12–15\%. A simple cell structure was fabricated on the layers in a collaboration between the above two institutions and Universität Stuttgart [68]. The glass substrate under most of the cell area was removed by etching in concentrated HF and a rear metal contact was evaporated. A 2\% efficiency with a $V_{oc}$ of 340\,mV was achieved after hot-wire hydrogen passivation. Hydrogen passivation reduced grain boundary recombination velocity to less than 10$^4$/\,cm/s but $V_{oc}$ was limited by recombination in the
space charge region at grain boundaries.

Zone melt recrystallisation (ZMR) of silicon on high temperature glass has been investigated in a collaboration between Max-Planck-Institut für Festkörperforschung, Fraunhofer ISE, Max-Planck-Institut für Metallforschung and Universität Stuttgart [46]. A silicon layer 10–30μm thick was deposited by ion-assisted deposition, followed by a SiO₂ capping layer. After recrystallisation with a scanning speed of 30mm/min grain sizes were in the range 50–200μm, but up to 300μm by 2mm. Films were heavily doped and may be suitable as seeding layers for epitaxial growth of an active layer.

Substrates with Diffusion Barriers

Contamination of the active silicon layer by a low cost substrate may occur during high temperature processing. This can be reduced by using a diffusion barrier layer. Other desirable features of a diffusion barrier are good nucleation and wetting, optical confinement and back-passivation of the active silicon layer. The diffusion layer must be chemically and mechanically stable at high temperatures.

Astropower has taken the diffusion barrier approach furthest. They use a continuous sheet solution growth process to grow thin silicon layers on high-temperature substrates. Steel, ceramics and graphite cloth have been investigated as substrates but the nature of the preferred substrate has not been disclosed. Initially, contamination meant that the effective diffusion length was less than 10μm. A metallurgical barrier is now used to prevent contamination and provide good nucleation and wetting. The as-grown layer has a grain size of 1–5 mm and diffusion length of 25–40μm. To improve the material quality after growth, phosphorus and aluminium gettering are performed together for 4 hours. The diffused and alloyed regions are then etched away to prevent re-contamination of the bulk. The bulk is passivated using RF hydrogen plasma. Surface passivation is achieved with low-temperature PECVD oxide as high temperature oxidation tends to depassivate hydrogenated materials. Effective minority carrier diffusion lengths can be over 150μm after the gettering and passivation steps. The highest efficiency achieved to date is 16.6% (608mV) on a 1cm² cell [23]. The highest efficiency that has been achieved on a low-cost substrate is 12.5% (566mV) for a thin (60–100 microns), 0.5cm² cell [117]. A short circuit current of 25.8mA/cm² was achieved for a cell of 20μm thickness [30]. Sheet presently in production is 15cm wide [29]. A new machine has demonstrated that sheet can be made 30cm wide. An efficiency of 11.6% (582mV) was achieved on a cell of area 676cm².

Astropower are pursuing both conducting substrates with a conventional cell design and insulating substrates with both contacts on the front and monolithic integration of the cells. One option is to use isolation cuts in the silicon layer with insulators along one
side of the cut to avoid shunts [117]. A 36 segment monolithically interconnected device of 320cm$^2$ had an efficiency of 9.8%. A 6 segment device has also been reported with a $V_{oc}$ of 3.33V [287].

Multiple diffusion barrier layers can also be used to reduce the requirements on each layer (such as preventing diffusion and providing good nucleation and wetting). Promising results have been achieved at Fraunhofer ISE using SiO$_2$ and SiNx as diffusion barriers. A seeding and BSF layer 20–50μm thick was deposited by LPCVD on SiSiC with a buffer layer of SiO$_2$/SiNx/SiO$_2$ (ONO) as shown in figure 2.2 [147, 255]. The seeding layer was recrystallized by ZMR at 10mm/min, which resulted in a grain size several millimetres by several centimetres and a dislocation density of $10^6$cm$^{-2}$. An active layer 30–90μm thick was deposited by RTCVD at a growth rate of 5μm/min. A dry solar cell process produced a 9.3% efficient cell of 1cm$^2$ with a $V_{oc}$ of 567mV and an average diffusion length of 15μm. The same process on a SiAlON substrate (with an ONO barrier) led to a cell efficiency of 5.5% [256].

A similar deposition process was followed to produce cells on graphite with a SiC interlayer and a cell efficiency of 11% (570mV) [199]. The diffusion length for this cell was 30μm and the active layer thickness was 15μm. Graphite substrates that were fully encapsulated by SiC and ONO (and therefore insulating) were used to produce 10.8% efficient cells. For all the above results a dry solar cell process was used. In the dry solar cell process, cleaning, phosphorous glass etching and cutting for cell isolation are performed by reactive ion etching (RIE). Dry processing is needed because of the porosity of the graphite substrates. It is possible to encapsulate the substrate with a chemically tight cover instead but this increases costs. The fact that the 11% cell efficiency was not improved upon by the encapsulation of the substrate with ONO indicates that SiC on its own is an equally good diffusion barrier.
A ‘surface modification film’ is being used by Daido Hoxan to improve nucleation and wettability. A continuous layer of silicon has been grown by LPE on graphite using this approach [210]. The temperature difference method was used, which involves heating the source wafer more than the substrate to create a concentration gradient in the melt. The growth rate was 1–8μm/min and the grain size was 0.1–3 mm. A very high defect density was found near the graphite-silicon interface, possibly due to the difference in thermal expansion coefficients. Layers 50×50mm² with a diffusion length of 30μm were deposited [166].

A buffer layer of SiNx/SiOx has been used at the Electrotechnical Laboratory to grow silicon layers on alumina ceramics by electron cyclotron resonance plasma CVD (ECR-PCVD) and electron beam recrystallisation [303]. It was found that SiNx increases wettability and reduces agglomeration of silicon and SiOx acts as a diffusion barrier. Deposition was done at 500°C and recrystallisation at 850°C. The active layer thickness was about 5μm and the growth rate was about 5μm/hr. Grain size was 10μm by 200μm. This group also achieved a cell efficiency of 6.5% (480mV) for a 4.2μm thick cell produced by CVD on alumina coated with SiO2 and Si3N4, followed by laser recrystallisation at 400–500°C [284]. The cell process included hydrogen-plasma passivation and a double layer antireflection coating. The reflectivity of the substrate contributed to a relatively high current density of 25.5mA/cm² but the efficiency was limited by low Voc and fill factor.

Laboratoire PHASE, IMEC and Fraunhofer ISE have collaborated to investigate RTCVD on graphite using a barrier layer of SiO2 [216]. Grain sizes of 0.1–6μm and diffusion lengths of 3μm were achieved for a layer thickness of 15μm. ZMR was applied after the RTCVD to give an average grain size of 2.5μm by 1.6mm and a defect density of 10⁶cm⁻³.

SiC has been used at ASE GmbH as an intermediate layer to seal porous graphite substrates [82]. A seed layer was then deposited on the SiC by CVD and recrystallised by ZMR. A highly doped seed layer was required to form a back surface field to reduce the effect of high recombination at the SiC contact. The grain size was about 100μm with a minority carrier diffusion length of 10–15μm.

Solution growth, using a sputtered silicon source, has been used to deposit silicon on temperature resistant glass at 650–750°C [350]. An initial layer of AlN was deposited on the substrate to improve wetting. Continuous, preferentially (111) orientated layers with a grain size of about 5μm were obtained. The layers were doped to a level corresponding to the solid solubility of aluminium (10³⁵cm⁻³) so cannot be used for the active layer of a cell but could be used as a back surface field (BSF) or seeding layer.

An alternative option to improve the growth of silicon on foreign substrates is to mod-
ify the substrates. Annealing for 210 hrs increased the maximum grain size of alumina substrates from 7 to 60 microns [103]. Since silicon tends to nucleate at the grain boundaries of the alumina this will increase the grain size of the silicon. Thermal etching of the grain boundaries of the alumina was found to improve growth by providing nucleation sites for the silicon [274].

An interesting method of creating a back surface field has been demonstrated recently at Technische Universität Hamburg. Thin seeding layers were deposited on graphite by LPCVD and recrystallised by ZMR using an electron beam [192]. Doping of the seeding layer was achieved by immersing the graphite substrate in an aqueous dopant solution prior to silicon deposition and baking it to remove excess solvent. The dopants were driven in by diffusion during recrystallisation. The grain size after LPCVD was about 50nm and after recrystallisation was 100μm by a few cm. Some SiC was found on the surface of the recrystallised silicon. This will need to be removed, for example by ion beam etching, prior to epitaxial growth of the active layer. Out-diffusion of impurities from the graphite substrate caused unintentional doping with a level of 10^{15}–10^{17}cm^{-3} varying across the sample area that was compensated by the immersion doping technique.

Table 2.7 shows a summary of deposition on foreign substrates above the melting point of commercially available glass.

### 2.5 Ribbon Growth

Ribbon growth is a promising option for thin-film silicon solar cells. Layers as thin as 5μm [327, 328] have been grown and cell efficiencies as high as 15.1% on 100μm multicrystalline layers [170] and 17.3% on single crystal layers demonstrated [230]. A large benefit of ribbon grown silicon is that commercial viability has already been demonstrated [170, 174]. Ribbon growth has been included in this study because ribbon grown silicon does not require slicing. Although some of the ribbon growers are still producing thick layers, thinner layers are clearly a more economical option and research is moving in this direction.

#### 2.5.1 Growth Techniques

Ribbon growth involves pulling a sheet of silicon from a molten stockpile. Solidification occurs at the meniscus and the meniscus geometry and pull rate determine both the rate and direction of cooling and the subsequent grain morphology [203]. Also included in this section are Silicon Sheets from Powder (SSP) whereby powdered silicon is irradiated to form sheets.

Ribbon growth can be divided into 2 broad categories; vertical growth and horizontal
<table>
<thead>
<tr>
<th>Institution</th>
<th>Substrate</th>
<th>Grain Size (μm)</th>
<th>Electrical</th>
<th>Refs</th>
</tr>
</thead>
<tbody>
<tr>
<td>PHASE, ECN &amp; CNRS-LMPM</td>
<td>Alumina</td>
<td>10</td>
<td>( \tau = 0.3\mu s, )</td>
<td>[14, 290]</td>
</tr>
<tr>
<td>PHASE, LPM &amp; GEMPPM</td>
<td>Alumina</td>
<td>10</td>
<td>( L = 10\mu m )</td>
<td>[65]</td>
</tr>
<tr>
<td>IMEC &amp; PHASE</td>
<td>Alumina</td>
<td>5–10</td>
<td>( \tau = 0.5\mu s )</td>
<td>[33, 34]</td>
</tr>
<tr>
<td>ETL</td>
<td>Alumina</td>
<td>10×200</td>
<td>( \eta = 6.5% )</td>
<td>[284]</td>
</tr>
<tr>
<td>ETL</td>
<td>Alumina</td>
<td>–</td>
<td>( L = 8\mu m )</td>
<td>[233]</td>
</tr>
<tr>
<td>TU-Berlin</td>
<td>Alumina</td>
<td>10</td>
<td>( \tau = 0.5\mu s )</td>
<td>[13]</td>
</tr>
<tr>
<td>PHASE &amp; IMEC</td>
<td>Mullite</td>
<td>10–15</td>
<td>( \eta = 11.0% )</td>
<td>[199]</td>
</tr>
<tr>
<td>MPI-F, MPI-M &amp; LSG &amp; TU-Hamburg</td>
<td>Glassy carbon</td>
<td>10</td>
<td>( L = 30\mu m, )</td>
<td>[210, 166]</td>
</tr>
<tr>
<td>Fraunhofer ISE</td>
<td>Graphite</td>
<td>mm×cm</td>
<td>( \eta = 11.0% )</td>
<td></td>
</tr>
<tr>
<td>Daido Hoxan</td>
<td>Graphite</td>
<td>100–300</td>
<td>( L = 30\mu m )</td>
<td></td>
</tr>
<tr>
<td>PHASE, IMEC &amp; Fraunhofer ASE GmbH</td>
<td>Graphite</td>
<td>0.1–6</td>
<td>( L = 3\mu m )</td>
<td>[216]</td>
</tr>
<tr>
<td>TU-Hamburg</td>
<td>Graphite</td>
<td>100</td>
<td>( \tau = 10–15\mu m )</td>
<td>[82]</td>
</tr>
<tr>
<td>ECN</td>
<td>Si/SiAlON</td>
<td>10–100</td>
<td>–</td>
<td>[192]</td>
</tr>
<tr>
<td>UNSW</td>
<td>High-temp glass</td>
<td>50</td>
<td>–</td>
<td>[283]</td>
</tr>
<tr>
<td>UNSW &amp; U Stuttgart</td>
<td>High-temp glass</td>
<td>100</td>
<td>–</td>
<td>[281]</td>
</tr>
<tr>
<td>MPI-F, U Erlangen &amp; U Stuttgart</td>
<td>High-temp glass</td>
<td>2</td>
<td>( L = 2\mu m, )</td>
<td>[43, 68]</td>
</tr>
<tr>
<td>NTT</td>
<td>High-temp glass</td>
<td>5</td>
<td>( \eta = 2% )</td>
<td>[350]</td>
</tr>
<tr>
<td>Telecommunication Energy Labs</td>
<td>Not disclosed</td>
<td>1000–5000</td>
<td>( \eta = 16.6% )</td>
<td>[23]</td>
</tr>
<tr>
<td>Astropower</td>
<td>SiSiC</td>
<td>mm×cm</td>
<td>( L = 15\mu m, )</td>
<td>[147]</td>
</tr>
</tbody>
</table>

Table 2.7: Summary: high temperature deposition on foreign substrates.
growth. Vertical growth is much slower than horizontal growth. For vertical growth, crystallisation rates are typically cm/min, leading to production rates in the range 10–160cm²/min [186]. Examples of vertical growth techniques are dendritic web, edge-defined film-fed growth (EFG), string ribbon (see figure 2.3) and silicon sheet from powder (SSP). Kardauskas [174] claims that vertical growth has an inherent crystallisation rate limitation to 1–2cm/min due to the thermoelastic stress that produces both an increase in dislocation density and buckling. Vertical growth can be further classified into growth where the meniscus is short (in the order of the ribbon thickness) as in the case of EFG, and free rising meniscus (whereby the molten silicon has very little contact with the shaping element) as in dendritic web and string ribbon growth [203]. Slow growth produces substantially higher quality silicon than fast growth, but this must be balanced against the higher production costs.

During horizontal growth, the solidification front is almost in the same plane as the ribbon surface and production rates of m²/min may be achieved [186]. Fast growth has a large solid/liquid interface area that enables the latent heat of fusion to be more readily removed, therefore leading to higher growth rates [203]. Grain growth is parallel to the surface. Figure 2.4 shows a schematic of horizontal growth.

There are several groups that have had some success both in growing ribbon layers and in cell fabrication on ribbon grown silicon. An outline of the techniques used by some
groups and the current status of ribbon and cell development is given below.

2.5.2 Ribbon Grown on Substrate - Bayer

Bayer fabricate the ribbon grown on substrate (RGS) material, which involves growth of molten silicon on a supporting substrate. Growth is fast, with a production rate of one $10 \times 10 \text{cm}^2$ wafer/s [135]. Drawbacks are that material usage is high, layers are 300$\mu$m thick and the uneven front surface and carbon rich rear surface must be removed. This results in the removal of about 50$\mu$m of silicon from the front surface and 25$\mu$m from the rear.

Typical characteristics include a thickness of 300–400$\mu$m, a grain diameter of 0.1–0.5mm, a dislocation density of $10^5$–$10^7$/cm$^2$, a carbon concentration of $1$–$2 \times 10^{18}$/cm$^3$ and an oxygen concentration of $2 \times 10^{18}$/cm$^3$ [186]. Three different groups have made solar cells on this material. A comment relevant to all groups is that although the $J_{sc}$ value was reasonable, $V_{oc}$ was low. The results, as reported by Bayer [186] were: an efficiency of 11.1% and $V_{oc}$ of 538mV by the University of Konstanz using slow cooled RGS, their V-grooving technique and hydrogen passivation, 10.1% by Fraunhofer ISE using rapidly cooled RGS and pre-gettering and 9.8% by ISFH, Emmerthal using slowly cooled RGS and standard Metal-Insulator-Semiconductor (MIS) processing.

Subsequent work at the University of Konstanz resulted in a cell efficiency of 12.5% (560mV) for a $2 \times 2 \text{cm}^2$ cell. Mechanical V-texturing was done with the aim of reducing the reflectivity and thereby increasing the $J_{sc}$. Additional benefits of this texturing are that, since light enters at an angle, charge carriers are generated closer to the surface and hence the collection probability increases. The efficiency improvement of these cells can be attributed in part to a Microwave Induced Remote Hydrogen Plasma (MIRHP) step used to passivate crystal defects [137]. The MIRHP step involves in-diffusion of atomic hydrogen and greater efficiency has been achieved with long passivation times at low temperature. There is the possibility of high temperature, short term passivation if it

![Figure 2.4: Horizontal ribbon growth, after Green [129].](image-url)
is done earlier in the process (before metallisation) [136]. The optimum temperature and
time were found to be related to the concentration of interstitial oxygen, which acts as an
inhibitor for the atomic hydrogen. MIRHP was found to increase the efficiency by 1.1%
absolute [136].

Peters et al. have shown that rapid thermal processing (RTP) has advantages over
conventional quartz tube furnace processing on RGS material. This is because the inter-
stitial oxygen remains dissolved during an RTP process. Eight cells were prepared and
diffusions done by either RTP or in a conventional quartz furnace. The highest efficiency
for the conventional furnace was 12.4% (546mV) whereas the RTP process resulted in a
cell efficiency of 13.6% (558mV) [245]

2.5.3 Dendritic Web Growth - GIT and EBARA Solar

Dendritic web growth is achieved by pulling dendrites of silicon from a solution of molten
silicon that becomes trapped between the dendrites and solidifies. The dendrites can be
removed and recycled. The result is usually a bi-crystalline ribbon with twin boundaries
at the centre where two mono crystals meet. The mono crystals are a result of single
crystal growth from each edge of the solidifying meniscus. Grain growth is parallel to the
surface [203]. Dendritic web growth is typified by low production rate, but high quality
material [129].

Both the Georgia Institute of Technology (GIT) and EBARA Solar are involved in the
production of dendritic web ribbons. Present production material from EBARA Solar is
100μm thick and 6cm wide, making cells of 10cm². A continual feeding process allows the
growth of crystals of up to 37m in length [205]. A recent change has been from induction
heating to resistance heating. This has removed moving parts from the heating process,
made the delivery of heat more flexible and increased the reproducibility [205].

In a collaboration between EBARA Solar and GIT, a single crystal silicon cell with
an efficiency of 17.3% and a \( V_{oc} \) of 618mV was demonstrated with a sophisticated cell
processing sequence. The cell area was 4cm², and the material was 100μm thick [230].
This cell had a relatively high \( V_{oc} \) compared to other cells made on ribbon material.
This was due to the high bulk lifetime and steps taken during cell processing to achieve
a low surface recombination [230]. A high throughput RTP process was used to enable
simultaneous diffusion of a light boron emitter and deep phosphorous back surface field
(BSF). The cell had a \( S_{eff} \) of 20cm/s and a bulk lifetime of 150μs. The modelling program
PC1D was used to show that the BSF resulted in a 4% increase in absolute efficiency
compared to cells with infinite \( S_{eff} \) [230].

A new cell structure used on the 100μm thick ribbon resulted in an efficiency of 14.4%
Ribb on Gro wth

(Voc of 606mV) on a 4cm² cell. A pn-junction was formed by alloying aluminium and n-type silicon. The junction was located at the rear of the cell and does not shunt. Contacts were screen printed [206].

EBARA Solar and GIT have developed bifacial cells that have demonstrated almost equal rear and front surface efficiencies. An interdigitated back contact (IBC) cell has also been proposed. A precursor to this cell with front and rear contacts was made to check the use of an aluminium alloy pn-junction as a back junction. It was 4cm² and demonstrated an efficiency of 13.2% and a Voc of 599mV [205].

2.5.4 String Ribbon - Evergreen Solar

String Ribbon is a growth technique used by Evergreen Solar. In the past it has also been called edge supported ribbon and edge stabilised ribbon. A non-conductive string is used to stabilise the edges of the ribbon and this remains in the material during cell fabrication [330]. Ribbon thickness is a function of melt temperature, ribbon thermal environment and pull speed. The main advantage of this method is a high tolerance of temperature variations; up to ±5°C due to the high meniscus and edge stabilisation. A simple method of continuous melt replenishment has been developed and ribbon can be cut ‘on the fly’ [170]. Over time, segregation of impurities has been found to occur naturally in the melt, leading to the possibility of using poorer quality material and/or necessitating periodic dumping of the melt.

Evergreen Solar have a manufacturing plant in operation 24 hours/day, 7 days/week that is using the string ribbon technique to produce material for commercial use in 30 or 60 W modules [170]. The commercially produced ribbon is 300μm thick, 5.6cm wide and p-type with a resistivity of 1Ωcm [170]. Final cells are 15cm long, therefore having an area of 84cm² [330].

The issue of thermal stress has been addressed by both an active, tunable afterheater and a passive afterheater [327]. An active afterheater allowed growth rates of up to 25mm/min and a passive afterheater, 18mm/min (to produce 84cm² sheets [327]). The overall stress level was best lowered by having the largest cooling rate in regions of high temperature [328]. Evergreen Solar have been active in pursuing thin ribbon and have grown ribbons with thicknesses as low as 5μm [327, 328].

A 15.2% (581mV) cell has been demonstrated at Paul Scherrer Institut (PSI) using 200μm thick string ribbon. A RF plasma hydrogen passivation step and phosphorous and aluminium cogettering were used and as a result the minority carrier diffusion length increased by a factor of two [104].

In conjunction with Sandia National Laboratories and the University of New Mexico a
14.5% efficient cell with a $V_{oc}$ of 600mV on 300μm thick ribbon was demonstrated [263]. PECVD silicon nitride was used to provide surface passivation and an anti-reflection coating (ARC). H₂ and NH₃ plasma pretreatments have also been used both with and without a protective nitride layer. This resulted in lower efficiencies than the direct deposition method.

Evergreen Solar have also worked in conjunction with GIT to increase the lifetime of the string ribbon material. An increase of the as-grown value of 1μs to 9μs after cell fabrication was achieved [359]. This is thought to be due to hydrogen passivation of defects and impurity gettering. Cell fabrication included a forming gas anneal (FGA) and phosphorous and aluminium gettering. The FGA resulted in an average increase in efficiency of 1.2%. The average cell results were a $V_{oc}$ of 580mV and an efficiency of 14.6%. The best cell had an efficiency of 15.4% and a $V_{oc}$ of 589mV. A 100μm thick cell that was fully screen printed and had a beltline diffused emitter (BLP) had an efficiency of 10.9% and a $V_{oc}$ of 568mV. SiN was applied by PECVD as an ARC and for front surface passivation. Further improvements are expected since the screen printing process possibly degraded the SiN and because there was poor back surface passivation [359].

Cell manufacturing in conjunction with the University of Konstanz (UKN) recently raised the efficiency of standard production string ribbon material. The most important change was an increase in the sheet resistivity of the emitter diffusion. There is room for a further increase, which is hoped to result in even greater efficiency improvements. The highest efficiency for cells processed at UKN was 14.3% (average $V_{oc}$ was 596mV) for a 8×10cm² cell. Using the same recipe, the highest efficiency for cells processed at Evergreen Solar was 13.9% for a 8×15cm² cell. The strings have been found to cause shunting that has limited performance. Cells were successfully isolated from the strings, and there was an efficiency increase per area of solar cell, but not per area of ribbon produced [138].

### 2.5.5 Edge-Defined Film-Fed Growth - ASE Americas

ASE Americas use the Edge-defined Film-fed Growth (EFG) technique to produce commercial quantities of string ribbon. EFG growth involves the movement of molten silicon up the interior of a graphite die by capillary action, after which it can be mechanically pulled [203]. Although the die provides edge stabilisation, it can also introduce impurities or react with the silicon to form silicon carbide precipitates. As the die dissolves, the width and thickness of the ribbon will increase [203]. Generally, EFG has few grain boundaries but it is known to contain many dislocations, twin arrays, point defects and saturated carbon levels [171]. Kardauskas found the twin arrays to be of high density but mostly electrically inactive [174]. There is an inhomogeneous distribution of dislocations
Ribbon Growth

(often more than $10^6$/cm$^3$) and some regions have low diffusion lengths, which processing methods must take into consideration. Material tends to be of (110) orientation [171]. At ASE Americas, work has been done to increase yield and productivity by introducing continuous melt replenishment, using a shallow crucible with low melt volume and a short die and increasing the operation life of the die crucible.

ASE Americas produce 5m long, hollow, 8 sided tubes, each face being 10cm wide and 300μm thick. Routine production of cells with efficiencies of around 14% was demonstrated [174]. The tubes are cut with lasers to form wafers 10×10cm. The transfer from octagon to wafer results in a total material loss of around 8%. Less than 5% of the material must be cleaned away before a cell can be made [174]. For more than 50 tubes 150–200kg of silicon goes through a single crucible and the residual silicon loss is about 500g [171]. Therefore, for the whole procedure, less than 13% of the input silicon is lost.

ASE Americas have grown cylinders with a thickness of 75–100μm. The as grown value of $L_{\text{diff}}$ was 30–50μm and some grains sizes were 100μm. Iron was gettered by aluminium alloying [171]. The advantages of cylindrical growth are; faster pulling rates (by a factor of two), better electronic properties, reduction of thermoelastic stress due to the symmetry and the fact that rotation can be used to achieve a more uniform thickness. Future plans for the company include a 20MW production facility [171].

2.5.6 Silicon Sheets from Powder - IMEC, KU Leuven and Fraunhofer ISE

A cooperation between groups at IMEC, KU Leuven and Fraunhofer ISE have grown silicon sheets from powder (SSP) using a compacted silicon powder on a substrate. The powder is heated from one side only with a halogen heat source. Some of the silicon powder (granular, of 0.15–1.5mm diameter) melts and ‘percolates’ into the underlying powder, combining with particles to form a self-supporting pre-ribbon. A zone melt recrystallisation (ZMR) process is then used to increase the grain size of this ribbon [107]. ZMR is typically done from both above and below the ribbon. Another alternative is to melt only from above. This simplifies the process, but grain sizes and growth rates are limited. Advantages of the SSP technique are that it is simple and that liquid silicon is not in contact with any sources of possible contamination [108]. Sheets are 350μm thick and 80×150mm$^2$. Grains are typically several cm long and several mm wide and (221) orientation is favoured. At Fraunhofer ISE, a cell of 13.1% (563mV) efficiency with a double layer ARC was made on these ribbons [108]. Recently, microwave remote plasma hydrogenation has been used on pre-ribbon substrates, for which the grain size is between 10–50μm, with the aim of fabricating cells on pre-ribbon. This has enabled increases in
Voc from 370mV to 500mV [107]. An additional Al BSF step further increased the Voc value to 530mV, and the cell efficiency to 6.5% [107]. A disadvantage of the SSP technique is that the ribbon is very thick, which means that lower quality silicon will probably be needed to reach a low cell cost.

2.5.7 Silicon Sheets from Powder - University of Konstanz

Ribbons from powder on a stabilising substrate have been developed at the University of Konstanz. A resistively heated, movable graphite strip heater is used to irradiate the powder. The resulting poly-Si films have grain sizes in the order of several mm, are 20–800 μm thick and are made from an original particle size of 0.3–125 μm [238]. Minority carrier diffusion lengths of up to 20 μm have been achieved. In contrast with the material produced at the Fraunhofer Institute, only a single irradiation is required. A disadvantage is that there are severe restrictions placed on substrate choice for thin ribbons relating to purity, wetting and separability.

Several different substrates have been used: quartz, quartz coated with Si₃N₄, graphite, graphite coated with SiC, graphite coated with PyroC, amorphous Carbon, pyroC, AlN, BN and BN coated with PyroC. A self-supporting silicon sheet has been achieved after separation from both quartz and pyrolytic graphite substrates. The pyrolytic graphite substrates resulted in p-type silicon with a diffusion length of about 20 μm. Quartz produced only small grained silicon sheet [238].

Table 2.8 shows a summary of cells fabricated with ribbon material.

2.6 Silicon on Low Cost Silicon

Low cost silicon substrates have the advantages that the substrate is thermally stable and the substrate and active layer have matching coefficients of thermal expansion. If a diffusion barrier is not used they also provide an epitaxial template allowing for the possibility of a high quality grown layer. Epitaxy allows a low interface defect density and therefore a low back surface recombination velocity. It is relatively easy to fabricate a heavily doped interface between the grown silicon layer and the silicon substrate, which further reduces rear surface recombination. A disadvantage of bare silicon substrates is that long wavelength, weakly absorbed light will be lost into the electrically inactive substrate.

There are two main approaches for growing silicon layers on silicon. One is to grow epitaxial layers on high-throughput silicon ribbons or upgraded metallurgical grade silicon (MG-Si). High efficiencies have been achieved on a model system of good quality
multicrystalline substrates, but these have not yet been transferred to low-cost substrates.

Another approach is to use a barrier layer (most commonly SiO$_2$) to prevent diffusion of impurities from the substrate to the active layer. This produces grain sizes that are much smaller than those obtainable with a silicon epitaxial template. Recrystallisation is often used to overcome this hurdle, but this introduces extra costs. It is desirable that a diffusion barrier be reflective to long wavelength light and provide back surface passivation of the active layer.

The relative advantages of glass, opaque and multicrystalline silicon substrates have been considered by Blakers, using PC1D to model cells with the parameters expected to be achievable on each type of substrate [57]. It was found that, in cases where the silicon grown on the opaque substrate had an effective diffusion length more than twice that of the silicon grown on glass, the optical advantage of glass relative to an opaque substrate was completely offset by lower quality electrical properties.

<table>
<thead>
<tr>
<th>Technique</th>
<th>Thickness</th>
<th>Efficiency, $V_{oc}$</th>
<th>Comment</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>RGS</td>
<td>300–400µm</td>
<td>11.1%, 538mV</td>
<td>cell by University of Konstanz (UK)</td>
<td>[136, 186]</td>
</tr>
<tr>
<td>RGS</td>
<td>300–400µm</td>
<td>10.1%</td>
<td>cell by Fraunhofer ISE</td>
<td>[186]</td>
</tr>
<tr>
<td>RGS</td>
<td>300–400µm</td>
<td>9.8%</td>
<td>cell by ISFH</td>
<td>[186]</td>
</tr>
<tr>
<td>Dendritic Web</td>
<td>100µm</td>
<td>17.3%, 618mV</td>
<td>single crystal</td>
<td>[230]</td>
</tr>
<tr>
<td>String Ribbon</td>
<td>300µm</td>
<td>14.5%, 600mV</td>
<td>with PECVD SiN</td>
<td>[170, 263, 327, 328]</td>
</tr>
<tr>
<td>String Ribbon</td>
<td>100µm</td>
<td>10.9%, 568mV</td>
<td>screen printed with BLP</td>
<td>[359]</td>
</tr>
<tr>
<td>String Ribbon</td>
<td>200µm</td>
<td>15.2%, 581mV</td>
<td>cell by PSI</td>
<td>[104]</td>
</tr>
<tr>
<td>String Ribbon</td>
<td>–</td>
<td>14.3%, 596mV (average)</td>
<td>cell by UK</td>
<td>[138]</td>
</tr>
<tr>
<td>EFG</td>
<td>300µm</td>
<td>14%</td>
<td>routine</td>
<td>[174]</td>
</tr>
<tr>
<td>EFG</td>
<td>75–100µm</td>
<td>30–50µm (L$_{diff}$)</td>
<td>cylindrical growth on recrystallised ribbon</td>
<td>[171]</td>
</tr>
<tr>
<td>SSP (IMEC et al.)</td>
<td></td>
<td>13.1%, 563mV</td>
<td>on pre-ribbon</td>
<td>[107]</td>
</tr>
<tr>
<td>SSP</td>
<td></td>
<td>6.5%, 530mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSP (UK)</td>
<td>20–800µm</td>
<td>20µm (L$_{diff}$)</td>
<td>–</td>
<td>[238]</td>
</tr>
</tbody>
</table>

Table 2.8: Summary of ribbon growth achievements.
2.6.1 Examples for Silicon on Silicon

High Efficiency Approaches

In order to develop deposition techniques and optimise growth parameters, silicon has been deposited on single crystal substrates by many groups. This enables some judgement to be made of the ultimate efficiency potential of each technique. Heavily-doped monocrystalline silicon is in some ways a model of a poor quality silicon substrate in that it is electrically inactive but does not have the complication of grain boundaries. High efficiencies have been achieved with epitaxial layers grown by both LPE and CVD.

When moderately-doped active layers are grown to more than a critical thickness on heavily doped substrates (particularly boron doped substrates), misfit dislocations are generated. This is due to lattice mismatch caused by the differences in doping level. Experimental and numerical studies indicate that the recombination associated with these dislocations can limit $V_{oc}$ to around 660mV [106]. These cells remain a useful model because most fabrication technologies will result in at least moderate back surface recombination.

The effect of highly doped monocrystalline substrates on the efficiency of thin layers of active material has been investigated at Max-Planck-Institut für Festkörperforschung using PC1D and Sunrays [17]. It was discovered that, for active layer widths of 20μm, substrates with doping of $6 \times 10^{18}$/cm$^3$ could contribute 4% to the short circuit current. For active layer widths of less than 10μm, the contribution to $J_{sc}$ could be over 10%. For a thin layer cell with a high quality base and good front surface passivation, back diffusion of electrons into the substrate was determined to be important.

An early demonstration of this approach was at the Max-Planck-Institut für Festkörperforschung where a $V_{oc}$ of 663mV was achieved on a 20μm thick layer grown by LPE on a heavily doped substrate [60]. Later, an efficiency of 17.3% was demonstrated using CVD [346]. An efficiency of 15.4% was achieved at ASE GmbH by CVD on heavily doped monocrystalline silicon substrates with no texturing but with a DLAR coating [82].

LPE layers on heavily doped sc-Si substrates were used to produce a cell with an efficiency of 14.7% and a $V_{oc}$ of 659mV for a 16.8μm thick layer at Max-Planck-Institut für Festkörperforschung [347]. Effective diffusion lengths of up to 317μm were demonstrated on these layers.

The ANU achieved an efficiency of 18.1% and a $V_{oc}$ of 666mV using LPE growth on a lightly doped sc-Si substrate and an indium melt [59]. The epilayer was 35μm thick and the substrate was thinned to 15μm. Inverted pyramids were used to improve light trapping, while an oxide with boron diffused contact dots provided passivation of the rear
of the cell. Al on top of the oxide acted as a rear reflector and provided electrical contact to the base. The measured value for $J_{sc}$ included some contribution from the substrate because the substrate was lightly doped. A similar process yielded 17% on heavily doped sc-Si with most of the substrate removed [58].

An efficiency of 16.4% and a $V_{oc}$ of 645mV was achieved at UNSW on a 32$\mu$m thick layer with an area of 4cm$^2$ grown by LPE [366]. The substrate was heavily doped sc-Si and a high-efficiency cell process was used including a microgrooved surface texture, a ZnS/MgF$_2$ DLAR coating on passivating oxide, and a graded doping level in the active layer.

A multilayer cell with an efficiency of 17.6% and $V_{oc}$ of 664mV was fabricated at UNSW with 5 active layers and a p$^+$ buffer layer, deposited by CVD on a heavily doped Cz substrate [365]. Microgrooved and inverted pyramid passivated emitter (PESC) structures were used. Deep isolating grooves were used to define the cell area. Only the two uppermost n-type layers were connected in parallel via the texturing process. The other n and p-type active layers were floating except for the rear p-type layer, which was contacted via the p$^+$ buffer layer and the heavily-doped substrate.

Fraunhofer ISE have achieved an efficiency of 17.6% and a $V_{oc}$ of 661mV with a high efficiency cell process on a layer grown by RTCVD on a heavily-doped Cz substrate [110]. The cell had an active layer thickness of 37$\mu$m plus a 15$\mu$m thick BSF. IMEC achieved an efficiency of 14.9% on a 30$\mu$m thick layer grown by CVD [106]. Beijing Solar Energy Research Institute demonstrated an efficiency of 12.1% on a 20$\mu$m thick active layer deposited on a sc-Si substrate by RTCVD [334].

The effect of substrate thinning for cells fabricated on heavily doped silicon substrates has been investigated at UNSW [367]. Substrate thinning was found to increase $V_{oc}$ and FF by decreasing bulk recombination and hence the saturation current. Reflection of light from the thinned cell back surface was found to increase $J_{sc}$. MgF$_2$ between the silicon bulk and the aluminium contact was used to reduce the metal/silicon contact area and therefore reduce rear surface recombination. Cells were thinned to a total thickness of less than 50$\mu$m. Thinning improved the efficiency of poorer cells by a factor of 23.7% [368]. The spectral response of thinned cells was much improved, especially at long wavelengths.

**Silicon on Multi-crystalline Silicon**

Good quality multicrystalline silicon (mc-Si) has been used as a model to develop techniques for depositing silicon on silicon. In mc-Si grain boundaries are present but grains are large and impurity levels are not as high as in metallurgical grade silicon. Currently the cost of high quality multicrystalline silicon is too high for it to be used commercially...
as a substrate, but metallurgical grade silicon and some forms of ribbon-grown silicon are commercially interesting.

Modelling with PC1D at ANU has shown that cells without light trapping can still have good efficiencies if diffusion lengths are relatively large (ie. corresponding to lifetimes $> 1\mu s$), which can be achieved on mc-Si substrates [27]. The same group has used LPE on mc-Si substrates to produce a cell of 15.4\% efficiency and $V_{oc}$ of 639mV on a lightly doped substrate and a cell of 15.2\% efficiency and $V_{oc}$ of 639mV on a heavily doped substrate (with no texturing in either case, but with a TiO$_2$ ARC). It was estimated that the current originating from the lightly doped substrate was about 0.5mA/cm$^2$. Layers were grown 20–50μm thick. Periodic meltback was used to obtain a smooth morphology at the grain boundaries and thereby avoid emitter/substrate shunts.

A 13.3\% efficient cell with a $V_{oc}$ of 615mV was fabricated at IMEC and KU Leuven on a 20μm thick active layer grown by APCVD on a highly-doped mc-Si substrate [320]. The cell process included an ARC but had no other light confinement. It was found that the optimal resistivity for the active layer is about 0.2Ωcm since a higher resistivity increases the grain boundary barrier height. Microwave induced remote plasma (MIRP) hydrogenation increased the diffusion length from 19μm to 29μm. The back surface recombination velocity at the interface between the highly-doped substrate and the active layer was about $3 \times 10^3$cm/s.

Screenprinting and laser grooved buried grid processes have been applied to epilayers grown on mc-Si substrates in a collaboration between IMEC and BP Solar [319]. Layers were grown by APCVD to a thickness of 20μm at a growth rate of 5μm/min. A resistivity of 0.2Ωcm was achieved to a depth of 15μm. In the remaining 5μm, the resistivity was lowered due to indiffusion of dopants from the heavily doped mc-Si substrate. This reduced the active cell volume and hence increased $V_{oc}$. The short circuit current tended to increase due to the BSF effect, but to decrease due to the reduction in cell volume, so there is an optimum depth of indiffusion. The BSF due to the indiffusion also reduced the sensitivity of the cell to recombination at the substrate/epilayer interface. It was found that epitaxy induced a surface texture due to development of $\langle 111 \rangle$ facets on the grown layers. The texture resulted in a difference in $J_{sc}$ of 2.4mA/cm$^2$ between the textured cell and a non-textured cell simulated with PC1D. An efficiency of 13.2\% was achieved on a 20μm thick epilayer grown on a V-grooved mc-Si substrate. An industrial-type process was used that included POCl$_3$ emitter diffusion, PECVD nitride deposition, screenprinted metallisation, firing through nitride, parasitic junction removal and evaporation of MgF$_2$. This process resulted in an efficiency of 11\% on an epilayer grown on a non-textured, heavily doped EFG ribbon substrate. It was found that the level of hydrogen passivation achieved with firing
through nitride was not as high as that produced with microwave induced remote plasma (MIRP) hydrogenation [317]. Firing through nitride is attractive industrially because it is a much quicker process than MIRP hydrogenation.

A collaboration between Georgia Institute of Technology, Astropower, Sandia National Laboratories and EBARA Solar Inc investigated rapid thermal process (RPT) of various silicon substrates [262]. Efficiencies of 17.1%, 16.6%, 15.1% and 11.6% were achieved on FZ, Cz, dendritic web and polycrystalline Silicon-Film™ respectively without any conventional furnace processing steps. The process involved rapid, simultaneous emitter and BSF diffusion followed by rapid, low temperature deposition of a PECVD SiN/SiO2 DLAR coating. The trapped hydrogen in the SiN layer passivated bulk and surface defects. Slow cooling, rather than quenching during the rapid thermal anneal, improved the relative efficiencies of dendritic web and Silicon-Film cells by 50% and 15% respectively due to an increase in bulk lifetime. The process time for the emitter and BSF diffusion using slow cooling was up to 12 minutes.

LPE on MG-Si substrates with a Cu/Al solvent has been investigated at NREL [333]. A diffusion length of 42µm was achieved for a layer thickness of 30µm on a MG-Si substrate. LPE often takes place in a H₂ atmosphere to remove native oxide from the silicon but in this case an Ar atmosphere was used and the Al performs the native oxide removal. The Cu was found to reduce Al incorporation into grown layers. An advantage of this approach is the high silicon solubility in the Al/Cu solvent of 20–35 atomic%. This high silicon concentration has been found to result in more isotropic growth rates on grains of different orientations than solvents with lower Si solubilities, such as In or Sn, and also offers the potential for higher deposition rates. Resistivities of up to 0.2Ωcm were achieved with Cu levels below the threshold for solar cell degradation [89].

Epitaxial layers have been grown on heavily doped RGS-ribbon substrates by CVD in a collaboration between IMEC, KU Leuven and Bayer AG [318]. RGS silicon has a high dislocation density of 10⁸cm⁻² and a surface roughness of 100µm (±50µm) in a 400µm thick ribbon. No initial polishing steps to make the ribbons smoother were undertaken. The epitaxial layers had grain sizes of 10–100µm and a defect density of 10⁶–10⁷cm⁻². A cell efficiency of 10.4% and a V_{oc} of 558mV were achieved on a 30µm thick layer with an area of 25cm². The cell process included aluminium gettering of the substrates and passivation of the active layer bulk by microwave induced remote plasma hydrogenation. Diffusion lengths were 15–20µm after hydrogenation.

LPE with meltback has been used to grow layers on a UMG-Si substrate using the substrate as the silicon source. As the top surface of the substrate was dissolved into the melt, it was effectively etched by molten indium, leaving a mirror-like finish on the final
epitaxial layer. The substrate was heavily p-type, but removal of boron from the system and impurity segregation to the surface of the melt resulted in a relatively high quality layer with a bulk carrier concentration of less than $10^{17}/\text{cm}^3$. A 2cm$^2$ cell with a $V_{oc}$ of 597mV and 10.0% efficiency was achieved [188].

LPE has been used to grow layers on heavily doped RGS ribbons in a collaboration between Institut für Kristallzüchtung, Max-Planck-Institut für Festkörperpforschung and Universität Erlangen [325]. A slider system was used with an In solvent, a cooling rate of 0.7°C/min and a temperature range of 950–850°C and resulted in a thickness of about 20μm. The substrate was mechanically polished to reduce the roughness of the RGS substrate. Despite this, the epilayer had a roughness of about 20μm, which is in the same order as the layer thickness. Cells were fabricated but were found to be shunted due to contact of the emitter to the p+ RGS substrate at dips in the epilayer.

Silicon Sheets from Powder (SSP) is a ribbon material with an average grain size of 60μm and a dislocation density of $10^6–10^7\text{cm}^{-2}$. The ribbons have a surface roughness of 200μm over 5m. This can affect the width of grid fingers (according to whether they are close to the mask or not). Epitaxial layers have been grown on SSP ribbon at Fraunhofer ISE using a RTCVD system designed to offer the technical potential to be convertible to a continuously operating system [109]. Growth rates of up to 10μm/min have been demonstrated. A cell with an efficiency of 8.0% and a $V_{oc}$ of 553mV was achieved on RTCVD epitaxial layers deposited with this system on SSP ribbons [111]. A cell with an efficiency of 13.2% and a $V_{oc}$ of 614mV was also achieved on heavily doped mc-Si with this system [110]. The diffusion length was 8.5–12μm for a cell thickness of about 10μm. IMEC and KU Leuven achieved an efficiency of 7.6% using CVD layers on SSP pre-ribbon with MIRP hydrogenation [321].

**Silicon on Diffusion Barriers**

If a diffusion barrier is deposited between the active layer and a low-cost substrate, then diffusion of impurities from the substrate into the active layer can be reduced. The diffusion barrier properties of SiO$_2$ (deposited by PECVD) have been investigated at Fraunhofer ISE [255]. Iron was used as the introduced impurity because it is fast-diffusing and can significantly reduce minority carrier lifetimes. It was shown qualitatively that SiO$_2$ of 0.5 to 4μm thickness is a good diffusion barrier against iron at temperatures of 1000–1400°C with typical solar cell processing times.

It is important to achieve low recombination rates at the silicon/diffusion barrier interface. One way of doing this is to dope the diffusion barrier with boron.

Porous silicon has been used as an intermediate layer for growth on low quality sili-
con substrates [52]. It was found that the porous silicon acted as a diffusion barrier and gettered impurities from the substrate. Porous silicon also acted as a back side reflector, which is otherwise difficult to achieve with a silicon substrate. In order to achieve reasonable epitaxial quality, deposition temperatures were limited to 800°C.

Silicon deposited onto diffusion barriers (other than porous silicon) without recrystallisation tends to have a small grain size. Delft University of Technology found silicon deposited on SiO₂ by CVD with or without a LPCVD nucleation layer had average grain sizes of 1–2μm [372].

Recrystallisation is often done to increase grain size and improve electrical properties. Mitsubishi Electric Corporation produced a 4cm² cell of 16.4% efficiency and V_{oc} of 608mV [163] (not confirmed independently) and a 100cm² cell of 14.2% efficiency [164] (confirmed independently) by ZMR and CVD on SiO₂. LPCVD was used to deposit 3–5μm of μc-Si on SiO₂ grown on sc-Si substrates. Capping layers of SiO₂ and Si₃N₄ were deposited and ZMR was applied. The capping layers were etched away and a BSF layer followed by the active layer were deposited by CVD to a thickness of about 60μm. The substrate and rear SiO₂ were removed to allow contact to the rear of the cell, except for a grid, which was left unetched to provide mechanical stability. H⁺ ion implantation from the rear was used for defect passivation and an oxide was used for front passivation. It was found that hydrogen passivation increased cell efficiency by a factor of 20–30% [19]. The influence of the ZMR scanning speed was investigated by varying it from 0.2–1mm/s. Defect densities were 2×10⁶cm⁻² at 0.2mm/s and 3×10⁷cm⁻² at 1mm/s. It was found that the (100) orientation dominates at low scan speeds, so anisotropic etching can be used for texturing to form random pyramids. An AR coating was used to further improve light trapping. Diffusion lengths of up to 150μm were achieved with low scanning speeds and H⁺ passivation. It was found that the scanning speed could be increased to 3mm/s with good results if the seeding layer was thinner (0.5μm) [29]. Fine temperature control of the ZMR was shown to be important in achieving low defect densities [175]. A later development of this technology is to etch via holes through the grown layer and dissolve the SiO₂ with HF, allowing detachment of the grown layer and recycling of the substrate (see section 2.7.1).

Promising results have also been achieved in a collaboration between IMEC and Fraunhofer ISE [33]. The process involves deposition of SiO₂ on sc-Si, followed by chemical vapour deposition of a seeding layer and a capping layer of SiO₂, ZMR, phosphorus gettering and etch-back, and deposition of the active layer. A dry cell process developed by Fraunhofer ISE produced a cell of 9.3% efficiency on a layer with a boron doped initial SiO₂ layer. An interdigitated IMEC process without an AR coating resulted in a cell of
Figure 2.5: Cross section of the epitaxial layer, perforated SiO$_2$ barrier and SSP substrate structure produced at Fraunhofer ISE.

4.8% efficiency on a 30μm thick layer. Surface roughness (2–3μm) caused problems, which were solved by mechanical polishing for the Fraunhofer cells and a different resist spinning procedure for the IMEC cells. Diffusion lengths of 12–17μm were achieved. It was found that intra-grain recombination dominated performance in these cells. An efficiency of 12.8% was achieved with a non-dry cell process that included texturing and hydrogen passivation [256]. The same process on SSP substrates produced from semiconductor grade silicon powder resulted in an efficiency of 10.4% for a 1cm$^2$ cell. SSP substrates made from low-cost silicon powder were too rough to undergo ZMR without a surface smoothing treatment. In 2001, Fraunhofer reported a cell efficiency of 12.3% (594mV) on mc-Si and 11.3% (578mV) on SSP substrates. Both results were for 1cm$^2$ cells [180].

The advantages of bare silicon and silicon that has been coated with a diffusion barrier can be combined to some extent by using a substrate that provides a partial epitaxial template and a partial diffusion barrier. A perforated SiO$_2$ barrier on a silicon substrate has been investigated at Fraunhofer ISE. SiO$_2$ was deposited on SSP ribbon, the SiO$_2$ layer was perforated with a lithographic process, and an epitaxial RTCVD seeding layer was deposited, as shown in figure 2.5 [370]. This layer was then recrystallised by large area melting and the active layer was grown on top. The perforation (seeding) holes were 250μm in diameter on a 2.5mm grid so they covered about 1% of the surface. Grain size after recrystallisation was found to be determined by the distance between the seeding holes, which was about 2.5mm. The cell process included remote plasma hydrogenation and resulted in a cell efficiency of 11.5% and a $V_{oc}$ of 562mV with an effective diffusion length of 35–70μm for an active layer thickness of 50μm.

A variant of this approach is epitaxial lateral overgrowth (ELO). Silicon is grown epitaxially out of seeding holes in a barrier layer (usually SiO$_2$). The silicon overgrows the barrier layer and closed layers can be achieved. ELO utilises the large differences
in growth rates of different crystal orientations achievable on silicon. Width to height ratios for single crystal epitaxial layers grown by this technique can be as high as 40:1 for substrates slightly misoriented from (111) [28]. Growth is performed near thermal equilibrium so that silicon is not deposited directly on the barrier layer. Epitaxial lateral overgrowth for solar cells has been investigated at the University of Delaware using LPE over SiO₂ on highly doped sc-Si substrates [4]. The aim was for the interlayer to eventually be both reflecting and passivating. The active layer/SiO₂ interface had a reflectivity of about 40%. The level of passivation provided when silicon overgrows SiO₂ is unknown but it will need to be large if high efficiencies are to be achieved. Epitaxial lateral overgrowth by CVD has been investigated at Delft University of Technology [372]. SiO₂ lines 2µm wide covering 50% of the wafer area were obtained by lithography. Growth was epitaxial but many twins were observed over the SiO₂ regions.

Beijing Solar Energy Research Institute has used RTCVD to deposit silicon on sc-Si p⁺⁺ substrates with perforated SiO₂ or Si₃N₄ interlayers [334]. Better morphology was found for layers grown on Si₃N₄, possibly because the silicon tended to ball up on the SiO₂ and create gaps between the grains. The grain orientation was preferentially ⟨100⟩ on SiO₂ and ⟨111⟩ on Si₃N₄.

RF PECVD has been used to grow μc-Si at 0.12µm/min on bare and SiO₂-covered c-Si at Saitama University [16, 15]. The effect of the surface roughness of SiO₂ was investigated and it was found that crystallinity was improved by a moderately roughened SiO₂ surface.

Deposition of silicon by PECVD on Si, SiO₂ and quartz has been investigated at Kyoto University with temperatures of 500–900°C [369]. Film thickness were 0.5–3µm with growth rates of 5–40nm/minute. Films on SiO₂ had a very strong ⟨110⟩ orientation at 900°C. It was found that films were amorphous below 600°C and that crystallinity improved as the temperature increased. Between 600 and 800°C films were partly polycrystalline and above about 800°C films were totally polycrystalline.

A large range of grain sizes introduces nonuniformities in the minority carrier diffusion length that can result in a cell whose performance is dominated by poor quality regions. One way to address this is to control the location of nucleation sites. Canon have introduced a selective nucleation-based epitaxy process (SENTAXY) [191]. This involves the use of artificial nucleation sites to control the size of crystallites and their boundaries. SiO₂ on sc-Si is irradiated with silicon ions to form a lattice of silicon-rich SiO₂ points that behave as artificial nucleation sites. Silicon is then deposited by CVD. Islands of SiNₓ in SiO₂ have also been used to provide artificial nucleation sites. Canon have also developed a low-temperature SENTAXY technique.

Table 2.9 shows a summary of silicon on silicon achievements.
# Review of Thin-Film Silicon Solar Cells

<table>
<thead>
<tr>
<th>Institution</th>
<th>Substrate</th>
<th>Deposition Method</th>
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<th>Refs</th>
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<td>sc-Si</td>
<td>CVD</td>
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<td>ZMR &amp; CVD</td>
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<tr>
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<td>ZMR &amp; CVD</td>
<td>9.3%, 529mV</td>
<td>[33]</td>
</tr>
<tr>
<td>Fraunhofer ISE</td>
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<td>LPCVD &amp; ZMR</td>
<td>6.1%</td>
<td>[144]</td>
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<tr>
<td>Delft UT</td>
<td>SiO₂ on Si</td>
<td>CVD</td>
<td>grain size 1–2μm</td>
<td>[372]</td>
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</tbody>
</table>

Table 2.9: Summary of silicon on silicon.
2.7 Lift-off Silicon Layers

Thin film silicon layers that can be detached from a reusable silicon substrate have a very high efficiency potential. This is mainly due to the fact that because the substrate is recycled, there is no need to compromise on material quality. The inherent disadvantages of deposition on non-silicon substrates such as diffusion of impurities, material defects and film stresses are absent [139]. The radiation tolerances of these thin-film cells may be very high because large amounts of damage can be sustained before the diffusion length falls to less than the wafer thickness.

Most of the groups working in this area grow single crystal silicon on a high quality substrate with a sacrificial attachment region. This region may be of a different doping level, made from porous silicon or made from SiO₂. A disadvantage of using doping levels and dopant selective etchants is that high temperatures may broaden doping profiles. A porous silicon sacrificial layer allows epitaxy, bonding and oxidation to occur at higher temperatures. Porous silicon also has a very high etch selectivity over non-porous silicon; ratios of up to $10^5$ have been demonstrated [270]. For growth processes that use hydrogen, less hydrogen is used in the growth of sc-Si, compared with the case of non sc-Si during which hydrogen is used to passivate grain boundaries [73].

Groups who are working on detachable layers include Mitsubishi Electric Corporation, Canon, Sony Corporation, the University of Erlangen, the University of Stuttgart, IMEC, INSA (in Lyon), the Australian National University, Silicon on Insulator Technology (SOITEC), Canon and LPM. With the exception of Canon, the groups detailed here aim to recycle the substrate.

2.7.1 VEST process - Mitsubishi Electric Corporation

A 77µm thick cell with an area of 96cm², an efficiency of 16% and a $V_{oc}$ of 589mV was achieved using the VEST (etching of underlying substrate through what are termed ‘via-holes’ in the silicon film) process at Mitsubishi Electric Corporation [139, 219]. The Mitsubishi technique was shown to be reliable with a batch of cells of 10cm² area from which 22 out of 25 had an efficiency greater than 15% [139]. A 13.1% efficient module of 924cm² was also demonstrated [218].

VEST cells are made by first separating the active layer from the substrate and then fabricating a cell. Figure 2.6 shows the VEST cell structure. Layer separation is achieved by forming a silicon on insulator (SOI) layer on SiO₂ deposited on a c-Si wafer. A thin seeding layer of silicon is deposited by CVD with a capping layer. This is followed by zone melt recrystallisation (ZMR). The resulting silicon is mainly (100) orientated. A
back surface field and thick active layer are then deposited by CVD. An anisotropic etch through a masking layer is used to form an array of 100 μm² via holes through the silicon layer to the underlying SiO₂. The hole spacing is 1.5mm. The SiO₂ layer is removed by HF that enters through the via holes, causing layer separation. Cell fabrication is preceded by another anisotropic etch that forms random pyramids on the front surface.

Cell fabrication involves a phosphorous diffusion to form a heavily n-type region over the entire surface and down the via-holes, an etch back of the front surface to form the emitter and application of a SiN antireflection coating using LPCVD. The final steps are; formation of an interdigitated pattern of n and p regions on the rear surface, screen printing of both base and emitter electrodes on the rear and hydrogen ion implantation for passivation. Recently, a plasma CVD process has been used to provide both hydrogen passivation and an ARC [218]. The electrodes are made of a paste that is screen printed directly onto the cell. For the emitter it is an Ag paste and for the base, an Al containing Ag paste [219].

A feature of the VEST technique is that the ZMR process results in a mostly (100) surface orientation which allows texturing. Finger shading losses can be avoided since both electrodes are on the rear and current is collected from the sunward surface through the via holes. The c-Si substrate may be recycled [139].

The VEST cell fabrication technique has been optimised to overcome a number of difficulties. The diffusion length, L_{diff} after ZMR is quite low (40 μm) and this was increased to 167 μm by phosphorous gettering and etch back. There was a low fill factor caused by the high series resistance of the emitter since both contacts are on the rear and the via holes are widely spaced. This has been partially overcome by arranging for a heavy phosphorous diffusion in the via holes and a lighter diffusion on the top surface. The top

**Figure 2.6:** Schematic of the VEST cells, after Morikawa [219].
surface diffusion is typically 60Ω/□, which results in a moderate loss of blue response. A
drawback of the VEST technique is that at present the electrodes are formed by a screen
printing process, which requires a minimum film thickness of about 80µm [139].

2.7.2 Porous Silicon

A sacrificial porous silicon layer has been used for layer transfer by a number of groups.
The first of these was Sony.

Sony Corporation

Sony Corporation have used a sacrificial porous silicon layer and have achieved a 12µm
thick, thin-film cell of 4.0cm² area, with an efficiency of 12.5% and V_{oc} of 623mV [309].
A material lifetime of 60µs was demonstrated. The highest cell efficiency reported to date
is 14.0% for a 1.6mm×10cm cell [307].

Sony cells are made by first anodising a silicon substrate. Three porous silicon layers
are formed, two of low porosity (16% top layer and 26% bottom layer) and one of high
porosity (40–70%). The location of the high porosity layer is shown in figure 2.7 and its
function is to allow easy separation of the cell layer from the substrate. The crystalline
structure and pore distribution of the porous silicon are altered by a high temperature
hydrogen anneal at 1100°C for 30 minutes. This causes the low porosity layer to form
small, circular pores while the high porosity layer tends to form broad based pillars and
wide voids. During this anneal, the porous layer also acts to getter metals. Epitaxial
growth of the active silicon layer occurs directly onto the top surface of the substrate
and as this is of low porosity, the grown layer has a low lattice strain. A thin p⁺ layer
(approximately 1µm) is grown epitaxially onto the substrate, using silane and hydrogen
diluted B₂H₆ gas at atmospheric pressure. This is followed by the growth of a thicker
p-layer (approximately 11µm) that forms the base region of the solar cell. Phosphorous
diffusion, application of a TiO₂ antireflection coating and metallisation completes the cell.
Layer separation is achieved by the application of a weak tensile stress or ultrasound. The
porous layer is then removed and the substrate can be recycled [309].

The 12.5% efficient cell had an oxidation step that served to passivate the front surface
and a TiO₂ antireflection coating. An inexpensive plastic film was adhered to the front
surface for mechanical strength. A minor disadvantage of the process developed at Sony
is that the porous layer is 8µm thick at present and this is sacrificed in cell production. A
planned improvement is to put an optical reflector on the rear of the cell [307].

In 2001, Sony reported a mini-module of 10×10cm² made of 48 cells. The highest
single cell efficiency was 14.0% for a 1.6mm×10cm [307] cell. A second module with four
cells each measuring $1\times1.5\text{cm}^2$ resulted in a $V_{oc}$ of 2.41V, but a low $J_{sc}$. The highest individual cell efficiency was 9.4%. Cells on this wafer were isolated after cell formation, which perhaps explains the low $J_{sc}$ values [308]. A $10\times10\text{cm}^2$ cell was transferred to a plastic film and demonstrated a 5cm radius of curvature. The efficiency was low; only 1.5% [150].

Ψ Process - University of Erlangen

The Perforated Silicon (Ψ) process has been used to make cells at ZAE Bayern at the University of Erlangen. A lifetime of 0.27$\mu$s and $L_{\text{diff}}$ of 11$\mu$m on a 5.8$\mu$m thick layer [75] were demonstrated and more recently, a diffusion length of more than 32$\mu$m on a 16$\mu$m layer was also shown [76, 115]. A cell efficiency of 4.4% (501mV) was reported for a 7$\mu$m thick cell transferred to a glass substrate [115]. The highest cell efficiency reported to date is 13.2% for a $4\text{cm}^2$ cell that was part of a 16$\mu$m thick module of $5\times5\text{cm}^2$ with an overall efficiency of 10.6% and a $V_{oc}$ of 3.035V [115, 76].

The first step in the Ψ process is the texturing of the surface of a sc-Si substrate using a combination of photolithography and KOH etching. Two distinct porous silicon layers (PSL) are then formed on the substrate using an anodic etch in HF solution. The upper layer is about 30% porous and the lower about 50%. The PSL are stabilised by an oxidation step. Prior to epitaxy, the sample is heated to 850°C for around 10 minutes to remove the native oxide that forms on the porous silicon. To make cells, a layer of silicon is deposited using ion assisted deposition (IAD) at a substrate temperature of 700°C. Deposition rates of 1Å/s have been achieved [40, 50]. The deposited film has the same crystallographic
structure as the substrate. A low temperature deposition technique is advantageous since at temperatures greater than 850°C, sintering of the porous silicon occurs due to the surface mobility of silicon atoms on the inner surface. Once cell fabrication is complete, the layer can be separated from the substrate using mechanical stress. This is done by attaching a glass superstrate to the front surface with a transparent encapsulate (poly-ethylenphthalate). Further steps, such as surface passivation and reflector formation on the rear surface, must occur below a temperature that both the encapsulate and superstrate can withstand. Earlier versions of the Ψ cells, which did not have the two porosity levels, were removed by a 2 minute ultrasonic agitation. The rear surface was then passivated and a reflector added. After removal of the PSL layer, the substrate can be reused several times before retexturing [73, 75]. Future improvements that are planned include a reduction in the porous layer thickness (currently 10–15μm thick [189]) and an increase in the deposition rate [73, 75].

Work on the Ψ process to produce waffle cells has been done by ZAE Bayern at the University of Erlangen. The films are termed waffle due to the three dimensional texturing of the entire film. The optimum period of texturing for effective light trapping (and reflection control) has been theoretically determined to be about the same as the waffle thickness. Layers of 85mm in diameter have been separated from the substrate using mechanical stress. A feature of this technique is that the emitter is grown epitaxially, since this is faster than diffusion. A 7.8μm thick, pyramidal structure with a dislocation density less than $10^4$/cm$^2$ was formed [73].

In 2001 ZAE Bayern reported a diffusion length of more than 32μm on a 16μm thick wafer and a mini-module also with a thickness of 16μm, a $V_{oc}$ of 3.035V and an overall efficiency of 10.6%. Single cells were 4cm$^2$ and the total module was 5×5cm$^2$. The highest single cell efficiency was 13.2%. An important achievement of this work is that the mini-modules did not use photolithography and did not require any high temperature oxidation steps. Substrate re-use has been demonstrated with a single wafer being used four times [115, 76]. A 15.5μm thick layer was processed into a cell with a $V_{oc}$ of 600mV without using photolithography [76, 115].

**QMS - University of Stuttgart**

Quasi-monocrystalline silicon (QMS) has been developed by IPE at the University of Stuttgart and cell efficiencies on glass substrates of 13% for a 14.5μm thick cell, 15.4% for a 24.5μm thick cell and 16.6% for a 44.5μm thick cell were reported. A mini-module with six series connected cells each 0.81cm$^2$ was reported with a total $V_{oc}$ of 3.5V, but a comparatively low fill factor at 0.55 [37].
The silicon has been termed 'quasimonocrystalline silicon' (QMS) due to the high density of voids [40, 49]. Deposition is done using CVD and the deposition temperature is relatively high (1100°C). Layer thickness is 12–50μm and consists of an initial back surface field layer, followed by an absorber layer. The front grid is formed using photolithography and a SiNx ARC is used. Separation of the layer is by mechanical force after attaching it to glass using an organic resin. Modelling has been done that showed that a 25μm thick layer with a \( L_{\text{diff}} \) of 40μm may lead to a 17% cell [40, 49].

**Porous Silicon on Ceramics - IMEC**

A group from IMEC, Belgium are looking at porous silicon layers that can be lifted off a silicon substrate, onto a ceramic substrate where CVD will be used to grow the active cell. The transfer and bonding of the porous silicon layer to uneven and flat ceramic surfaces has been demonstrated. The advantage of this technique is that it avoids any uncontrollable lift-off of the seeding layer during cell processing. The technique requires a ceramic that can withstand the high temperatures of cell fabrication and is therefore likely to be expensive [53].

**Institut National des Sciences Appliquées de Lyon**

A group in France are also working on porous silicon transfer layers, in this case, liquid phase epitaxy is used to grow the cell layer on the porous substrate. Growth has been on p-type silicon and was found to produce a pyramidal structure on (100) oriented silicon and a flat structure on (111) oriented silicon [38].

**2.7.3 Epilift Process - Centre for Sustainable Energy Systems, ANU**

At the Centre for Sustainable Energy Systems, ANU, the epilift process has been used to grow layers of 50–100μm thickness on single crystal silicon. A lifetime of 3.8–11.7μs for a sample with a light phosphorous diffusion and thin oxide as surface passivation was demonstrated [83].

The epilift process involves deposition and patterning of a masking layer on a sc-Si substrate. The masking layer is exposed in a mesh pattern; lines are of 2–10μm width and spaced 50–100μm apart. The substrate is usually orientated in the (100) direction, the mesh in (110) directions. An epitaxial layer is grown on the substrate using liquid phase epitaxy (LPE). The growth faces have mostly (111) orientation and the layer has a diamond cross section, giving it a natural antireflection texture. Initially deposited layers are more heavily doped (which means they are etched faster) and later layers more lightly
doped. A selective etch is used to remove the epilayer. The masking layer and substrate may be reused, provided the masking layer is not attacked by the etch. Figure 2.8 shows an SEM image of an epilayer structure attached to a substrate [83, 338].

The epilift layer grows in a mesh pattern and the holes can be closed over to an arbitrary amount. An advantage of the holes is that they allow both contacts to be on the rear, thereby avoiding shading losses. A possibility for cell fabrication is to leave the epilayer partially attached to the substrate (for example, at the corners) and to process the cell, attach the epilayer to a superstrate and then detach the cell from the substrate [338].

An indium solvent is used in the growth of epilayers, and films with an area of $10\mathrm{cm}^2$ and a thickness of up to 100$\mu\mathrm{m}$ have been detached. A film without holes was achieved by leaving an epilayer attached only at the corners, growing again and using shear force to separate the layer. A potential problem with the technique is that the material may have a high dislocation density [338]. The dislocations are due to the oxide mask and are not evenly distributed across the wafer [83]. A cell efficiency of 10.4% was reported using this process [342].

2.7.4 Smart Cut - SOITEC

‘Smart Cut’ technology has been introduced at Laboratoire d’Electronique de Technologie et d’Instrumentation (LETI) and co-developed with SOITEC (Silicon on Insulator Technology). The technique provides a method for separating a thin layer of silicon from a bulk
wafer [96]. At present it is mainly in use in the IC industry, although it has applications for solar cells. The technique involves growing a SiO$_2$ layer and implanting hydrogen into the silicon underneath this layer. Most of the hydrogen atoms are a uniform distance below the silicon/SiO$_2$ interface, creating a mechanically weakened layer. By bonding the SiO$_2$ layer to a silicon wafer or a quartz or glass superstrate, a thin (200nm) layer of silicon can be peeled from the original wafer [96]. When a silicon wafer is used as the superstrate, separation is achieved using a heat treatment at $400-600^\circ$C. A second heat treatment at more than $1000^\circ$C is used to strengthen the chemical bonds between the superstrate and the thin silicon layer. The substrate wafer can then be polished and is ready for hydrogen implantation and reuse [96]. An advantage of the technique is that the silicon layer has defect levels close to those of bulk silicon [79].

Since the separated layer is very thin, epitaxial growth of a thicker active layer of silicon must take place after separation of the seeding layer from the substrate. A supporting superstrate that has a thermal expansion coefficient similar to silicon will be needed for this process. A number of options exist for such a substrate, such as an oxidised silicon wafer with pre-existing holes at a 1mm spacing. Separation of this wafer from the epitaxially grown layer would simply require immersion in hydrofluoric acid (HF). There is some concern about the cost of hydrogen implantation.

### 2.7.5 Eltran Process - Canon Incorporated

A technique termed ELTRAN (epitaxial layer transfer) has been developed by Canon. This is based on a new BESOI (bond and etch back of silicon on insulator) technology [270]. An epitaxial layer is formed on a $10 \mu$m thick porous silicon layer by chemical vapour deposition (CVD) at 1000–1150$^\circ$C and the rear of the surface is exposed by grinding away the original wafer. The porous silicon can then be removed. An etchant selectivity of $10^5$ has been achieved [270]. At present, the fact that the substrate wafer is destroyed makes this process inapplicable for solar cell technology. In future, the technique may be adapted for photovoltaic applications.

Canon have also developed the SCLIPS process. This involves LPE growth on porous silicon films and lift-off using a water jet. A $10 \mu$m thick silicon film has been detached and used to make a 9.5% efficient cell [237].

### 2.7.6 LPM - CNRS

A group from LPM-CNRS have formed epitaxially grown thin-film layers 25$\mu$m thick. The method involves direct texturing of nc-Si, grid formation and LPE growth. The grid is
formed by patterning and electrochemical etching of the substrate. Growth is done by LPE with the grid either attached or detached. It is intended to eventually transfer the grid to another substrate, for example, mullite \((\text{Al}_6\text{Si}_2\text{O}_{13})\) [112].

Table 2.10 shows a summary of lift-off achievements.

### 2.8 Cell Design

It has been known for some time that thin cells have the potential for higher efficiency than thicker cells due to reduced bulk recombination [126, 314]. In order to realise this potential, it is essential that excellent surface passivation and light trapping be implemented. Depositing silicon on foreign substrates or low-quality silicon tends to result in small grain sizes and short effective diffusion lengths. The need to obtain high currents within these constraints has led to thinner cells and to novel cell designs.

An advantage of deposited silicon as opposed to silicon wafers or ribbons is that doping can be incorporated in the deposition process. This means a diffusion step can be avoided. Deposition also allows doping profiles that would be difficult or impossible to obtain with diffusions. Deposited or grown silicon layers also lend themselves to novel module designs, such as series interconnected cells. An increasing number of groups are working in this area.

#### 2.8.1 Efficiency Potential of Thin Crystalline Silicon Solar Cells

The efficiency potential of thin cells has been investigated both theoretically and experimentally. The results in this section apply to cells of conventional design, and do not consider multiple junctions or drift fields, for example.

<table>
<thead>
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<th>Group/Technique</th>
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<th>Comment</th>
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<td>16%, 589mV</td>
<td>poly-Si layer</td>
<td>[139, 219]</td>
</tr>
<tr>
<td>Sony Corporation</td>
<td>12μm</td>
<td>14.0%</td>
<td>1.6mm×10cm</td>
<td>[309]</td>
</tr>
<tr>
<td>Ψ process</td>
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<td>13.2%</td>
<td>-</td>
<td>[73, 75, 115]</td>
</tr>
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<td>44.5μm</td>
<td>16.6%</td>
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<td>slicing method</td>
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<td>-</td>
<td>[79, 96]</td>
</tr>
<tr>
<td>Canon, SCLIPS</td>
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<td>-</td>
<td>transfer to ceramic</td>
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<td>INSAL</td>
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<td>-</td>
<td>LPE on porous silicon</td>
<td>[38]</td>
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Table 2.10: Summary of lift-off silicon layers.
Experimental Studies of Efficiency Potential

The most efficient thin silicon solar cell produced to date is a 21.5% efficient cell, with a $V_{oc}$ of 699mV, incorporating a rear n-type inversion layer, fabricated on a 47µm thick, chemically-thinned FZ wafer at UNSW [331]. A 20.6% cell with a $V_{oc}$ of 683mV on a thinned 47µm thick FZ wafer was achieved at Max-Planck-Institut für Festkörperforschung [71]. An analytical model for the internal quantum efficiency (IQE) was used to calculate the back surface recombination velocity ($S_b$) and minority carrier diffusion length ($L_b$) of the 20.6% efficient cell from measured quantum efficiency spectra for cells with light trapping and back surface fields. ($L_b$ and $S_b$ are adjusted to reproduce measured IQE and reflectance data.) The model also includes the current contribution from the emitter so it is applicable to very thin cells. It was found that $L_b$ was greater than 100µm and $S_b$ was less than 1000cm/s. Using Cz material, a 19.6% efficient cell (653mV) was achieved on a 115µm wafer using the RP-PERC cell structure [336].

Theoretical Studies of Efficiency Potential

The maximum theoretical efficiency for silicon solar cells is imposed by Auger recombination [126, 314]. $V_{oc}$ will increase as cell thickness decreases because the volume for Auger recombination decreases. With perfect light trapping, $J_{sc}$ is independent of thickness, whereas with Lambertian light trapping, and probably any realistic light trapping scheme, $J_{sc}$ decreases as cell thickness decreases. This leads to a broad maximum in efficiency of about 29% at a cell thickness of 50–100µm [56, 314]. In a real cell as the cell thickness is reduced, a point will come where recombination at the cell surfaces and elsewhere will dominate the total recombination and $V_{oc}$ will saturate. Very low surface recombination and a large ratio of minority carrier diffusion length to cell thickness are needed to approach the Auger limit [126]. Modelling with PC1D [90] has shown that ratios of $L/W$ of at least 5 and surface recombination velocities less than 100cm/s are needed to achieve a $V_{oc}$ of 700mV.

The influence of the grain size and dislocation density of polycrystalline cells when one of these parameters dominates the cell performance has been examined in a collaboration between Toyota Technological Institute, Toyota Central R&D Labs, and Simitomo SiTiX Corp [160, 161]. The relationships between minority carrier diffusion length and grain size or etch pit density were obtained empirically. These equations were then used to predict cell performance with PC1D. It was predicted that an efficiency of 17% is attainable for a grain size of 10µm and an etch pit density of $1 \times 10^6$cm$^{-2}$ with a film thickness of 2µm if effective light trapping can be achieved. To achieve 17% efficiency with a cell thickness of
10\(\mu m\), a diffusion length of 70\(\mu m\) and an internal reflectance of more than 90% were found to be necessary. This demonstrates the importance of light trapping for highly efficient thin silicon cells. It was found that the shape of the IQE curve gives some indication as to whether the minority carrier diffusion length or the internal reflectance is responsible for poor cell properties.

2.8.2 Design Considerations for Thin Cells Deposited on Substrates

Much effort has been directed recently to fabricating thin cells on insulating substrates including glass and some types of ceramics. To provide electrical contact to these cells either a conducting layer must be deposited prior to the silicon deposition or both contacts must be placed on the same side of the cell in an interdigitated design. Transparent conducting oxides, commonly used with amorphous silicon cells, could be used for contacting cells fabricated on glass superstrates.

For cells on glass superstrates, interdigitated designs have an advantage over conventional cell designs in that shading losses are avoided. The usual trade off between shading and series resistance for a front grid is eliminated and series resistance can be minimised by metallising most of the back of the wafer. Back junction cells also have a potential advantage in that the emitter does not need to be optically transparent and so can be thicker in order to reduce series resistance losses. The requirements on material and passivation quality for a front junction design are not as severe as for a back junction design, as described below. For cells on transparent substrates, this fact has to be weighed against the shading loss and more restricted emitter optimisation of a front junction design. For cells fabricated on non-transparent, insulating ceramics, both contacts must be placed on the front of the cell, which is a disadvantage as shading losses are increased.

Almost all the light in a silicon solar cell is absorbed near the front (about 50% in the first 3\(\mu m\)). Thus front junction cells have the advantage that most of the carriers are generated near the junction. The ratio of minority carrier diffusion length to cell width (L/W) has increased importance for back junction cells because minority carriers must be transported further. Modelling with PC1D [32] shows that \(J_{sc}\) drops rapidly for a well passivated back junction cell as L/W is decreased below 2. For a front junction cell the drop in \(J_{sc}\) is much slower and a high collection probability can be achieved for L/W equal to 1. For the same reason it is more important to avoid horizontal grain boundaries in a back junction cell. For a given material quality the optimum thickness of a back junction cell is therefore smaller than that for a front junction cell. This will tend to result in a lower \(J_{sc}\) in the back junction cell for a given light trapping scheme.

It is also very important that the front surface of a back junction cell is well passivated.
Because of the high density of carriers at the front of the cell, a high surface recombination velocity will significantly reduce \( J_{sc} \) as well as \( V_{oc} \). The carrier concentration gradient from the front to the rear of the cell is smaller in a cell with a high front surface recombination velocity, resulting in a lower rate of carrier transport to the back of the cell. The optimum thickness of a back junction cell is therefore lower for a cell with a higher front surface recombination velocity.

Currently, passivation of interfaces is more difficult than passivation of surfaces, which may affect the optimum cell design for layers grown on substrates or transparent superstrates. For a cell grown on a substrate, a heavily doped region can be used to reduce recombination at the rear of the cell. A heavily doped region could also be used to achieve low front surface recombination for layers grown on transparent superstrates, but this could lead to reduced collection efficiency for short wavelength light due to low lifetimes in the heavily doped region. Interface recombination is a potentially serious problem for cells grown on a glass superstrate.

### 2.8.3 Interdigitated Cells

Recent results from Fraunhofer ISE have indicated that the interdigitated design can be almost as efficient as conventional designs. An efficiency of 22.1\% on 1\( \Omega \)cm FZ wafers was achieved when the cell was illuminated from the non-contacted side [98]. Optimum performance was achieved by including a floating emitter at the front surface to minimise front surface recombination. It was found that the current is non-linear with light intensity and that this is well described by shunting at the floating emitter. The passivation quality of the floating emitter depends on the excess carrier density. Under all operating conditions, losses in the base are dominant, which underlines the high passivation quality of the floating emitter. The surface recombination velocity of the oxide passivated random pyramid texture was three times higher than for an equivalent planar surface. Good agreement between modelling and measurement was obtained when metal and perimeter losses were included. The Fraunhofer ISE interdigitated cell design is shown in figure 2.9.

An interdigitated 46\( \mu \)m thick cell grown epitaxially by CVD on a monocrystalline SIMOX silicon-on-insulator (SOI) substrate wafer had an efficiency of 19.2\% [146]. SIMOX is Separation by Implanted Oxygen and uses high dose oxygen implantation into a sc-Si wafer to achieve a buried SiO\(_2\) layer under a thin layer of high quality silicon.

A screenprinted, interdigitated cell with an efficiency of 16\% was produced by Mitsubishi using the VEST process. For a stand-alone silicon wafer, screenprinting requires a minimum thickness of 80\( \mu \)m.

Interdigitated, screen-printed cells on Cz wafers have been produced at BP Solar [260].
Processing included texturing, a heavy phosphorus diffusion, SiN deposition, laser cutting of isolation trenches, surface damage removal, removal of the SiN to expose the emitter, screen-printing of contacts and firing. Ag/Al was used for the p-type contacts to form a p-type region under the contacts after firing. Cell performance was dominated by series resistance due to lateral current flow in the base and recombination at the p-type contacts. The cells had an efficiency of 6.3% when illuminated from the contacted surface and 1% when illuminated from the front, non-contacted surface. Additional losses when the cell was illuminated from the front came from recombination in the bulk and at the non-contacted surface. Limitations on the contact geometry imposed by the screen-printing process contributed to the low efficiency.

### 2.8.4 Multilayer Cells

Diffusion lengths and grain sizes of silicon deposited on foreign substrates tend to be small. The multilayer cell design, shown in figure 2.10, has been developed at UNSW in order to improve the efficiency potential of poor quality material [102, 127, 128, 344, 362]. The design consists of multiple n-type and p-type layers with layers of the same polarity connected in parallel. One advantage of the multilayer cell is that the layer structure can be designed so that every point in the device is within a diffusion length of a collecting junction, independent of the device thickness. The multilayer structure is also designed to reduce the impact of grain boundaries by reducing the part of the device volume that is closer to a grain boundary than a junction. EBIC studies on layers fabricated on multicrystalline substrates have shown that the multilayer structure restricts low collection regions to the immediate vicinity of the grain boundary [128]. The main disadvantage is that junction recombination was increased, which reduces both FF and $V_{oc}$. Another
potential problem is that the number of junctions intersected by grain boundaries was larger (approximately proportional to the number of layers).

**Results for Multilayer Cells**

An efficiency of 17.6% has been achieved at UNSW with a 32μm thick, 6 layer structure deposited by CVD onto a heavily doped silicon substrate [362]. The two uppermost n-type layers were connected in parallel via texturing. All other layers except the bottom p-type layer were floating, in contrast to the original design that had layers of each polarity connected together. Floating junctions need to be forward biased by illumination to allow current to pass. One-sun illumination is sufficient to provide this forward bias. An efficiency of 12% was achieved for a multijunction cell with 5 layers connected in parallel, grown by CVD on a heavily doped substrate [176]. Experimental devices fabricated so far have used good quality material, thereby avoiding any problems with junction recombination.

**Modelling of Multilayer Cells**

The simulation package Dessis and a 1D analytical model have been used to predict the performance of multilayer cells [102]. The performance of the device was found to be fairly insensitive to surface recombination velocity, and junction recombination was dominant. Trap-assisted tunnelling made an important contribution to junction recombination in heavily defected material. The calculated severity of the effect of trap-assisted tunnelling was found to depend on the model used (Hurkx [155] or Schenk [271]). An efficiency of 12.6% was predicted with a 1D model and Hurkx tunnelling compared with an efficiency of 14.9% for a 2D model with Schenk tunnelling. Efficiencies of 12–15% were predicted for 10μm thick cells with a Lambertian light-trapping scheme fabricated on silicon with a
lifetime of 10ns.

The relationship between minority carrier lifetime and doping density depends on the deposition technology [300]. Wenham et al. argue that in low-quality multicrystalline silicon, the minority carrier lifetime, and hence diffusion length, can be limited by the grain size and grain boundary recombination velocity, so the doping level can be increased without affecting the minority carrier diffusion lengths [344]. This reduces the dark saturation current since it depends on the minority carrier concentrations. It was calculated that the optimal number of junctions for a 10µm thick device with 10ns lifetime is 10 if Lambertian light-trapping and surface recombination velocities of $2 \times 10^4$ cm/s are assumed.

Several other groups have modelled the multilayer cell design numerically. Stocks et al. [300, 299] found that the multilayer design is more efficient when light trapping is not included, but that in the case of good light trapping, conventional one or two-junction devices are more efficient. The optimal device thickness for poor quality silicon is quite thin (3.3µm for silicon with a lifetime of 10ns and Lambertian light trapping), so the degree of light trapping strongly affects cell performance. It was also determined that it is important to optimise the device thickness for each choice of the number of junctions. If the device thickness is fixed at a value higher than the diffusion length, as was done in the UNSW analysis, then the efficiency potential of a single junction device will be underestimated. This is important because the device thickness is a free parameter with most deposition technologies.

The relationship between minority carrier lifetime and doping density is dependent on deposition technology and is not known for most technologies, so cases where the lifetime was dependent and independent of doping were considered by Stocks et al.. Dopant densities were optimised within the range $10^{16}$–$10^{19}$ cm$^{-3}$, and in all cases perfect surface passivation was assumed. In the case where lifetime was assumed to be independent of doping, modelled multilayer cells demonstrated efficiencies 2% (absolute) better than single junction cells when light trapping was not incorporated. For devices with Lambertian light trapping, a two junction device was found to be most efficient for poor quality material. For these parameters, efficiencies of cells with one to five junctions were found to vary by less than 0.5% absolute. In the case where lifetime varied with doping, multilayer cells had an efficiency advantage of 1% absolute if light trapping was not included. When Lambertian light trapping was incorporated, the optimal number of junctions was found to be one.

Incorporation of thin (10–30nm) intrinsic layers in the junction region between heavily doped layers to reduce trap-assisted tunnelling and hence junction recombination has been discussed by Green [127]. Insertion of intrinsic layers also prevents bandgap narrowing
from enhancing depletion region recombination and could enhance effective carrier lifetimes in the depletion regions. It was claimed that, for a multilayer doping level of $5 \times 10^{18} \text{cm}^{-3}$, these effects reduce achievable junction recombination by a factor of $2 \times 10^4$ compared to that obtained by Stocks et al. [300]. The average dopant spacing in material doped at $5 \times 10^{18} \text{cm}^{-3}$ is 6nm. A quantum mechanical rather than classical band structure treatment is probably required to properly analyse the effect of the insertion of 10 to 30 nm thick undoped layers. There would be considerable technological difficulties, especially for low cost deposition.

A semi-analytical 1D model and a 2D numerical model were used by Goldbach et al. to optimise the multilayer structure with respect to number of junctions [124]. An optimum number of junctions greater than two was found for a wide range of minority carrier lifetimes, but the thickness of the devices was fixed rather than being optimised independently of the number of junctions. Optimisation of contact spacing, doping and thickness of the first two layers were performed for a 3 junction, 12$\mu$m thick cell. Efficiencies of 14% and 10% were predicted for structures optimised within these constraints and with minority carrier lifetimes of 100ns and 10ns respectively.

An Ebers-Moll model for the multilayer structure has been used to predict an efficiency of 10.8% for an 4-layer structure, optimised with respect to layer thicknesses and doping, with a SRH minority carrier lifetime of 100ns [67].

Modelling of single and multijunction cells with the encapsulated-V light trapping structure has been performed in a collaboration between University of Bayreuth and Max-Planck-Institut für Festkörperforschung [253]. Multijunctions were found to improve the performance by about 3% absolute where the surface recombination velocities are high ($10^5 \text{cm/s}$) but to be of marginal benefit if the surface recombination velocities are less than $10^4 \text{cm/s}$. Low surface recombination velocities ($<10^4 \text{cm/s}$) are required to achieve reasonable cell efficiencies.

The Emitter-Wrap-Through Cell Design

In the emitter-wrap-through (EWT) cell design, light-generated electrons collected at the front are transported by holes (or pipes) in the cell to the metal contacts at the rear of the cell, reducing front shading losses [95, 121]. Other advantages of the EWT design are low grid resistance and simplified module assembly since cell interconnection can also be performed entirely from the rear. The double-junction EWT cell collects carriers from both surfaces and is equivalent to a two-junction multilayer cell. If n-type surfaces are used then there is a potential for higher voltages than for a conventional design with a p-type surface, because n-type surfaces are more easily passivated than p-type. For a series resistance of
0.25Ωcm² and a cell area of 100cm², maximum achievable efficiencies of 21% and 18% for Cz and mc-Si material, respectively were modelled with PC1D (assuming respective lifetimes of 30μs and 15μs) [121]. A performance enhancement of nearly 1% absolute was predicted compared to the front-junction cell. Efforts to date have focussed on wafer-based, rather than thin-film, designs. The EWT cell design has obvious applications with the epilift and VEST processes, which result in thin silicon structures with a grid of holes as a natural part of each process.

### 2.8.5 Drift Field Cells

A doping gradient resulting in an electric (drift) field can be incorporated in the base of solar cells to attract minority carriers toward the pn-junction. This enhances the effective diffusion length of the minority carriers. The maximum difference in doping concentration between the front and the rear of the base that can be achieved depends on the deposition technology. Larger drift fields can be achieved in thin layers than thicker layers. Some deposition technologies lend themselves to producing doping gradients. With LPE, the change in distribution coefficient of the dopant atoms with temperature means that doping gradients tend to be a natural consequence of the growth process.

A collaboration between UNSW, Pacific Solar and Max-Planck-Institut für Festkörperforschung has produced 16.4% efficient, 4cm² drift field cells by LPE on p⁺⁺ sc-Si substrates [367, 368]. The layer thickness was 20–32μm and the doping varied from $2 \times 10^{16}$cm⁻³ at the front of the base to $2 \times 10^{17}$cm⁻³ at the rear. An In/Ga melt and an Ar/4% H₂ ambient were used. A high efficiency cell process was applied that included two phosphorus diffusions, micro-grooving and a double layer anti-reflection coating (DLARC). The junction between the epilayers and the heavily doped substrates created a strong back surface field that reduced back surface recombination velocity and dark saturation current.

Although it is generally agreed that drift fields enhance effective minority carrier diffusion lengths, questions have been raised by Weber et al. as to whether this translates into significant improvements in cell performance [340]. PC1D was used to model drift field solar cells, assuming an exponential doping profile in the base region (typical of that obtained with LPE). The reflectivity of the rear surface, surface recombination velocity and minority carrier lifetimes were varied over wide ranges in order to determine those regimes in which drift fields would enhance cell performance. Cell thickness was optimised in each case. The general conclusion was that drift fields would only be marginally useful at best, and only in a limited number of cases.

It was found that for a moderately passivated, highly reflective rear surface (ie. excellent light trapping) with a BSF, the benefits of incorporating a drift field are negligible.
For a high recombination velocity and high reflectivity rear surface, efficiency improvements of up to 0.4% (absolute) are obtained for drift field cells but variations in dopant density in the base of up to two orders of magnitude are required to obtain this improvement. For cells with no light trapping (e.g., cells fabricated on an epitaxial layer grown on a silicon substrate) an efficiency advantage of 0.8% was predicted for drift field cells, but again variations of dopant density of two orders of magnitude are required. The modelling showed that a significant enhancement of \( I_{\text{cell}} \) caused by a drift field does not necessarily indicate a significant enhancement of efficiency. It was concluded that the benefits of a base drift field are fairly small.

In-situ dopant profiles may be useful, as a replacement for a rear diffusion or back surface passivation, thereby reducing the number of steps required for cell fabrication.

2.8.6 Monolithic Integration

In a conventional module, wafers are connected in series by soldered tabs that connect the back of one wafer to the front of the next. Many groups are seeking to eliminate this labour-intensive step by using a monolithically integrated structure in which the interconnection is integrated within the silicon layer. This type of design should be inherently more reliable. The higher voltage and lower current help reduce series resistance losses. Most of the work to date has focussed on process or design development and optimisation rather than cost reduction.

A mini-module produced at Fraunhofer ISE consisting of 12 cells each of area 1cm\(^2\) monolithically integrated on a SOI wafer had an efficiency of 17.1% [123]. Cell isolation was achieved by laser-grooving down to the SiO\(_2\) layer.

A 36 segment monolithically interconnected device with an area of 321cm\(^2\) and an efficiency of 9.8% was fabricated at Astropower [116]. The supporting tape-cast ceramic provided light trapping via pigmentation and random texturing. The effective reflectance of the silicon/ceramic interface was about 60%.

Astropower have investigated electrostatic bonding, which allows silicon wafers to be attached to glass and processed to form monolithically interconnected devices [286]. The silicon layer is thermally oxidised to provide front surface passivation and then bonded to glass and thinned to 30\(\mu\)m. Electrical isolation of the unit cells is achieved by V-grooves that are etched completely through the silicon. A wrap-around emitter is formed by rapid thermal diffusion after bonding, thinning and V-groove formation, so a high temperature glass superstrate is required. Re-interconnection is provided by forming ohmic contacts on the (oppositely-doped) sides of the V-grooves or the back surface of the device. Rear random pyramids, an oxide for rear surface passivation and a reflector are then applied.
Predicted losses due to shading and series resistance are less than 5%. A 28μm thick device had an efficiency of 11.1% with a $V_{oc}$ of 5.5V and an area of 3.12cm$^2$. Another device, 27μm thick, had an effective minority carrier diffusion length of 195μm.

A monolithically interconnected structure has been fabricated at Electrotechnical Laboratory on SOI wafers with a 3μm thick silicon layer [305]. Cell isolation was achieved with diffused n++ regions and series connection was obtained via adjacent p++ regions, as shown in figure 2.11. Because the n++ regions are diffused through to the underlying SiO$_2$ layer, the cell thickness is limited to several microns. The base electrode is at one end of the cell and the emitter is at the other end, so unit cells are long and narrow. The structures have a unit cell width of 200μm. If the doping of the n++ and p++ regions is high enough, a tunnel junction is formed and metal interconnections are not necessary. With cells fabricated to date, metal interconnection was used to ensure series resistance was sufficiently low. The size of the interconnection region was reduced compared with mechanical isolation and re-interconnection, so shading losses were reduced. An open circuit voltage of 10.65V was achieved using 20 unit cells interconnected on an area of 0.4cm$^2$. The fill factor decreased with increasing number of unit cells due to series resistance loss in the emitter, base and interconnection regions, and shunt resistance loss in the interconnection region. Efficiencies were 6.2%, 5.4% and 4.8% for 1, 5 and 20 unit cells respectively. This p-n tunnel junction integrated structure has been simulated in 2D using Medici [304]. It was found that the optimum width of the unit cell is about 200μm. Because the cell is very thin, surface passivation is very important with this structure. The cell performance is affected more by $S_{rear}$ than $S_{front}$ (because the emitter reduces the effect of the front surface recombination velocity) and $S_{rear} < 10^3$cm/s is necessary for high efficiencies. Series resistance at the p-n tunnel junctions needs to be small and a maximum series resistance across one tunnel junction of about 1Ωcm$^2$ was found to be necessary to avoid significant loss in efficiency.

Brendel and Oelting have demonstrated a process to produce monolithically interconnected cells by epitaxy through shadow masks [72]. Stretched wires are used to mask epitaxy by ion-assisted deposition. Epitaxial p+, p and n+ layers are deposited sequentially, and the mask is moved after deposition of each layer so that p+ region of one cell and the n+ region of the next cell are connected.

A method of interconnection based on n-type and p-type conductive pipes in thin silicon on dielectric-coated segmented metal has been proposed by Thorp [311]. Possible ways of producing the structure are proposed, including depositing multilayer structures on glass or opaque materials. The process can also be applied to wafer-based cells.

Monolithic interconnection schemes introduce concerns about the impact that failed
or mismatched cells will have on module performance since the individual devices are not tested and sorted. These concerns can be addressed by bypassing failed or shaded cells via reverse bias breakdown of the pn-junction [101]. A cell with a small reverse breakdown voltage causes a small loss in a series connected cell string if the cell current is reduced (by shading for example). The reverse breakdown acts like a bypass diode. A design that incorporates automatic series interconnection of multilayer cells using the buried contact scheme by doping one side of each contact groove p-type and the other n-type has been proposed at UNSW. Breakdown between the heavy contact doping and the edge of the active layer/s (the contact junction) appears more promising than breakdown of the active junction as there may be little scope for optimising the breakdown characteristics of the active junction without severely degrading the forward bias characteristics. It is argued that Zener breakdown is the most promising breakdown mechanism and modelling indicates that Zener contact junction breakdown voltages of 2V can be achieved. The contact junction can be optimised for reverse bias breakdown almost independently of the forward characteristics of the device. Extra (redundant) cells can be included in each module to increase yield. Modules with low reverse bias breakdown should exhibit greater tolerance to shading than conventional modules.

### 2.9 Light Trapping

Light trapping is especially pertinent for silicon cells due to the low absorption constant in the infra red region. As cell thickness decreases, the maximum attainable $J_{sc}$ drops
Light trapping sharply and the improvement that may be attained with a Lambertian surface (a surface that reflects light with uniform brightness in all directions), compared with a polished surface, increases substantially \[81\]. Hence light trapping is vital to achieve high efficiencies for thin-film cells. Fortunately, the nature of most thin-film depositions is such that the surface is far from optically flat and some degree of light trapping is inherent. In many instances, additional measures may be taken but light trapping schemes developed for conventional silicon solar cells are not always applicable to thin cells. In particular, direct texturing of a thin-film may be too damaging \[312\]. For thin-film silicon on foreign substrates or cheap silicon substrates, the crystallographic orientation is often random. In this case, anisotropic etching may be too unreliable and photolithography too expensive \[312\]. Similarly, texturing of a silicon substrate is undesirable as it may lead to an increased number of nucleation sites and therefore a lower quality material \[312\].

Alternative techniques developed for thin-film light trapping schemes include a textured substrate or deposition of a textured layer onto a substrate prior to growth of a thin-film layer. Thorp has claimed that for thin-films, antireflection properties may be as important as light trapping properties \[312\]. Antireflection coatings (ARC) that are applicable to thick cells are also applicable to thin-film cells and are not discussed in detail. Schmidt et al. have demonstrated the use of PECVD SiN\(_x\) films, for both passivation and as an ARC on the QMS material produced at the University of Stuttgart. A \(J_{sc}\) value of 26.6mA/cm\(^2\) was demonstrated on a non-textured cell and 32.0mA/cm\(^2\) on a cell textured with random pyramids and with a SiN\(_x\) layer \[276\].

Figure 2.12 is adapted from Campbell and Green \[81\] and shows the improvement in \(J_{sc}\) that may be obtained using Lambertian, rather than polished, surfaces and the maximum attainable \(J_{sc}\), both as a function of cell thickness. Cell thicknesses may not be simply read from this graph for cells deposited on textured substrates, as the effective width and the thickness of the deposited layer will not be equal.

Light trapping achievements are usually measured in terms of improvement in the short circuit current. \(J_{sc}\) is also affected by surface recombination and minority carrier lifetime. Light trapping is related to the extra absorption achieved due to the light trapping structure. This is dependent on surface texturing and internal reflectivity of the front and back surfaces \[249\].

An issue that has arisen when considering light trapping in thin-film cells is the relationship between texture period and cell thickness. For conventional cells, the texture period has always been much less than the thickness \[70\]. Textured substrates and thin-films allow the effect of a texture period much greater than the thickness to be investigated \[313\]. A texture period in the range of microns is necessary to investigate the effect
of having a texture period in the same order of magnitude as the film thickness, this has been demonstrated with the sol gel coating developed by several groups based in Germany and is discussed in section 2.9.3.

### 2.9.1 Textured Silicon Surface

Deposition of silicon onto foreign substrates often results in a naturally occurring surface texture and Kaneka have used this to advantage in the STAR cells (naturally surface texture and enhanced back reflector) [228, 352]. The surface texture of STAR cells is controlled primarily by the deposition temperature but also by deposition rate, the ELA (excimer laser anneal) conditions and the surface treatment of the laser annealed poly-Si [228, 352]. STAR cells have demonstrated a very high J<sub>sc</sub>.

### 2.9.2 Textured Substrates

An alternative to direct texturing of a silicon film is to texture the substrate. This is being investigated by a number of groups. The simplest textured surfaces are two dimensional grooves, although three dimensional texturing is more effective. Another possibility is random texturing.

Two dimensional texturing to date has used conformal grooves. In addition to the light trapping properties, conformal grooves lead to an increased surface area, which may allow
for better heat transfer. A disadvantage of conformal grooves is that the increased cell volume leads to increased recombination and therefore to losses in $V_{oc}$ [253]. This is also the case for three dimensional texturing. Most modelling results have predicted values for $J_{sc}$ of around 35mA/cm$^2$ for cell thicknesses of about 5$\mu$m when using a V-grooved substrate.

Encapsulated-V texturing has been demonstrated and modelled at the Max-Planck-Institut für Festkörperforschung. The encapsulated-V texture was formed by mechanically texturing a glass surface with V shaped grooves. Silicon was then deposited by ion-assisted deposition. The substrate temperature was 610–650°C. A detached back surface reflector (BSR) was used together with shallow groove angles corresponding to a texture period of 500$\mu$m on the glass. Having the BSR detached decreased the number of reflections and therefore light absorption in the BSR. An additional advantage of this BSR is that it is made from aluminium and so may provide series connection [74].

Three dimensional texturing of foreign substrates may be realised by imprintation of ceramic substrates while in powder form and by embossing micron sized features in glass substrates [313].

A pyramidal film texture has been developed by groups at Max-Planck-Institut für Festkörperforschung and the Universität Erlangen. Theoretical predictions are for a $J_{sc}$ of 37mA/cm$^2$, assuming a thickness of 4$\mu$m, a texture period of 15$\mu$m and a facet angle of 75°. A texture period of 500$\mu$m is more in line with what is achievable today and results in a $J_{sc}$ of 34mA/cm$^2$. Facet angles between 0 and 80° were modelled and cell performance was found to increase with increasing facet angle [44].

Foreign substrates may lend themselves more readily to random texturing than to regular texturing. A randomly textured substrate allows the Lambertian limit to be approached.

Surface scattering is said to be responsible for the efficiency of 7% and $J_{sc}$ of more than 25mA/cm$^2$ on the $\mu$-cSi:H cells deposited on glass substrates at the Academy of Sciences of the Czech Republic and the Universite de Neuchatel [247].

### 2.9.3 Substrate Coatings

Max-Planck-Institut für Festkörperforschung, the Institut für Neue Materialien and the Universität Stuttgart have collaborated to investigate the possibility of using a sol-gel coating on a glass substrate. The sol is made from tetraethoxysilan, trimethoxysilan and silica sol using a hydrochloric acid catalyst. It sets to form a gel film. The aim is to provide surface texturing that has a period in the same order of magnitude as the film thickness [70]. Theoretical modelling has been used to determine the relative advantages
of 4 different features; encapsulated-V texture with a V-grooved glass substrate, tripyramidal film, square pyramidal film and hexapyramidal film. All features have advantages of large facet angles, which reduces reflectance. The BSR is detached from the silicon layer to reduce reflections. Both the air/glass and glass/silicon interfaces are without antireflection coatings. The modelled thickness was 4μm and each cell included a SiO₂ layer for surface passivation at the silicon/air interface. (SiO₂ also provides some antireflection properties) [70].

With the V-texture, the average path length was found to be 12 times \(W_{\text{eff}}\). With the other textures, the \(J_{sc}\) was found to be larger and an average path length of 49 times \(W_{\text{eff}}\) was obtained [70]. The efficiency of thin cells was found to be current, rather than voltage controlled and texturing could almost double the current. The theoretical maximum value for \(J_{sc}\) was 40mA/cm², which was achieved with a thickness of 4μm, a facet angle of 75 degrees and period of 15μm. The front glass surface was textured (grooves).

Preliminary sol gel textured surfaces have been prepared. Facet angles were 40° at ridges, decreasing to 0° at the base of the pyramids. The embossing process has not yet been optimised and initial films did not hold their shape. Sol gel substrates will require a deposition temperature of less than 500°C to prevent decomposition of the film.

Other substrate coatings that have been investigated include ZnO on glass or stainless steel and a diffraction grating. ZnO may be applied using magnetron sputtering. The deposited layer can then be chemically etched [114, 322]. Sony are investigating the use of a diffraction grating on both the rear and front surface of a cell [212].

### 2.9.4 Porous Silicon

Porous silicon may be useful for light trapping of thin-film cells, having the ability to diffuse light well [294], although the electrical transport properties are not yet fully understood [293]. Porous silicon is formed using electrochemical anodisation [294] and the porosity level controlled by varying the current density. The process is usually quick, but requires handling of single wafers [316]. The refractive index of silicon decreases with increasing porosity [360, 361], and varies from 1.7–2.1 [289]. The large surface area of porous silicon means that good surface passivation techniques will be necessary [294]. The fact that porous silicon absorbs a fair amount of light will need to be addressed [289]. The structure of porous silicon is sensitive to high temperatures such that any further processing steps may need to be done at lower temperatures [294]. The reliability of porous silicon over time also needs to be investigated [289].

At IMEC, the use of porous silicon as a diffuse backside reflector has been investigated [294]. Epitaxial layers of 2–3μm have been grown on porous silicon layers of about
350nm. The resulting layers were of lower reflectance but highly defected, and consequently a low quality material [294]. Using CVD at 1050°C or 1130°C to deposit on porous silicon material, an efficiency of 12.1% was obtained on sc-Si and 10% on 10×10cm² mc-Si. Both substrates were heavily doped [54].

The use of a porous silicon multilayer for a backside reflector (BSR) has been investigated at the University of Erlangen [360, 361]. A highly doped substrate was used, and a porous layer formed on this by anodic etching. A thin-film silicon layer was then grown on the porous silicon layer. Advantages of the process are that it is simple, fast and compatible with standard cell processing. It is also conceivable to combine light trapping with back surface passivation if the porous silicon layer has a thin p⁺ layer grown into it. A challenge for the group is to grow epitaxially on the porous silicon and still maintain the reflectance capabilities of the porous silicon. Maximum reflectance occurs if a large number of porous layers are stacked. Bragg reflectors are formed by stacking layers with alternating porosity such that $nd = \lambda/4$ [360]. At present, 20 layers are used with porosities alternating between 0.4 and 0.6 and layer thicknesses of 125nm and 100nm respectively [360]. A cell was made such that porous silicon covered one half of the surface. An epitaxial layer was grown on both the porous silicon layer and on the bare silicon area. The epitaxial layer was a 3µm thick p-type silicon layer deposited by CVD at 1000°C. The result was an increase in EQE for all wavelengths in the range 350–1000nm, but it is possible that sintering of the porous silicon layer caused an increase in epilayer thickness. The reflectance was enhanced in the 900–1100nm range [361]. The value of $J_{sc}$ was 9mA/cm² and 12.5mA/cm² for layers grown on bare silicon and on porous silicon respectively. No ARC was used [360].

2.10 Cost

Important issues for commercialisation of PV technologies are low manufacturing cost and that the technology is manufacturable with the potential for high yields and throughput. Process complexity and the need for specialised equipment should be minimised. Thinner layers and simpler processes have the potential for higher throughput. The use of hazardous materials must be minimised for cost, environmental and health and safety reasons.

A factory designed to produce 10MW of PV in a year needs to produce about 1 module/minute [278]. If deposition times preclude a continuous process, a batch process can be used, but with generally higher capital costs. If multiple chambers are used, downtime in a batch process can be reduced in comparison to a continuous process because of
the ability to service one chamber while the others are kept in-line.

Competition for thin crystalline silicon films also comes from improvements to bulk processing methods. The mechanical yield of thin cells produced by slicing has been investigated at Siemens Solar [223]. Mechanical yield loss of the various process steps was analysed for different cell thicknesses. Lower yields for 100μm and 125μm thick wafers were attributed to lower levels of experience and training of operators in fabrication of thin cells rather than the reduced mechanical stability of the wafers. Both ribbon growth and the lift-off techniques potentially produce stand alone thin-film silicon wafers that must be processed into cells. They will require more sensitive handling techniques than thicker wafers. Work by Bruton et al. has looked at industrially applicable processing of thin Cz wafers. An initial mechanical yield of 85% was achieved for 140μm thick wafers and 100cm² cells with efficiencies of ~ 17%. It is envisaged that later yield statistics will be comparable to those of thick silicon [80].

Development of thin crystalline silicon technologies is still mostly at the laboratory scale. In 2001 market share of solar cells was 34.6% single-crystal, 50.2% polycrystalline, 5.6% ribbon and 8.9% amorphous silicon [273].

2.10.1 Importance of Efficiency

The importance of increased efficiency versus lowered cost of panels has been considered by Kiess and Toggweiler [181]. In an idealised calculation it was found that that the cost per kWp is inversely proportional to the efficiency of the cells. This suggests that it is beneficial to increase efficiency unless the fabrication or area-related costs increase more than linearly with efficiency. Factors such as these are technology dependent, so the optimum cell and panel size will depend on the manufacturing technology used. Using projected high volume manufacturing costs for today’s technologies, it is predicted that cells with efficiencies in the range 12% to 18% will result in the lowest energy price. These technologies include CIS, CdTe, mc-Si and screenprinted and laser-grooved Cz Si cells. Balance of system (BOS) costs would need to be reduced by a factor of two to make cells of lower efficiencies competitive.

A goal for PV system prices that will make it attractive to investors (rate of return 10% after tax) of US$1.5/W (including BOS costs) has been calculated [373]. This was based on electricity costs of 6c/kWh. Currently BOS costs are about $2–$3/Wp, which is equivalent to about $250/m². In order to reach this long term goal, module efficiency needs to be about 15% to keep BOS costs down, even assuming significant reductions in future BOS costs. In order to reach a module efficiency in production of 15%, laboratory cells will need to reach efficiencies of about 19%, because of losses due to non-uniformities
and the fact that production efficiencies are average, not best, efficiencies. High yields and good material use will be necessary.

Increased reliability of power conditioning systems and BOS components is required to increase the lifetime of PV systems to 30 years [99]. In a 1990 study into performance of modules after 10 years in the field, 98% of non-producing modules were the result of BOS problems. Because mature technologies are involved, the only way to achieve the desired reliability for BOS components is to use higher quality, more expensive components. The area dependence of some BOS costs will increase the trend towards higher efficiency modules. The costs of making PV systems more reliable may mean that installed PV system costs decrease more slowly than expected. The life-cycle costs of PV energy will decrease if system lifetime increases.
Review of Thin-Film Silicon Solar Cells
This chapter discusses liquid phase epitaxy in relation to thin film silicon layers, produced with the epilift technique, that can be used to make solar cells. Firstly, the morphology resulting from different seeding patterns, the transfer of dislocations to the epitaxial layer and the lifetime of layers grown using oxide compared with carbonised photoresist barrier layers is discussed. The second half of this chapter discusses the boron doping of epitaxial layers. Simultaneous layer growth and boron doping was demonstrated, and used to produce a 35μm thick layer with a back surface field approximately 3.5μm thick.

3.1 Introduction: The Epilift Technique

The epilift technique was developed by Weber and Blakers [337]. It is a method for producing thin-film silicon layers that can be processed into solar cells. A high quality, single crystalline wafer is used as a reusable substrate. As discussed in chapter 2, approximately 40% of the cost of a finished solar module is due to the silicon, and hence thin-film silicon solar cells have a potential cost advantage over conventional silicon solar cells.

The epilift technique involves substrate preparation, layer growth, layer separation and cell fabrication. Cell fabrication may be done before or after the epitaxial layer is separated from the substrate. Figure 3.1 shows a schematic of the epilift process.

The substrates used for the epilift technique are single-crystalline and typically (100) orientated. A thermal oxide is grown on the substrates and this is patterned with a grid. The grid lines are 2–10μm wide and typically spaced 50–100μm apart. The patterned substrate is shown in part a) of figure 3.1.

Layer growth is done using liquid phase epitaxy (LPE) in a hydrogen ambient with the tipping boat mechanism [197]. Part b) of figure 3.1 shows the epitaxial layer growth on the substrate. Layer growth requires a substrate wafer, source wafer and metal melt.
Figure 3.1: Schematic of the epilift process. Part a) shows substrate preparation, where a thermal oxide is grown on the substrate and patterned with a grid. Part b) shows layer growth, where liquid phase epitaxy is used to grow the epitaxial layer on the substrate. Growth only occurs on the exposed silicon and assumes the crystallographic structure of the substrate. Part c) shows layer detachment, where a chemical etchant or mechanical means is used to separate the epilayer from the substrate. The substrate must be cleaned and the oxide grid re-formed before it can be reused.
3.1 Introduction: The Epilift Technique

There are three stages of growth, as shown in figure 3.2. Firstly, the furnace is heated to the temperature at which growth will begin (typically 970°C). At this point the melt is liquid. Secondly, the furnace is rotated so that the melt lies on the source wafer. Silicon dissolves from the source into the melt to the solubility limit at that temperature.

Thirdly, the furnace is rotated, so that the melt lies on top of the substrate wafer, and cooled. A typical cooling rate is 2°C/minute. The silicon solubility in the melt decreases with decreasing temperature and silicon therefore precipitates onto the exposed regions of the substrate. The solubility of silicon in indium and tin at 800 and 1000°C is shown in table 3.1. The epitaxial layer grows only on the exposed silicon. This is a property of the LPE process, resulting from the fact that growth occurs close to thermal equilibrium. The epilayer then overgrows the mask laterally. The resultant layer assumes the crystallographic orientation of the substrate and is therefore single crystalline. In the case of growth on a (100) orientated wafer with grid lines aligned in the (110) directions, the grown layer has a diamond shaped cross section, which is advantageous for light trapping. Figure 3.3 shows a scanning electron micrograph of an epilayer attached to a substrate. The temperature range over which growth occurs and the cooling rate can be adjusted to achieve the desired layer coverage.

Substrate and source wafers are given an RCA clean and dipped in an HF solution before loading into the furnace. The clean is necessary to remove any contaminants that may compromise the electronic quality of the grown layer and to remove dust particles from the surface, as these can introduce dislocations [341]. The HF dip is necessary to
remove the thin oxide that forms during an RCA clean, since growth will not occur on an oxide-covered surface. For the same reason, growth is aided by the hydrogen ambient. The hydrogen aids in the removal of thin layers of oxide that can form after exposure to air or due to trace amounts of oxygen or water vapour in the system [343]. After epitaxial layer growth, any melt remaining on the wafer is removed in a boiling aqua regia etch (3:1 HCl:HNO₃).

The last stage of the epilift process follows one of two paths; either a cell is fabricated and then the layer is detached or the layer is detached and a then cell is fabricated. If cell fabrication is done first, the layer may be partly detached prior to cell fabrication using an electrochemical etchant, in which case final layer separation is done mechanically. If cell fabrication is done after layer detachment, the layer may be detached using either an electrochemical etchant or a mechanical process. Part c) of figure 3.1 shows the epitaxial layer detached from the substrate. The substrate must be cleaned and re-patterned before reuse.

**Table 3.1:** Silicon solubility in indium and in tin at 800 and 1000°C.

<table>
<thead>
<tr>
<th>Melt</th>
<th>Silicon solubility (atomic %)</th>
<th>at 1000°C</th>
<th>at 800°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>In</td>
<td>1.9</td>
<td>0.38</td>
<td></td>
</tr>
<tr>
<td>Sn</td>
<td>2.5</td>
<td>0.62</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 3.3:** A scanning electron micrograph of an epilayer attached to a substrate. The diamond cross section of the layer is visible. (From Catchpole *et al.* [83].)
3.2 Epitaxial Layer Morphology

Incorporation of individual silicon atoms into a growing layer occurs at ‘face’, ‘step’ or ‘kink’ sites where the incoming atom binds to 1, 2 or 3 atoms, respectively. Growth is favoured at sites where a greater number of bonds are formed. On an atomic scale, with a fast cooling rate the morphology of a finished layer is determined by the availability of growth sites and the local supersaturation of the melt at the epilayer/melt interface [339]. With a slow cooling rate, the morphology is also influenced by free energy considerations, the silicon atoms will rearrange so as to minimise the free energy of the epitaxial layer. On a large scale, morphology is influenced by the crystallographic orientation of the substrate wafer, the cooling rate during growth, the temperature range over which growth occurs and the pattern on the oxide.

In the case of epilift solar cells, the layer morphology is important as it determines the thickness and hole fraction of the final layer. An important requirement is that the morphology is reproducible. The optimum hole fraction will depend on the detachment method and cell fabrication process, for example, a selective etchant detachment method may require larger holes to ensure a continuous supply of solution to the attachment region. With a greater hole fraction, a rear reflector becomes increasingly important. The optimum layer thickness will depend on the minority carrier diffusion length and the thickness necessary for structural stability during layer detachment and cell fabrication.

On a (100) orientated substrate with grid lines aligned along the (110) directions, growth at the intersections of the lines is different to growth far from these points. At the line intersections there is a plentiful supply of atomic steps and growth is limited by the supply of silicon from the solution. Far from the intersections, growth is limited by the supply of atomic steps on the (111) orientated surfaces [339]. Weber et al. found that higher cooling rates led to less selective growth at the intersections and therefore to layers of more uniform thickness.

In this section, the morphology resulting from square grids with different seeding line widths and layers grown using different cooling rates has been studied. Following this, the effect of varying seeding line width and cooling rate for lines aligned at 60° has been studied.

3.2.1 Experimental Procedure

The substrates used for this work were Cz, 0.015Ωcm and (100) orientated. Layer growth was done using the tipping boat method, described in section 3.1, and an indium melt of six nines purity. Three growths were done, each from 970–870°C, using cooling rates
of 0.3, 1 and 3 °C/minute. Each substrate wafer was patterned using an oxide mask that had eight different grid patterns. Five of the grids were square with seeding lines spaced 40 μm apart and 1–20 μm wide. The remaining three grids had seeding lines angled at 60°, spaced 80 μm apart and between 2–10 μm wide. Table 3.2 shows a summary of the grid patterns used for this section of work. The morphology of the finished layers was viewed using a scanning electron microscope (SEM). Limitations of the photolithography resolution meant that the seeding line width resulting from the 1 μm wide mask lines was closer to 2 μm.

### 3.2.2 Results and Discussions

#### Square Grid

Figure 3.4 shows SEM images of the epilayers grown using a square oxide grid with 5 μm wide seeding lines and a cooling rate of a) 0.3 °C/minute, b) 1 °C/minute and c) 3 °C/minute. With the lower cooling rates the layer was thicker and the holes were smaller. The growth was slightly non-symmetrical about the line intersections for the cooling rate of 0.3 °C/minute.

The lower wafer coverage and decreased epilayer thickness with increased cooling rate indicates a reduction in total silicon deposition. Silicon deposition is reduced with increased cooling rate due to two factors. Firstly, when the final temperature is reached, the growth is stopped immediately. The melt will not have time to reach thermal equilibrium and can be supersaturated. Therefore, with a higher deposition rate, more silicon remains in the melt and less is deposited. Secondly, for silicon deposition with the LPE method, it is possible for silicon crystallites to form in the melt. These then become alternate growth sites for silicon atoms in the melt and silicon deposition onto the substrate is reduced. With higher cooling rates, crystallite formation happens more readily as the silicon atoms
Figure 3.4: Scanning electron micrographs of epitaxial layers grown using a square oxide grid with 5μm wide seeding lines and a cooling rate of a) 0.3°C/minute, b) 1°C/minute and c) 3°C/minute.
have less time to diffuse to the growing surface and the top layer of the melt more quickly reaches a critical degree of supersaturation where spontaneous nucleation occurs.

Figure 3.5 shows epitaxial layers grown using a square oxide grid and a cooling rate of 1°C/minute. Seeding lines were a) 2μm wide, b) 5μm wide and c) 10μm wide. For all the images shown in figure 3.6, layer growth was thicker at the grid intersections. This effect is discussed by Weber and Catchpole [339] and is explained qualitatively using free energy considerations. The free energy is lower when there is thicker growth at the seeding line intersections because this minimises the surface area to volume ratio. This effect of free energy minimisation is evident with lower cooling rates because the silicon atoms have time to move into the lowest energy configuration.

Figure 3.6 shows SEM images of the epilayers grown using the same seeding line widths shown in figure 3.5, but with a cooling rate of 3°C/minute. With the faster cooling rate, bunching at the line intersections was less evident. This is because the local super-saturation of the melt at the epilayer-melt interface was higher and epitaxial layer morphology was therefore determined by surface kinetics and the diffusion of silicon in the melt [339]. Near the line intersections, growth was limited by the supply of silicon from the melt, whereas far from the intersections, growth was limited by the supply of atomic steps.

Figure 3.7 shows SEM images for the layers grown using the 1μm wide seeding lines. The first image shows a wafer grown at a cooling rate of 1°C/minute and the second shows a wafer grown at a cooling rate of 0.3°C/minute. With the slower cooling rate a preferential growth direction was established. Even with the faster cooling rate, a slight preferential direction was still visible.

The observation that a preferential growth direction was established with narrower seeding lines is usually explained by constitutional supercooling. As the line width decreases, small differences become more important and can lead to a significant difference in growth rate in the initial stages of growth. For example, slightly wider lines would result in slightly thicker growth. Slight misorientation of the grid can also favour growth in one direction. Once preferential growth has occurred in one region, constitutional supercooling acts to enhance slight variations in layer thickness that are present in the initial stages of growth. Constitutional supercooling describes the effect whereby silicon atoms in the melt diffuse towards the substrate and encounter the thicker regions of the epitaxial layer first. These regions then continue to build up in preference to others. For the results shown in figure 3.7, the cooling rates were very low and, especially in part b), free energy considerations are also important. The free energy is reduced by increased faceting (because the (111) orientated surfaces have a lower energy) and by the dominance of one growth
Figure 3.5: Scanning electron micrographs of epilayers grown using a square oxide grid and a cooling rate of 1°C/minute. Seeding lines were a) 2μm wide, b) 5μm wide and c) 10μm wide.
Figure 3.6: Scanning electron micrographs of epilayers grown using a square oxide grid and a cooling rate of 3°C/minute. Seeding lines were a) 2μm wide, b) 5μm wide and c) 10μm wide.
direction (because this results in a lower surface area to volume ratio and hence a lower free energy).

**Grid Lines Angled at 60°**

Figure 3.8 shows SEM images resulting from layer growths on seeding lines spaced 80µm apart and orientated at 60° to each other. In both cases, the seeding line width was 2µm. The first image is of a layer grown at a cooling rate of 1°C/minute. The (111) growth faces, characteristic of growth on (100) orientated substrates, were clearly visible as was approximately symmetric growth near the line intersections. The second image is of a layer grown at a cooling rate of 0.3°C/minute. Again the (111) growth faces were clearly visible, but growth was highly irregular. This irregularity was probably due to constitutional supercooling enhancing small initial variations in the seeding pattern and in the initial stages of growth.

### 3.3 Dislocations Within the Epitaxial Layer

This section discusses the transfer of dislocations from a substrate to an epitaxial layer. This is significant because discontinuities or dislocations within a crystal lattice are often sites of increased recombination and therefore reduce the electronic quality of the wafer. Dislocation sources for an epitaxial layer are thought to include dust particles and rough oxide edges, in the case of patterned epitaxial layers [341]. In the case of epitaxial layers grown on (100) orientated substrates with grid lines orientated in the (110) direction, the density of dislocations in an epilift layer has been shown to be unrelated to oxide thickness and not to influence the morphology [341].

In epitaxial layers grown on oxide patterned substrates, the dislocation density can be very high, which will lead to low lifetimes in the epitaxial layer. Dislocations are thought to multiply with epitaxial growth due to stresses in the epilayer. In a patterned layer, one source of stresses is the oxide. Banhart *et al.* [28] observed a curvature of the oxide for epitaxial layers grown on a patterned substrate. Raidt *et al.* [248] showed that the curvature of the oxide may be due to either adhesive forces between the silicon and the oxide or to the surface tension of the melt acting to bend the oxide down towards the wafer. Unfortunately, the areas of high dislocation density are seemingly randomly located, making it difficult to find approaches that may avoid or reduce dislocation multiplication. It is possible, for example, that different masking material may lead to less stress in the epitaxial layer and therefore reduce dislocation multiplication. ‘Carbonised’ photoresist (formed by annealing in a forming gas ambient at 1000°C for 30 minutes) has been found,
Figure 3.7: Scanning electron micrographs of epilayers grown using a square oxide grid with 1μm wide seeding lines and a cooling rate of a) 1°C/minute and b) 0.3°C/minute.
Figure 3.8: Scanning electron micrographs of epilayers grown using a grid with lines aligned at 60° to each other. In both cases the grid lines were 2µm wide. The first image is of a layer that was grown at a cooling rate of 1°C/minute and the second image is of a layer that was grown at a cooling rate of 0.3°C/minute.
for example, to be a suitable masking material that, under appropriate conditions, has very weak adhesion to the epitaxial layer.

3.3.1 Experimental Procedure

Two wafers were used for this work, the first Cz, 0.3Ωcm, p/B, (100) orientated and 275μm thick and the second Cz, 0.2Ωcm, p/B, (111) orientated and 380μm thick. Dislocations were introduced to both wafers by doing a very heavy phosphorous diffusion (4 hours at 1100°C). The phosphorous doped region was then stripped from the wafer using a 1:20 HF:HNO₃ solution.

A 60nm thick oxide was grown on both wafers and they were divided into three sections. On the first section, the oxide remained, so that during the LPE process, growth did not occur. The oxide was stripped from the second section, so that LPE resulted in growth of a plain epitaxial layer. The third section was patterned with a grid orientated along the (110) direction with lines 2μm wide, spaced 80μm apart. This resulted in growth of a layer that could be useful for the epilift process. Growth was done from 980–790°C using a cooling rate of 2°C/minute, a 6N (99.9999%) pure indium melt and a 40–90Ωcm p/B source wafer.

Once the epitaxial layers had been grown, Yang’s etch [358], consisting of a 1:1 mix of 1.5M CrO₃ and 49% HF was used to differentiate the dislocations. Dislocations were visible as etch pits on the wafer and were viewed using a scanning electron microscope (SEM).

3.3.2 Results and Discussions

Figure 3.9 shows an SEM image of the etch pits resulting from dislocations on the (100) orientated wafer. The first image is of the section of the substrate that was covered in oxide, and on which no epitaxial growth occurred. The second image shows the epitaxial layer grown on the plain substrate and the third shows the epitaxial layer grown on the patterned substrate. Figure 3.10 shows similar images for the (111) orientated wafer.

For both wafers, the number of dislocations on the plain epitaxial layer was significantly greater than on the substrate wafer. In both cases, the number of dislocations visible on the epitaxial layer grown on the patterned substrate was significantly reduced compared with the number on the substrate wafer. The results support the view that dislocations present in a substrate do not multiply into an epitaxial layer grown from seeding lines and show that it is not possible to use a dislocated substrate as a means for introducing dislocations into the epitaxial layer.
3.3 Dislocations Within the Epitaxial Layer

Figure 3.9: An SEM image showing etch pits resulting from dislocations on a) the plain (100) orientated wafer, b) the epitaxial layer grown on the plain, (100) orientated substrate and c) the epitaxial layer grown on the (100) substrate patterned with a square oxide grid.
Figure 3.10: An SEM image showing etch pits resulting from dislocations on a) the plain (111) orientated wafer, b) the epitaxial layer grown on the plain, (111) orientated substrate and c) the epitaxial layer grown on the (111) substrate patterned with a square oxide grid.
3.4 Lifetime Experiments

A minority carrier lifetime in silicon is a measure of the electronic quality. It is the average amount of time a minority carrier exists before it recombines with a majority carrier and is effectively lost to the cell. Similarly, the minority carrier diffusion length is the average distance a minority carrier travels before it recombines with a majority carrier. Lifetime measurements are discussed in more detail in section 4.5. Minority carrier lifetime, \( \tau \), is related to the diffusion length, \( L \), through:

\[
L = \sqrt{D \tau}
\]  

where \( D \) is the diffusion coefficient. With thinner cells it is acceptable to have a shorter diffusion length and therefore a lower minority carrier lifetime while still obtaining high internal quantum efficiencies. Epilift layers grown using an oxide mask have been demonstrated to have a comparatively high lifetime. Catchpole et al. [83] measured effective minority carrier lifetimes of between 3.8–11.7\( \mu \)s with an average of 7\( \mu \)s on a p-type epitaxial layer (grown using an indium melt doped with gallium). This corresponds to a minority carrier diffusion length of 120\( \mu \)m, which is much greater than the average cell thickness of 40\( \mu \)m [85].

All the epitaxial layers grown on a patterned substrate discussed thus far have been made by patterning an oxide layer. In this section of work, the lifetimes resulting from layers grown using both oxide and carbonised photoresist barrier layers are compared. A thermally grown oxide has the advantage of being commonly used in the semiconductor industry. Carbonised photoresist is an alternative masking layer that may reduce stresses in the epitaxial layer and therefore reduce dislocation multiplication. Under appropriate conditions, the adhesion of epitaxial layers to a carbonised photoresist layer was found to be very weak and therefore it was supposed that stresses in the epitaxial layer may be reduced. This may be compensated by stresses arising from a mismatch in linear expansion coefficients.

3.4.1 Experimental Procedure

Epitaxial growth was done from seeding lines patterned in a masking layer. Three Cz 0.015\( \Omega \)cm p/B (100) wafers were used as substrates. The first had a 60nm thick oxide mask and the second and third had a carbonised photoresist mask. The photoresist was carbonised by placing it in a forming gas ambient at 1000\(^\circ\)C for 30 minutes after the pattern had been exposed.
Layers were grown from 970–780°C at a cooling rate of 2°C/minute. The source wafer for LPE growth was heavily phosphorous doped with a surface sheet resistance of 5Ω/□. This resulted in entirely n-type epitaxial layers on a heavily doped p-type substrate and the epitaxial layers could therefore be detached using an electrochemical etchant. The electrochemical etching setup is shown in figure 3.11. Silicon is dissolved via the reaction of holes in the silicon with F\(^-\) ions in the HF solution and silicon is then dissolved in the solution as aqueous H\(_2\)SiF\(_6\). The reaction pathway may occur according to [66];

\[
\begin{align*}
\text{Si} + 2\text{F}^- + 2h^+ & \rightarrow \text{SiF}_2 + 2\text{H}^+ \\
2\text{SiF}_2 & \rightarrow \text{Si} + \text{SiF}_4 \\
\text{SiF}_4 + 2\text{HF} & \rightarrow \text{H}_2\text{SiF}_6
\end{align*}
\] (3.2)

The etch is selective for p-type material because the concentration of holes is higher than in n-type material. The etch selectivity can be greater than 1000 times if the voltage is low and low to moderately doped n-type silicon is used. Etching must be done in the darkness to avoid the photo-generation of holes in the p-type material. For the results discussed in this section, electrochemical etching was done with a 2V bias in a 10% HF solution. The epilayers required 3–5 hours for complete detachment.
To prepare the wafers for lifetime measurements, the surface was thoroughly cleaned and then passivated. This involved:

- a 20 second 1:20:20 HF:HNO₃:H₂O etch, to remove porous silicon remaining after the electrochemical etch;
- a 10 second 1:20 HF:HNO₃ etch, to remove the top layer of silicon and potentially any contaminants;
- an RCA clean (10 minutes in a 5:1:1 H₂O:NH₃:H₂O₂ solution plus 10 minutes in a 5:1:1 H₂O:HCl:H₂O₂ solution, both at 80°C);
- a dip in 10% HF solution until hydrophobic, to remove the oxide that forms during an RCA clean;
- an oxidation at 1000°C for 30 minutes;
- removal of the oxide in a 10% HF solution. These last two steps ensured any traces of carbon had been removed;
- an RCA clean;
- a dip in 10% HF solution until hydrophobic;
- phosphorous diffusion and in-situ oxidation (resulting in a wafer sheet resistance of 180Ω/□ and an oxide thickness of approximately 20nm) and
- a 400°C forming gas (5% H₂ in Ar) anneal (FGA). The light phosphorous diffusion, oxidation and FGA passivate the surfaces.

Lifetimes were measured on detached epilayers using the microwave photoconductance decay (MPCD) technique. The PCD lifetime measurement technique is discussed in more detail in section 4.5. One of the wafers grown using the carbonised photoresist layer was detached in three separate pieces, which enabled the lifetime to be measured in different areas of the epitaxial layer.

### 3.4.2 Results and Discussions

The results are shown in table 3.3. Table 3.3 also shows the equivalent minority carrier diffusion lengths, calculated using equation 3.1 and assuming a bulk doping level of 5×10¹⁶/cm³ in the epilayer.

These results show that the n-type material produced in this work using an oxide barrier layer had an equivalent lifetime to the p-type material measured by Catchpole et
The effective lifetime and equivalent diffusion length of epitaxial layers grown using different barrier layers. The two results for carbonised photoresist were for two different wafers and the result shown for the second wafer (6\(\mu s\)) is an average of three measurements: 7.5, 5.4 and 5.5\(\mu s\).

The equivalent minority carrier diffusion length is slightly lower for this work due to the lower mobility of holes compared with electrons. The results indicate that the lifetimes resulting from using a carbonised photoresist barrier layer may be better than those resulting from using an oxide barrier layer, but further work is required to produce meaningful statistics. The results show that lifetimes were approximately equivalent for different regions of the same epitaxial layer.

The lifetime measurement includes both surface and bulk recombination. The bulk lifetime is likely to be slightly higher since the epitaxial layers have a relatively high surface to volume ratio. In all cases, the layer quality is more than sufficient since the diffusion length is greater than the cell thickness of 40\(\mu m\).

### 3.5 Boron incorporation into Epitaxial Layers

The purpose of the work presented in this section was to do a detailed analysis of boron doping of silicon grown by liquid phase epitaxy. A simple solar cell design using an epitaxial layer could consist of a p-type bulk, a back surface field (BSF) and an emitter region. The emitter and BSF may be formed by the diffusion of appropriate impurities into the bulk or they may be grown. The ability to control the doping of the grown layers is important because cell efficiency is a function of both the thickness and doping profile in each of the three regions.

Doping of the epitaxial layer may be achieved by the addition of dopant to the melt, either as a pure element or a compound or by using a doped silicon source wafer. The doping profile is determined by the amount of dopant in the melt, the segregation coefficient of the dopant as a function of temperature and the temperature profile during growth. Commonly used dopants for silicon LPE include phosphorous for the growth of...
n-type epitaxial layers, and gallium and aluminium for p-type epitaxial layers. Boron is another possible p-type dopant but has received comparatively little attention to date.

A tin melt was used for this work. Like indium, tin has a moderate silicon solubility at temperatures near 1000°C, a low vapour pressure and low toxicity. Compared with indium, tin is electrically inactive (indium forms an acceptor level at $E_A = E_V + 0.16eV$, resulting in p-type layers, with a hole concentration of less than approximately $2 \times 10^{16}/cm^3$, in the absence of other dopant atoms [343]) and it is relatively abundant. A disadvantage of tin is that layers grown using a tin melt may have a reduced electronic quality since there are many misfit dislocations at the substrate/epitaxial layer interface [343].

The incorporation of boron into silicon epitaxial layers grown from a tin melt has been studied by Baliga. Baliga grew layers of 50-100μm thickness between temperatures of 1000°C and 900°C using cooling rates of 0.2-7°C/minute and found that the amount of boron transferred to the epitaxial layer decreased exponentially with depth. Baliga inferred from the growths that boron is rapidly depleted from the melt and that all of the boron is incorporated into the epitaxial layer in a single growth [24, 25].

### 3.5.1 Experimental Procedure

In most cases, the cooling rate was 2°C/minute and growth began at 970°C and ended at 780°C. Substrate wafers were 40-90Ωcm, p-type, (100) orientated and Cz. The tin was of six nines purity. Details of the source wafers are included in the relevant sections.

Doping profiles were measured using spreading resistance (SR) analysis and the total amount of boron present in very thin epitaxial layers was profiled using secondary ion mass spectrometry (SIMS). SR analysis measures electrically active material (as n- or p-type) and measurements were done as a depth profile over the full epilayer thickness. SIMS measurements are limited to a few microns and measure the total amount of a particular isotope present in the silicon. Boron 11 was profiled, but as boron is present in the normal isotopic ratio, the total amount of boron was obtained by multiplying the initial SIMS results by 1.25.

### 3.5.2 Doping Profiles

Figure 3.12 shows doping profiles of two epitaxial layers grown from 970-780°C at a cooling rate of 2°C/minute. A thickness of zero corresponds to the epitaxial layer/substrate interface, so that increasing thickness corresponds to decreasing temperature and later times. The layers were grown using a tin melt saturated with two different silicon sources. The first source was undoped, and the second highly boron doped (0.001-0.005Ωcm, which
corresponds to a doping level of $2-11 \times 10^{10}$ atoms/cm$^3$. The undoped source resulted in a very low n-type doping, due to the presence of residual n-type impurities in the tin melt. Adding boron to the melt via the silicon source wafer resulted in p-type doping of the epitaxial layer. In the regions where the hole concentration resulting from the boron doped silicon was more than an order of magnitude greater than the electron concentration resulting from n-type impurities in the tin melt, the carrier concentration can be assumed to approximate the concentration of electrically active boron.

![Graph showing carrier concentration vs. thickness](image)

**Figure 3.12:** An epitaxial layer grown using an undoped tin melt compared with an epitaxial layer grown using a heavily boron doped melt. The zero thickness point is the epitaxial layer/substrate interface.

The maximum boron concentration in the epitaxial layer shown in figure 3.12 was approximately $9.6 \times 10^{17}$ atoms/cm$^3$, and occurred in the first stages of growth. The amount of boron incorporated into the epitaxial layer dropped rapidly and the surface was n-type. This is in qualitative agreement with the results of Baliga [24, 25]. In contradiction to Baliga’s assumption, the amount of electrically active boron in the epitaxial layer is much less than the total amount of boron released from the source wafer. Incorporation of all of the boron released from the source wafer into the epitaxial layer in electrically active form should result in a p-type epitaxial layer with a mean doping of at least $2 \times 10^{19}$ atoms/cm$^3$.

One possible explanation of the ‘missing boron’ is that it remains in the melt and is available for layer growths. Figure 3.13 compares the doping profile of a second epitaxial
layer grown using the same melt with the boron doped epitaxial layer of figure 3.12. A lightly doped source (20-60Ωcm, n-type and phosphorous doped) was used to saturate the melt for this second growth. The p-type doping that occurs in the first few microns of growth suggests that some residual boron was still present in the melt following the growth of the first epitaxial layer. The available concentration had dropped by more than an order of magnitude. With further growths, the boron concentration in the epitaxial layer continued to drop and approached that of a layer grown from an undoped melt. The residual boron available for incorporation in the early stages of the second growth shown in figure 3.13 suggests that boron was not completely depleted from the melt in a single growth step, but insufficient remained to explain the ‘missing boron’. The results also suggest that the segregation coefficient for boron from liquid tin into solid silicon decreased between 970°C and 780°C.

![Graph showing carrier concentration vs. thickness for first and second growths](image)

**Figure 3.13:** A comparison of two epilayers grown directly following each other without re-doping the melt. Although the first growth shows no further boron deposition at low temperatures (the epitaxial layer surface), at higher temperatures (close to the epitaxial layer/substrate interface of the second growth) a small amount of boron remained, and the half of the epitaxial layer was p-type.

A second possible explanation of the ‘missing boron’ is that most of the boron incorporated into the epitaxial layers was electrically inactive. SIMS measurements do not support this hypothesis. Figure 3.14 shows boron concentrations for a sample that was
profiling with both SIMS (which measures total boron concentration) and SR (which measures electrically active boron) analysis. The surface peak in the SIMS measurement is due to an ion implantation step done for calibration purposes. The surface concentrations of electrically active and total boron concentrations were in good agreement with each other. Many SIMS measurements on the same samples showed that doping levels were uniform over the epitaxial layer surface to within a factor of two. In conclusion, most of the boron that dissolved into the melt from the boron doped source wafers was not incorporated into the epitaxial layers and was not available for subsequent growths.

![Graph](image.png)

**Figure 3.14:** A comparison of electrically active (measured using spreading resistance) and total (measured using SIMS) amounts of boron in a 2µm thick epitaxial layer. The surface peak in the ‘total boron’ curve is due to an ion-implantation step that was necessary for SIMS calibration.

### 3.5.3 Possible Mechanisms of Boron Removal

Three possible explanations for the apparent disappearance of boron from the system were considered. Firstly, boron hydrides may have formed due to a reaction between boron in the melt and the hydrogen gas. Many BₙHₘ compounds including B₂H₆ and B₄H₁₀ have boiling points below 220°C and would therefore be gaseous at 970°C. In order to test this hypothesis, it would be necessary to carry out growth in a vacuum or to detect boron compounds at the exit of the LPE system. Growth without hydrogen is difficult since hydrogen is necessary to remove the thin native oxide layer that forms on the silicon surface and epitaxial growth will not occur on an oxide covered surface [343]. Detection of boron compounds at the LPE exhaust is also difficult because the amount of boron in the
system is small, compared with the volume of the hydrogen gas. The removal of boron by hydrogen gas has also been suggested by Kopecek et al. [188] to explain the observation that boron did not accumulate in an indium melt after meltback of a significant number of heavily boron doped UMG-Si source wafers.

Secondly, boron may have been incorporated into the graphite, with which the melt was in contact during growth and saturation. In order to test for this, epitaxial layers were grown in an arrangement that avoided all contact between the melt and the graphite during the process. Two growths were done, the first with a 30 minute dwell time between saturation and growth and the second with a 4 hour dwell time between saturation and growth. SIMS measurements show that, again, the long dwell time reduced the amount of boron available for incorporation into the epitaxial layer. This suggests that boron was not incorporated into the graphite crucible.

A third possibility is that boron precipitates may have been formed within the tin melt. The solubility of boron in tin at the temperatures used in the LPE system is likely to be extremely low since no significant dissolution of boron into tin could be detected even at 1500–1600°C in a hydrogen atmosphere [141]. In this case, it may be expected that agitation of the melt would result in an increase in the rate of precipitation of boron. This is supported by an experiment in which the silicon substrate was placed on top of the melt during growth, rather than underneath it. The SR profile resulting from this experiment is shown in figure 3.15. In this arrangement, convection cells were set up within the melt during growth [172, 182] and the boron concentration in the epitaxial layer decreased more rapidly. The peak boron concentration shown in figure 3.15 is lower than that shown in figure 3.12. This may be due to the different physical arrangement for the growth where the substrate was placed above the melt. It may also indicate that that there was a slightly longer dwell time for the results shown in figure 3.15 since boron is depleted rapidly in the early growth stages.

In conclusion, the likely mechanisms for the removal of available boron from the LPE system are in the form of boron precipitates that remain in the tin melt or as volatile boron hydrides.

### 3.5.4 Application to Solar Cells

The removal of available boron from the LPE system with time may be useful for the epilift process. It is possible to tailor the time-temperature profile of the growth to obtain specific doping profiles. A particular example is the formation of the back surface field and bulk of a thin film solar cell in a single growth step. Such a structure was obtained as follows. A tin melt was saturated from a heavily boron doped source wafer at 970°C for
Figure 3.15: The doping profile resulting from a growth where the substrate was placed on top of the melt. The first 14µm were p-type and the remainder of the layer was n-type.

30 minutes. Following saturation, the melt was tipped onto the substrate and cooled to 965°C at 2°C/minute. This resulted in the growth of a thin layer, useful as a moderately doped back surface field. The temperature was then held constant at 965°C for 5 hours in order to remove most of the available boron from the system. Finally, the melt was cooled to 780°C at 2°C/minute to produce the lightly doped region. The resulting doping profile is shown in figure 3.16. The first half of the lightly doped region was p-type, due to the presence of some residual boron in the melt following the 5 hour dwell. The remainder of this region was n-type due to the presence of donor impurities in the tin melt. A discontinuous profile like that shown in figure 3.16 can usually only be obtained using LPE by doing two separate growths using differently doped melts and has correspondingly increased costs. Five hours is a long dwell time. Given that the available boron in the melt is significantly reduced during a typical growth of 2 hours, or in an arrangement with the substrate wafer held above the melt, the 5 hour period could be significantly reduced. A long dwell time becomes less significant for larger batches.

The addition of other dopants, such as gallium, can be used to ensure that the base region of the epitaxial layer is entirely p-type. Figure 3.17 shows the doping profile for an epitaxial layer grown with the addition of gallium to a tin melt. The results shown in this figure indicate that gallium is conserved in the melt in an available form, unlike boron.
3.6 Conclusions

The morphology resulting from grids with different seeding line widths, grown with cooling rates of 0.3, 1 and 3°C/minute and with seeding lines orientated at 90° and 60° relative to each other and was studied. The results were explained using arguments of free energy, constitutional supercooling and the relative availability of growth sites and the local supersaturation of the melt.

Dislocated substrate wafers of (100) and (111) orientation were produced and used to determine the transfer of dislocations into both a plain epitaxial layer and an epitaxial layer grown on a patterned substrate. For both wafer orientations, growth on the plain substrate resulted in a high density of dislocations but growth on a patterned substrate resulted in a relatively low density of dislocations. Dislocations present in a substrate were found not to multiply during growth of an epitaxial layer using a mask with seeding lines. This has important implications for the use of low quality, inexpensive substrates for solar cell production.

The effective lifetime of epitaxial layers grown using barrier layers of oxide and carbonised photoresist were compared. Carbonised photoresist masks resulted in effective lifetimes at least as high as when oxide was used. The n-type layers produced with this
The incorporation of boron into silicon grown using liquid phase epitaxy and a tin melt was studied. Boron incorporation was shown to be a function of both time and of temperature. The segregation coefficient for boron from liquid tin into solid silicon was inferred to be temperature dependent and to decrease with decreasing temperature. Boron incorporation decreased with time, probably due to either the formation of volatile boron hydrides that were removed from the system or boron precipitates that remained in the tin melt. Boron incorporated into the epitaxial layer was spatially uniform and electrically active. By choosing appropriate growing conditions, an abrupt and heavily doped p-type region was formed at the substrate/epitaxial layer interface. This would be useful as a back surface field for epilift solar cells.
Oxide/Nitride Stacks:  
Introduction

This chapter examines the use of oxide/nitride stacks on silicon using low pressure chemical vapour deposition (LPCVD) to deposit the nitride. The aim of this work was to determine if a nitride could be deposited in the early stages of cell fabrication. The motivation was that the nitride could then be used both throughout cell processing and as an anti-reflection coating for finished cells. Theoretical reflection losses from an oxide/nitride stack have been calculated and the influence of nitride deposition on effective lifetime for high resistivity, p-type, (100) oriented wafers was determined. There were two main conclusions. Firstly, with a 25nm thick oxide to provide adequate surface passivation, the ideal nitride thickness was determined theoretically to be approximately 50nm. Secondly, with a thin oxide layer between the silicon and the nitride, deposition of an LPCVD silicon nitride did not significantly alter effective lifetimes. Other examples of work on anti-reflection coatings formed in the early stages of cell fabrication are discussed in section 4.7.

4.1 Introduction

A silicon oxide/silicon nitride stack on silicon can behave as a good anti-reflection coating (ARC). In addition, silicon nitride has many properties that allow for increased processing flexibility and hence the realisation of novel cell structures. These properties include:

• nitride layers deposited at high temperatures are very hard and therefore scratch resistant. This is useful because scratches on the wafer surface may lead to shunts in a finished cell;

• nitride is etched much more slowly than oxide in solutions containing HF. This allows diffusion oxides to be thoroughly deglazed without fear of removing the masking nitride;
nitride can be used to mask against the oxidation of silicon because it oxidises very slowly and is relatively impermeable to oxygen;

- silicon nitride is a more effective diffusion barrier than silicon dioxide to many elements and

- a deposited nitride will correct for pinholes that may occur in a thermally grown oxide due to non-volatile particulates on the surface [264]. The nitride layer may also contain pinholes, but it is unlikely that these will align with pinholes in the oxide. This is particularly useful in cases when shunting is a major concern (for example, an interdigitated cell design with both contacts on the same side of the wafer).

Both the bulk minority carrier lifetime and the surface recombination velocity affect the efficiency of a solar cell. Therefore, the effect of the formation of an oxide/LPCVD nitride stack and post deposition treatment on both of these parameters must be determined. With thinner cells, such as the epilift cells discussed in chapter 3, the surface to volume ratio is increased and therefore the effect on surface recombination becomes increasingly important.

### 4.2 Low Pressure Chemical Vapour Deposition

The silicon nitride in this work was formed using low pressure chemical vapour deposition (LPCVD). This results in the deposition of amorphous, approximately stoichiometric silicon nitride, \( \text{Si}_3\text{N}_4 \). The LPCVD method was chosen as it is a reliable, mature technique with high throughput rates. LPCVD systems typically use pressures of between 0.01–1torr and are done in a ‘hot wall’ reactor, meaning that the entire furnace is heated. LPCVD is well suited to batch mode deposition, which is more economical than handling individual wafers [151]. LPCVD deposition generally results in good layer uniformity compared with other CVD systems. Compared with atmospheric pressure CVD (APCVD), LPCVD requires less dilutant gases [246].

Plasma enhanced chemical vapour deposition (PECVD) is an increasingly common method of nitride deposition in commercial solar cell manufacturing. It is used as one of the final stages of cell fabrication and provides excellent surface passivation, on both bare and oxide covered silicon [1]. To use silicon nitride as a processing aid, and hence to take advantage of the properties listed in section 4.1, it must be deposited in the early stages of cell fabrication. The wafer, with oxide/nitride stack, must therefore undergo high temperature steps. Since the advantage of PECVD nitride, namely the superior surface passivation, is lost when the wafer is heated (due to the loss of hydrogen), it is
not necessarily the optimal choice for nitride deposition, if the nitride is to be deposited in the early stages of cell fabrication. Table 4.1 is a comparison of LPCVD and PECVD methods. There are many exceptions to the generalised values shown in this table.

During deposition in an LPCVD furnace, the wafers are held inside a quartz cage, which leads to good radial uniformity [151]. Figure 4.1 is a schematic of the LPCVD system used to deposit silicon nitride for the work in this thesis. The deposition was done by reacting ammonia (NH₃) and dichlorosilane (SiH₂Cl₂ or DCS) to produce silicon nitride. The reaction is shown in equation 4.1:

$$3\text{SiH}_2\text{Cl}_2(g) + 4\text{NH}_3(g) \rightarrow \text{Si}_3\text{N}_4(s) + 6\text{Cl}_2(g) + 6\text{H}_2(g).$$  (4.1)

There are other reactions occurring in the LPCVD furnace, such as the dissociation of ammonia [246];
Many by-products are formed during nitride deposition, for example, hydrochloric acid (HCl). This may react with ammonia to form ammonium chloride (NH₄Cl) [243], a white powder that sublimes at 340°C [120]. Ammonium chloride can cause blockage problems in the vacuum system. The HCl, however, can be advantageous as it aids deposition by cleaning both the wafer surface and the deposition equipment and it also minimises ion contamination [264].

For all wafers, silicon nitride deposition was done at 0.6torr, 750°C and with a DCS:NH₃ flow rate of 1:4. Having an excess of NH₃ ensures the stoichiometry is maintained [264]. The deposition procedure used for the work discussed in this thesis is shown in figure 4.2. Deposition rates were typically ~6nm/minute, except for the first 3 minutes, during which deposition rates were negligible. The deposition rate was determined by including a polished wafer and using the Filmetrics system (discussed in section 4.4) to determine the nitride thickness. The wafers were always RCA cleaned and rinsed prior to deposition. An RCA clean involves 10 minutes in a 1:1:5 H₂O₂:NH₃:H₂O solution at 80°C followed by 10 minutes in a 1:1:5 H₂O₂:HCl:H₂O solution at 80°C. Nitrogen was used to pump down the system before use and to flush out the system after use. Some
specific problems that were encountered with the LPCVD deposition system are discussed in section 4.6.1.

4.3 Reflection Losses from an Oxide/Nitride Stack.

An oxide/nitride stack on silicon may behave as a good anti-reflection coating. Plain, polished silicon reflects more than 30% of incident sunlight for wavelengths corresponding to an energy greater than the band gap of silicon. Minimising reflection losses is therefore crucial in order to produce high efficiency silicon solar cells. The anti-reflection properties are dependent on the composition and thickness of both the oxide and the nitride and on the encapsulation material. This section discusses theoretical reflection losses from an oxide/nitride stack on silicon encapsulated under pottant, as shown in figure 4.3. As will be discussed later, the oxide layer must be underneath the nitride layer to ensure adequate surface passivation of the silicon wafer.

Since the refractive indices of silicon oxide, silicon nitride and silicon as a function of wavelength are well known, the reflection properties of an oxide/nitride stack on silicon can be accurately described using thin-film optics. An equation describing reflection loss from a double layer thin-film interface where both layers are transparent was published in 1948 by Crook [92], with the assumption of normal incidence onto an isotropic medium. Taking $E_0^-$ and $E_0^+$ to be the amplitudes of the electric vector for reflected and incoming light at the top surface and $n_i$ to be the refractive index of the $i$th layer, which is typically
Figure 4.3: An oxide/nitride stack on silicon and encapsulated under pottant. $E_0^-$ and $E_0^+$ are the amplitudes of the electric vector for reflected and incoming light at the top surface, $n_i$ are the refractive indices and $r_i$ are the Fresnel reflection coefficients.

A function of wavelength, $E_0^-$ may be written:

$$E_0^- = \frac{r_1 + r_2 \exp^{-2i\delta_1} + r_3 \exp^{-2i(\delta_1 + \delta_2)} + r_1 r_2 r_3 \exp^{-2i\delta_2}}{1 + r_1 r_2 \exp^{-2i\delta_1} + r_1 r_3 \exp^{-2i(\delta_1 + \delta_2)} + r_2 r_3 \exp^{-2i\delta_2}} E_0^+.$$  \hspace{1cm} (4.3)

$\delta_i$ is defined by

$$\delta_i = \frac{2\pi n_i d_i}{\lambda}$$ \hspace{1cm} (4.4)

where $d_i$ is the thickness of the $i$th layer, $\lambda$ is the wavelength of light. $r_i$ is the Fresnel reflection coefficient of the $i$th layer, given by

$$r_i = \frac{n_{i-1} - n_i}{n_{i-1} + n_i}.$$ \hspace{1cm} (4.5)

Figure 4.3 shows $E_0^-$, $E_0^+$, $n_i$ and $r_i$.

The reflectance, $R$, from the surface is defined as the ratio of reflected to incident energy. This is given by:

$$R = \frac{E_0^- (E_0^-)^*}{E_0^+ (E_0^+)^*},$$ \hspace{1cm} (4.6)

where the *s denote complex conjugates.

Defining $C$ by

$$C = \frac{r_1 + r_2 \exp^{-2i\delta_1} + r_3 \exp^{-2i(\delta_1 + \delta_2)} + r_1 r_2 r_3 \exp^{-2i\delta_2}}{1 + r_1 r_2 \exp^{-2i\delta_1} + r_1 r_3 \exp^{-2i(\delta_1 + \delta_2)} + r_2 r_3 \exp^{-2i\delta_2}}.$$ \hspace{1cm} (4.7)
4.3 Reflection Losses from an Oxide/Nitride Stack.

**Figure 4.4:** Theoretical reflectance from an oxide/nitride stack on silicon and under pottant as a function of wavelength. The curves are for: a 150nm oxide under a 150nm nitride (solid line), a 50nm oxide under a 50nm nitride (dashed line) and a 20nm oxide under a 50nm nitride (dotted line).

Equation 4.3 may be expressed as:

\[ E_0^- = CE_0^+ . \]  

(Hence, from equation 4.6,

\[ R = \frac{CE_0^+(CE_0^+)^*}{E_0^+(E_0^+)^*} = CC^* \]  

Figure 4.4 shows reflection, calculated using equation 4.9, as a function of wavelength for different oxide and nitride thicknesses. In order to plot the curves shown in this figure, non-dispersive (i.e. independent of wavelength) refractive indices of 1.4 and 1.46 were used for pottant and silicon oxide, respectively. The refractive assumed indices of silicon and silicon nitride are shown in figure 4.5.

The air mass 1.5 terrestrial solar spectrum is shown in figure 4.6. Assuming that any photon (provided it has energy greater than 1.1eV, which is the bandgap of silicon) has equal chance of creating an electron / hole pair, then photon flux is more relevant than energy distribution. Photon flux is defined as the number of photons incident per area, at
Figure 4.5: The complex refractive index of silicon and silicon nitride \( n = Re(n) - iIm(n) \) as a function of wavelength. The refractive index of silicon nitride is that given for Si\(_3\)N\(_4\) in the Filmetrics system (discussed in section 4.4), \( Im(n) \) values for silicon nitride are approximately zero. The refractive index of silicon is from Green [130].

At a given wavelength, and is given by the energy distribution divided by the energy of an individual photon \( (hc/\lambda) \), where \( h \) is Planck’s constant, \( c \) is the speed of light in a vacuum, and \( \lambda \) is the wavelength). Photon flux is also shown in figure 4.6.

From figure 4.6, reflection from an oxide/nitride stack at, for example, 700nm is of more importance than reflection at 350nm. To account for this point, the reflection found using equation 4.9 can be weighted by the photon flux. This results in a solar weighted reflectance (SWR);

\[
SWR(\lambda) = \frac{R(\lambda) \times S(\lambda) \times \lambda/hc}{N}
\]

(4.10)

\( S(\lambda) \) is the energy distribution as a function of wavelength and \( N \) is a normalising factor equal to the maximum value of \( S(\lambda) \times \lambda/hc \). Figure 4.7 shows solar weighted reflectance curves for the same stack parameters as depicted in figure 4.4.

With the input photon flux shown in figure 4.6, the total solar weighted reflectance is given by:

\[
SWR_{\text{total}} = \frac{\int_{\lambda_1}^{\lambda_2} R(\lambda)S(\lambda)\lambda d\lambda}{\int_{\lambda_1}^{\lambda_2} S(\lambda)\lambda d\lambda}
\]

(4.11)

where \( \lambda_1 = 0.295\mu m \), below which negligible solar radiation is incident on the Earth and \( \lambda_2 = 1.13\mu m \), which is the bandgap of silicon.
Figure 4.6: Terrestrial energy distribution (solid line) and photon flux (dotted line) as a function of wavelength. The energy distribution is for air mass 1.5 \([105]\). Photon flux is found by dividing the energy distribution by the energy of a single photon, \(hc/\lambda\).

From equation 4.11, theoretical reflection loss for a range of oxide and nitride thicknesses can be calculated. Figure 4.8 shows a contour plot of total solar weighted reflectance as a function of both oxide and nitride thickness for an oxide/nitride stack under pottant. Refractive indices for both silicon and silicon nitride are as shown in figure 4.5 and the refractive indices of silicon oxide and pottant are assumed to be non-dispersive and equal to 1.46 and 1.4, respectively. The maximum reflection shown in figure 4.8 is 35.6\%, which occurs with 112nm of oxide underneath 94nm of nitride. The minimum reflectance is 6.5\%, which occurs with no oxide and 78nm of nitride. For a 25nm oxide between the silicon and the nitride, the minimum reflectance is 8.6\%, which occurs with 50nm of nitride. As will be discussed in section 4.6, a thin oxide is required to achieve good surface passivation. A 25nm thick oxide under a 50nm thick nitride represents a good compromise between anti-reflection properties and surface passivation.

4.4 Oxide and Nitride Thickness Measurements

Nitride and thin (\(< 100\text{nm}\)) oxide thicknesses were measured using a Filmetrics system \([162]\). Thicker oxide thicknesses were estimated using a colour chart. The Filmetrics
Figure 4.7: Theoretical solar weighted reflectance from an oxide/nitride stack on silicon and under pottant as a function of wavelength. These curves are for the same stacks as shown in figure 4.4, weighted by the photon flux shown in figure 4.6. The three curves are for: a 150nm oxide with a 150nm nitride (solid line), a 50nm oxide with a 50nm nitride (dashed line) and a 20nm oxide with a 50nm nitride (dotted line).
Figure 4.8: Theoretical values for total solar weighted reflectance as a function of oxide and nitride thickness for an oxide/nitride stack on silicon and under pottant. The colour bar on the right shows percentage reflectance.
system uses light from a tungsten-halogen bulb in the wavelength range 400–3000nm. Light travels through a bundle of fibre-optic cables to the sample, where a fraction of the light is reflected. Reflection at different wavelengths is measured by dispersing the light using a diffraction grating. A linear photodiode array is used to measure the reflected light intensity as a function of wavelength. The thickness is determined by fitting a curve to the measured reflection data.

4.5 Lifetime Measurements

When a photon enters a cell and creates an electron/hole pair, one of these carriers is the ‘majority’ carrier and the other is the ‘minority’ carrier. In p-type material, holes are majority carriers and electrons are minority carriers. The reverse is true in n-type material. There are two possibilities for a minority carrier. It may recombine with a majority carrier and be lost to the cell. More desirably, it may diffuse to the p-n junction. The electric field here ensures the minority carrier crosses the junction, whereupon it is collected and becomes a majority carrier.

Minority carrier lifetime is the average time a minority carrier survives before it recombines with a majority carrier and is lost to the cell. A minority carrier with a longer lifetime has a greater chance of diffusing to the p-n junction and being collected. Thin-film silicon solar cells can tolerate a lower minority carrier lifetime compared with thicker cells because there is a shorter distance to the junction. Lifetime measurements are a useful diagnostic tool because they do not require a finished solar cell and can therefore be used to determine the efficiency potential of a wafer as it progresses through different processing steps.

Recombination of carriers may occur both at the surface and within the bulk of a wafer. There are three mechanisms of bulk recombination; radiative, Auger and defect. Radiative recombination is illustrated in part a) of figure 4.9 and occurs when an excited electron drops to an energy level below the valence band edge and releases a photon. Auger recombination is illustrated in part b) of figure 4.9 and is more dominant in highly doped or excited material [129]. Auger recombination occurs when an electron and hole recombine and pass the extra energy to a third carrier (either electron or hole), which then loses this energy in phonon vibrations. Defect recombination is illustrated in part c) of figure 4.9. It occurs when a minority carrier and a majority carrier recombine at a crystal defect or impurity. Crystal defect or impurity levels located in the centre of the forbidden gap are more effective at lowering lifetime than those located at either edge [129]. Recombination at the surfaces is generally due to crystal defects. Like defect recombination
in the bulk, recombination at the surfaces is often described using the Shockley-Read-Hall (SRH) model. In a wafer, recombination may occur by all three methods shown in figure 4.9 and the effective lifetime is given by

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{radiative}}} + \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{defect}}}.$$  \hfill (4.12)

Each of these terms has a bulk and surface component. As stated above, recombination at the surface can normally be described by contributions to the $\tau_{\text{defect}}$ term.

Recombination characteristics at the surfaces and in the bulk can be measured by determining the effective lifetime at a range of injection levels. This is done by exciting the wafers optically and observing the changes in carrier populations.

The lifetime measurements made in this thesis were done using the quasi-steady-state photoconductance (QSSPC) apparatus developed by Sinton. The data was analysed to extract both effective lifetimes and emitter saturation current using the equations of Sinton and Cuevas [288] with the addition of a generalised equation for $\tau_{\text{eff}}$ valid for both transient and steady state behaviour, as described by Nagel et al. [226]. This addition means that a light pulse of any length can be used to obtain accurate data over a very wide range of lifetimes (typically from $\sim 0.1 \mu$s to several ms [201]). Without this addition, the QSS method must be used for shorter lifetimes and the transient method for longer lifetimes (more than about 100$\mu$s for the flash used for the measurements reported in this thesis, which has a decay time of 2.3ms [201]). Using the QSSPC apparatus, effective lifetime is found by shining a light pulse onto a wafer and determining the photon flux onto the sample, $N_{ph}$, and sheet photoconductance of the sample, $\sigma$, as a function of time. Photon
flux is measured using a calibrated reference solar cell and sheet photoconductance is measured using inductive coupling to the sample. From Cuevas and Sinton [93], the excess conductance of the wafer is related to the excess carrier density in the wafer, $\Delta n$, according to:

$$\Delta \sigma = q \Delta n (\mu_n + \mu_p) W.$$  \hspace{1cm} (4.13)

$\mu_n$ and $\mu_p$ are the electron and hole mobilities, respectively, $q$ is the charge on an electron and $W$ is the wafer width. Equation 4.13 can be solved iteratively for $\Delta n$ and $\mu_n + \mu_p$.

The effective lifetime in quasi-steady-state operation can then be expressed as [288]

$$\tau_{\text{eff}} = \frac{\Delta \sigma}{J_{\text{ph}} (\mu_n + \mu_p)},$$ \hspace{1cm} (4.14)

where $J_{\text{ph}}$ is the photogeneration rate inside the wafer, defined by

$$J_{\text{ph}} = q N_{\text{ph}} f_{\text{abs}},$$ \hspace{1cm} (4.15)

where $f_{\text{abs}}$ is the fraction of photons absorbed. $f_{\text{abs}}$ depends on the wafer thickness, the presence of an ARC and texturing and is usually between 0.70 and 0.95. By using a range of light intensities, a plot of $\tau_{\text{eff}}$ as a function of $\Delta n$ may be obtained. This contains information about both the bulk and the surface of the wafer. The maximum bulk lifetime is at least equal to the maximum effective lifetime. This maximum normally occurs near where the excess carrier density is equal to the dopant density. Since $\Delta n$ is known, an implied value for the open circuit voltage, $V_{\text{oc}}$, can be determined using [93]:

$$V_{\text{oc}} = \frac{kT}{q} \ln \frac{\Delta n (N_A + \Delta n)}{n_i^2},$$ \hspace{1cm} (4.16)

where $k$ is Boltzmann’s constant, $T$ is the temperature, $N_A$ is the density of acceptor atoms (p-type impurity atoms) and $n_i$ is the intrinsic carrier concentration, equal to $8.63 \times 10^9$ /cm$^3$ at 298K, as recalculated in 1991 by Sproul and Green [292]. The $V_{\text{oc}}$ values quoted in this thesis are at the equivalent of ‘1 sun’ light intensity.

In cases where a diffusion is present, the surface recombination can be characterised by the emitter saturation current, $J_{\text{oc}}$. This is similar to $J_o$ in the modified diode equation;

$$J = J_o (\exp (qV / nkT) - 1) - J_{\text{sc}},$$ \hspace{1cm} (4.17)

discussed in chapter 1, except that $J_{\text{oc}}$ contains contributions from the emitter region only. With a diffusion, the inverse of $\tau_{\text{eff}}$ can be written as a sum of bulk and surface
contributions;
\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{\text{bulk}}} + \frac{2J_{\text{oc}}(\Delta n + N_A)}{qn_i^2W} \tag{4.18}
\]
where \(\tau_{\text{bulk}}\) is the minority carrier lifetime in the silicon bulk. Equation 4.18 can be rearranged to give
\[
\frac{1}{\tau_{\text{eff}}} = \left(\frac{1}{\tau_{\text{bulk}}} + \frac{2J_{\text{oc}}N_A}{qn_i^2W}\right) + \frac{2J_{\text{oc}}}{qn_i^2W}\Delta n. \tag{4.19}
\]
At high injection levels, provided \(1/\tau_{\text{bulk}}\) is a constant, a plot of \(\Delta n\) against \(1/\tau_{\text{eff}}\) results in a straight line, the slope of which is proportional to the emitter saturation current, \(J_{\text{oc}}\), as described by Kane and Swanson [173]. Assuming the lifetime has negligible injection level dependence below the measured injection levels, this curve can be extrapolated to find a value for \(\tau_{\text{bulk}}\). Since this assumption is rarely true, this fit is often highly inaccurate. It is more rigorous to make measurements across a range of injection levels and then say that the maximum bulk lifetime is at least the maximum effective lifetime, as explained above.

There is an upper bound on the \(J_{\text{oc}}\) value that can be accurately determined (to within approximately 10%) using the equations of Kane and Swanson. This is given by [173];
\[
J_{\text{oc}} < 0.1q\frac{n_i^2}{N_{\text{min}}}\frac{D}{W} \tag{4.20}
\]
where \(N_{\text{min}}\) is the minimum carrier concentration for which the assumption of high-level injection is valid and is approximately ten times the wafer doping. For the high resistivity FZ material used for many of the experiments in this thesis, equation 4.20 means that the maximum \(J_{\text{oc}}\) that may be accurately determined is approximately 2500fA/cm²/side.

The lifetime measurements made for this thesis were done at a range of light intensities and effective lifetime as a function of injection level consists of a number of curves (typically three). Figure 4.10 shows two curves, the raw data collected from the lifetime tester for the case of \(\sim 1\) sun illumination and this same data used to obtain a plot of \(\Delta n\) against \(1/\tau_{\text{eff}}\), from which \(J_{\text{oc}}\) can be estimated. Figure 4.11 shows three plots of \(\Delta n\) against \(1/\tau_{\text{eff}}\) at different light intensities and hence injection levels. If a longer light pulse had been used, the lifetime in the two lower injection region would have been measured over a broader range of injection levels. Due to the use of the generalised equations described by Nagel et al., the accuracy of the data is not compromised by having a shorter light pulse.
Figure 4.10: Raw data from the QSSPC lifetime tester and the resultant plot of $\Delta n$ (excess carrier density) against $1/\tau_{\text{ef}}$. This is the high injection level region and light levels are approximately equivalent to 1 sun. This wafer had a light phosphorous diffusion on the surface and so a line fit to the second plot may be done to find $J_{\text{oc}}$. This fit gives a $J_{\text{oc}}$ of 10fA/cm$^2$/side.

Figure 4.11: Plots of $\Delta n$ (excess carrier density) against $\tau_{\text{eff}}$ (effective lifetime) for measurements made at three different light intensities. The legend shows the approximate light levels. From the $\sim$0.01 sun results, the bulk lifetime can be said to be at least 5ms.
4.6 The Influence of LPCVD Nitride Deposition on Effective Lifetime

Wafers with a high bulk lifetime were used for this work. They were 100–400Ωcm, (100) oriented, p-type FZ. After passivation with a light phosphorous diffusion, thermal oxidation and 30 minute, 400°C forming gas anneal, $J_{oc}$ values were $\sim 10\text{fA/cm}^2/$side. Under normal conditions, deposition of an LPCVD nitride did not significantly alter effective lifetimes at any injection level. The minimum oxide thickness was 25nm and the maximum nitride thickness was 200nm. Figures 4.12 and 4.13 show effective lifetimes before and after LPCVD nitride deposition for the cases of a 25nm oxide under a 65nm nitride and a 225nm oxide under a 200nm nitride, respectively. Both these figures show that effective lifetimes were not changed significantly by nitride deposition. As will be discussed in section 4.6.1, nitride deposition sometimes did cause a significant drop in effective lifetime, probably due to contaminants in the furnace.

With a very light phosphorous diffusion and no oxide, the silicon surface was essentially

![Figure 4.12: Effective lifetime curves for a wafer with a 25nm thick oxide before (x) and after (o) deposition of a 65nm thick LPCVD silicon nitride. Deposition was done at 750°C and $\sim 0.6\text{torr}$ and took 16 minutes. $J_{oc}$ values before and after nitride deposition were 7 and 6 fA/cm$^2$/side, respectively. Implied $V_{oc}$ values before and after nitride deposition were 710 and 713mV, respectively.](image)
Figure 4.13: Effective lifetime curves for a wafer with a 225nm thick oxide before (x) and after (o) deposition of a 200nm thick LPCVD nitride. Deposition was done at 750°C and ~0.6torr and took 46 minutes. $J_{sc}$ values before and after nitride deposition were 15 and 14 fA/cm²/side, respectively. Implied $V_{oc}$ values before and after nitride deposition were 702 and 708mV, respectively.
The Influence of LPCVD Nitride Deposition on Effective Lifetime

Figure 4.14: Effective lifetime curves for a wafer with no oxide before (x) and after (o) deposition of a 14nm thick LPCVD nitride. Deposition was done at 750°C and ~0.6torr and took 10 minutes. The $J_{oc}$ value after nitride deposition was 850fA/cm²/side. Implied $V_{oc}$ values before and after nitride deposition were 532 and 566mV, respectively.

un-passivated. Surface passivation improved slightly after deposition of an LPCVD nitride. Figure 4.14 shows effective lifetime curves before and after deposition of 14nm of LPCVD nitride on a wafer with an emitter sheet resistance after phosphorous diffusion of 1020Ω/□ and no oxide. High injection level lifetime had improved, implying improved surface passivation. Note that the low injection level lifetimes were similar before and after nitride deposition, implying that the bulk lifetime was mostly unaffected by nitride deposition.

4.6.1 Experimental Problems

On some occasions, deposition of LPCVD silicon nitride caused a large drop in effective lifetime. This usually correlated with a build up of ammonium chloride inside the furnace. In addition, the inlet tubes for the ammonia and dichlorosilane gas run unusually deep into the furnace. This has resulted in deposition of silicon inside the DCS tube, which means that gas supply can be irregular. Early problems with vacuum reliability and failure of various components due to chemical contamination were also encountered. Since the wafers used for this work had very high lifetimes, they were a very sensitive indicator of problems in the LPCVD furnace. The results reported in this thesis are only for wafers that
had negligible or very small change in effective lifetime after nitride deposition. The main manifestation of the reliability problem with the LPCVD system for the results reported in this thesis is that a wide range of nitride thicknesses was used since the nitride deposition rate was highly variable. Subsequent equipment modification means that operation of the LPCVD furnace has been greatly improved.

4.7 Other ARCs Formed in the Early Stages of Cell Fabrication.

The primary novelty of the work presented in this thesis is not the use of an oxide/nitride stack as an anti-reflection coating, but the use of a nitride layer that contributes to the AR properties of the finished cell and is designed to be deposited in the early stages of cell fabrication. Anti-reflection coatings formed in the early stages of cell fabrication have also been reported by the photovoltaic group at the University of New South Wales (UNSW), particularly in conjunction with the buried contact cell design. Two different ARC have been reported, an oxynitride and a silicon oxide/titanium oxide stack. In all cases, the increased processing flexibility offered by an early-formed ARC must be balanced against the response of the wafers to both layer formation and subsequent high temperature steps.

At the University of New South Wales, an oxynitride was used as an ARC with the double sided buried contact cell design. The oxynitride was formed by first growing a thin, thermal SiO$_2$ layer and then annealing this in an NH$_3$ ambient at 900–1200°C for 5–15 hours to form the oxynitride. For example, a 10 hour anneal at 1150°C of a wafer with a 14nm thick oxide resulted in a 17nm thick oxynitride with a refractive index of 1.7. Compared to an LPCVD deposition system, this method was reported to be more economical and to use less material [100]. When used to produce double sided buried contact solar cells, the oxynitride resulted in lower cell performance compared to cells made with a thick oxide. Substrates were 1Ωcm and cell efficiencies were 12.4–12.8% using an oxynitride layer, compared to 15–15.8% using a thick oxide. The lower performance with the oxynitride layer was reported to be due to an increased surface recombination velocity and a modified cell design was suggested to utilise the properties of the oxynitride [100].

Two methods of silicon oxide/titanium oxide stack formation have been investigated at UNSW. The first is thermal oxidation of a silicon wafer, to form a silicon oxide (SiO$_2$) layer, followed by spray pyrolysis deposition of titanium oxide (TiO$_2$). The second is TiO$_2$ deposition followed by thermal oxidation. Both methods result in a thin oxide layer that lies between the silicon and the TiO$_2$.

The advantages of TiO$_2$ are that it is deposited at low temperatures and at atmospheric
pressure; it is formed using a non-toxic, non-corrosive precursor; the spray pyrolysis technique is well established [259] and it acts as a good ARC. A possible disadvantage of TiO$_2$ is that temperatures of at least 400°C are required for resistance to etching in solutions containing HF [152]. With the buried contact cell design, an added advantage of using a deposited TiO$_2$ layer is that it forms only a very thin layer inside the grooves. This ensures the metal fingers are contained within the grooves, which means that reflection from the top surface is reduced and there is a reduced series resistance in the metal fingers [152].

To form an SiO$_2$/TiO$_2$ stack on silicon after deposition of TiO$_2$ onto bare silicon, wafers were annealed in an oxygen ambient at 800°C for 10–20 minutes, causing an SiO$_2$ layer to form between the TiO$_2$ and the silicon. The advantages of this method (rather than first growing a thermal oxide and then depositing a TiO$_2$ layer) are firstly, that the stoichiometry of the TiO$_2$ is preserved, thus reducing the optical absorption that occurs in a TiO$_2$ layer and secondly, that carbon contamination is reduced [259].

TiO$_2$ deposited directly on silicon was reported to provide very little surface passivation. With a thin oxide layer, however, surface passivation was provided. $J_{oc}$ values reported in the case of TiO$_2$ deposition onto a thermally grown oxide were 70fA/cm$^2$ with a 20nm thick oxide and 28fA/cm$^2$ with a 480nm thick oxide. In the case of no oxide, $J_{oc}$ after TiO$_2$ deposition was 1400fA/cm$^2$ [204]. In the case of TiO$_2$ deposited directly on silicon with a subsequent oxidation, $J_{oc}$ after TiO$_2$ deposition was reported to be 4000fA/cm$^2$. This reduced to 45fA/cm$^2$ after formation of the thin oxide layer. In this case the SiO$_2$ and TiO$_2$ layers were 6 and 67nm thick, respectively and the wafer had a 175Ω/□ phosphorous diffusion.

The effectiveness of TiO$_2$ as a phosphorous dopant source was investigated by Richards et al. [258] who added phosphorous to the TiO$_2$ solution prior to spraying onto the silicon. Using this method and placing the wafer firstly into an oxygen-containing ambient at 800°C to form the thin oxide layer and secondly into a nitrogen ambient for 80 minutes at 950°C to drive the phosphorous through to the silicon, an emitter sheet resistance of 300Ω/□ was formed on 1000Ωcm p-type FZ silicon [258]. $J_{oc}$ after emitter formation was reported to be 900fA/cm$^2$.

The ability of TiO$_2$ to act as a phosphorous diffusion barrier has also been investigated. The TiO$_2$ layer was found to be unacceptable for this purpose since, on exposure to phosphorous in a gaseous ambient, the optical properties were destroyed, the film became conductive and the surface passivation was very poor. These effects were speculated to be due to the formation of titanium phosphates and the consumption of the silicon oxide layer [258].
4.8 Conclusions

This chapter introduced oxide/nitride stacks on silicon. A 25nm thick oxide under a 50nm thick nitride was calculated to have good anti-reflection properties. A 25nm thick oxide under a 65nm thick nitride was demonstrated to provide excellent surface passivation properties ($J_{sc}$ of $\sim 7fA/cm^2/side$) both before and after nitride deposition. Deposition of an LPCVD nitride over an oxide was found not to significantly alter effective lifetimes for a range of oxide and nitride thicknesses. LPCVD silicon nitride deposited directly onto silicon was found to provide minimum surface passivation.
Chapter 5

High Temperature Processing of Wafers with Oxide/Nitride Stacks

This chapter discusses the effects of high temperature nitrogen anneals on silicon wafers with oxide/nitride stacks. As long as at least a thin oxide was used, a high temperature nitrogen anneal resulted in a reduction in surface passivation, but did not significantly affect the bulk lifetime. The reduction in surface passivation was shown to be due to a loss of hydrogen from the silicon/silicon oxide interface. Emitter saturation current, \( J_{oc} \), was used to characterise the effects of high temperature nitrogen anneals. Higher temperatures, thinner oxides, thinner nitrides and longer times at high temperatures were all found to cause an increase in \( J_{oc} \). A hydrogen loss model has been developed to explain the observations.

5.1 Introduction

In order to take advantage of the physical and chemical properties of silicon nitride as part of an oxide/nitride stack on silicon, the nitride should be deposited in the early stages of cell fabrication. A wafer with an oxide/nitride stack must therefore be able to withstand high temperature processes. This chapter discusses the effect of high temperature nitrogen anneals on wafers with an oxide/nitride stack. Firstly, the effect on the surface and on the bulk of the wafer is discussed and a hydrogen loss model is introduced to explain the observations. Secondly, the effect of varying oxide thickness, nitride thickness and the time and temperature of the high temperature step on emitter saturation current, \( J_{oc} \), are discussed. Lastly, possible methods of \( J_{oc} \) recovery after a high temperature step are discussed.
5.2 Experimental Conditions

The wafers used for this work were 100–400Ωcm, (100) oriented, p-type FZ. They were processed as shown in table 5.1. Measurements of the effective lifetime were used to assess the wafers at various stages. The passivating diffusion was very light. This was deliberate since a light diffusion enables a more sensitive measurement of the surface recombination rate.

The term ‘anneal’ is usually used to describe a high temperature treatment that does not result in growth on the wafer or introduction of dopants to the wafer. For example, a process may include a 60 minute 900°C anneal in nitrogen. For the work described in

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Saw damage etch</td>
<td>1:10 HF:HNO₃ To remove approximately 20μm from each side (usually ~5 minutes).</td>
</tr>
<tr>
<td>2</td>
<td>RCA (Radio Corporation America) clean</td>
<td>10 minutes in a 5:1:1 H₂O:NH₃:H₂O₂ solution plus 10 minutes in a 5:1:1 H₂O:HCl:H₂O₂ solution, both at 80°C.</td>
</tr>
<tr>
<td>3</td>
<td>HF dip</td>
<td>in 10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>4</td>
<td>Light phosphorous diffusion on both sides</td>
<td>830°C for 30 minutes with a main flow of N₂: 180l/hour. O₂: 130cc/min and N₂ through the POCl₃: 45cc/min. R = 600–1800Ω/□.</td>
</tr>
<tr>
<td>5</td>
<td>Phosphorous glass deglaze</td>
<td>10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>6</td>
<td>Oxidation</td>
<td>For thickness ≥100nm: 1100°C with TCA, thickness controlled by varying the time. For thickness ~25nm: 900°C for 60 minutes with TCA. For all: O₂ flow rate 100l/hour and 30 minute N₂ anneal before unloading at 1000°C (flow rate 100l/hour).</td>
</tr>
<tr>
<td>7</td>
<td>Forming gas anneal (FGA)</td>
<td>30 minutes at 400°C in forming gas (5% H₂ in Ar).</td>
</tr>
<tr>
<td>8</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities</td>
</tr>
<tr>
<td>9</td>
<td>RCA clean and LPCVD nitride deposition</td>
<td>Deposition pressure 0.6torr, temperature 750°C. Flow ratio of DCS: NH₃ 1:4. Nitride thickness controlled by varying the deposition time.</td>
</tr>
<tr>
<td>10</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>11</td>
<td>RCA clean and nitrogen anneal</td>
<td>Flow rate 100l/hour. Varying temperature and time. Wafers unloaded at anneal temperature, up to a maximum of 900°C.</td>
</tr>
<tr>
<td>12</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities</td>
</tr>
</tbody>
</table>

Table 5.1: Processing steps for the wafers discussed in this chapter. The starting material was 100–400Ωcm, (100) oriented, p-type FZ. Measurements of the effective lifetime were used to determine the effect of previous steps on the wafer.
this thesis, two types of anneals were done, in nitrogen and in forming gas. The purpose of the nitrogen anneals was to simulate high temperature treatments, such as diffusion or oxidation. These were done between 750°C and 1000°C. The purpose of the forming gas anneals was to introduce hydrogen and therefore passivate the wafer surface. These were done between 400°C and 1000°C.

5.3 Effect of High Temperature Nitrogen Anneals: Surface Versus Bulk

For wafers with an oxide and a nitride layer of any thickness, a high temperature anneal in nitrogen caused a drop in effective lifetime. Figure 5.1 shows the drop in effective lifetime that occurred for a wafer with 150nm of oxide under 33nm of nitride after a one hour anneal in nitrogen at 900°C.

Oxide growth can result in high compressive stress in the oxide near the silicon/oxide interface. For temperatures greater than about 950°C, the viscosity of the silicon oxide is sufficiently low so that the oxide flows, which alleviates the stress [264]. Silicon nitride, however, has a high viscosity at the temperatures used (up to 1000°C) for the nitrogen anneals. High temperature anneals of silicon wafers with a silicon nitride layer therefore have the potential to result in high levels of stress in the silicon, due to the difference in linear thermal expansion coefficients for silicon (2.3×10⁻⁶/°C) and silicon nitride (4.0×10⁻⁶/°C) [264]. This stress may result in the generation of crystallographic defects such as dislocations. Such defects would result in a reduction in bulk lifetime. This kind of bulk ‘damage’ is usually irreversible. Stress on the silicon wafer caused by the presence of the silicon nitride is one possible explanation for the drop in effective lifetimes that was seen for oxide/nitride stacks following nitrogen anneal. Another explanation is a loss of surface passivation. It is also possible that a combination of bulk and surface effects were reducing effective lifetimes.

To determine if irreversible damage was done during nitrogen anneals, the oxide and nitride were stripped from a number of wafers following a high temperature nitrogen anneal. These wafers were then re-oxidised and given a standard FGA at 400°C. This ensured the surface was well passivated and meant that any remaining drop in effective lifetime may be attributed to stress damage to the bulk by the nitride layer. Three scenarios were studied, with various thicknesses of oxide and nitride.

The first scenario was a relatively thick oxide under a relatively thin nitride. Three wafers were used with initial oxide thicknesses of 100, 225 and 300nm and a nitride thickness of 37nm. These wafers were subjected to nitrogen anneals for 1 hour each at 900
Figure 5.1: The effect of a 1 hour, 900°C nitrogen anneal on the effective lifetime of a wafer with a 150nm thick oxide and a 33nm thick nitride. The effective lifetime is shown both after oxide/nitride stack formation (x) and after nitrogen anneal (o). Note that the wafer is of very good quality and even after nitrogen anneal, the maximum bulk lifetime is still at least 5ms. The $J_{oc}$ value increased from $14\text{fA/cm}^2$/side after oxide/nitride stack formation to $160\text{fA/cm}^2$/side after nitrogen anneal. Implied $V_{oc}$ values fell from 703mV to 644mV.
and at 1000°C. The oxide/nitride stack was removed and a 150nm thick oxide was grown on all samples (at 1100°C with a 30 minute nitrogen anneal at 1000°C). Figure 5.2 shows ‘oxide 1’ and ‘oxide 2’ lifetime curves. ‘Oxide 1’ curves were measured after initial oxidation and ‘oxide 2’ curves after oxide/nitride stack formation, nitrogen anneals, removal of the oxide/nitride stack and growth of a second oxide. For both measurements, surface passivation was excellent, so any difference between the two curves indicates irreversible damage resulting from stresses caused by the presence of the nitride. The two curves are very similar, suggesting that there has been negligible irreversible damage to the bulk of the wafer.

The second scenario was a relatively thin oxide under a nitride of approximately equal or greater thickness. The oxide thickness was 25nm for all wafers and nitride thicknesses were 18, 47, 72 and 94nm. Once again, these wafers were subjected to nitrogen anneals for 1 hour each at 900 and at 1000°C. After removal of the oxide and nitride, a second, 25nm thick oxide was grown (at 900°C with a 30 minute nitrogen anneal at 1000°C). Figure 5.3 shows ‘oxide 1’ and ‘oxide 2’ lifetime curves. ‘Oxide 1’ curves were measured after initial oxidation and ‘oxide 2’ curves after oxide/nitride stack formation, nitrogen anneals, removal of the oxide/nitride stack and growth of a second oxide. In each case, the effective lifetimes shown in the ‘oxide 2’ curve are slightly lower than those shown in the ‘oxide 1’ curve. The difference is very small and may be attributed to a small amount of irreversible damage caused by stress from the silicon nitride or to a contamination problem.

In the third scenario, no oxide was used beneath the silicon nitride. Figure 5.4 shows final lifetime curves for a wafer with no oxide compared with the final curves for the wafers with thick oxides under the nitride. (Initial and final effective lifetime curves for the wafer with no oxide can not be compared since there was negligible surface passivation without the oxide). The wafer with no initial oxide had significantly lower effective lifetimes than the wafers that did have an oxide layer. In the absence of the oxide, the nitrogen anneal appears to have resulted in irreversible damage to the wafer bulk. An alternative explanation is that the silicon nitride contained impurities that diffused into the silicon, but not through the silicon dioxide. This is unlikely since a thin silicon oxide layer is not an effective diffusion barrier for many ions [264].

In the case of no oxide underneath the nitride it is possible that while the irreversible damage is not restricted to the surface, it does not extend very far into the bulk. An experiment was done to determine if damage to the wafer bulk was confined to the first few microns. Two wafers were passivated with light phosphorous diffusion, 25nm thick oxide and 400°C FGA. This showed the potential effective lifetime of the wafers, which was high, as expected. The oxide was then stripped and nitride (38nm) was deposited
Figure 5.2: Irreversible influence of nitrogen anneals on effective lifetime for silicon wafers with a thick oxide under a relatively thin nitride. Each graph represents one wafer that initially had 100, 225, or 300nm of oxide (as shown in the title of each graph) and 37nm of nitride. All wafers were subjected to nitrogen anneals for 1 hour each at 900 and at 1000°C (at which stage, the effective lifetime had degraded significantly). The oxide and nitride were then stripped from the wafers and a second, 150nm thick oxide was grown. Two data sets are shown for each wafer. The ‘o’ marks represent wafers after first oxide growth and 400°C FGA. These represent close to the best lifetimes that may be expected from each wafer. The ‘x’ marks represent the same wafers after nitride deposition, nitrogen anneal, oxide/nitride removal, second oxidation and 400°C FGA.
5.3 Effect of High Temperature Nitrogen Anneals: Surface Versus Bulk

Figure 5.3: Irreversible influence of nitrogen anneals on effective lifetime for silicon wafers with a thin oxide under a relatively thick nitride. Each graph represents one wafer that initially had 25nm of oxide and 18, 47, 72 or 94nm of nitride (as shown in the title of each graph). All wafers were subjected to nitrogen anneals for 1 hour each at 900 and at 1000°C (at which stage, the effective lifetime had degraded significantly). The oxide and nitride were then stripped from the wafers and a second, 25nm thick oxide was grown. Two data sets are shown for each wafer. The ‘o’ marks represent wafers after first oxide growth and 400°C FGA. These represent close to the best lifetimes that may be expected from each wafer. The ‘x’ marks represent the same wafers after nitride deposition, nitrogen anneal, oxide/nitride removal, second oxidation and 400°C FGA.
directly onto the silicon. The wafers were given a nitrogen anneal, one at 900°C and the other at 1000°C, both for 1 hour. As expected, effective lifetimes at this point had dropped considerably. The nitride was then stripped, a 25nm thick oxide was grown and the wafers were given a 400°C FGA. As expected, effective lifetimes did not recover during this step. The oxide was removed and silicon was stripped from the wafers (9μm per side from the wafer that had the 900°C nitrogen anneal and 12μm per side from the wafer that had the 1000°C nitrogen anneal). Another light phosphorous diffusion was done and a 25nm thick oxide was grown with a 400°C FGA. The results for the 1000°C nitrogen anneal are shown in figure 5.5. This wafer had approximately 12μm of silicon stripped from each side before repassivation. There has been no improvement to the effective lifetime as a result of this silicon strip, indicating that the damage caused by stress is deeper than 12μm on each side. These results are very similar to those for the wafer that had the 900°C nitrogen anneal.

In conclusion, heating a wafer with an oxide/nitride stack in a nitrogen ambient did not cause significant irreversible damage to the wafer. This was the case even with a thin oxide and a thick nitride. For all wafers, there was a drop in effective lifetime after a high temperature nitrogen anneal. In the cases where at least a thin oxide was present, this can be attributed to a lack of surface passivation, rather than to significant damage to the silicon bulk.

The oxide was found to be necessary to relieve stress caused by a mismatch between the linear thermal expansion coefficients of silicon and silicon nitride. When silicon nitride was deposited directly on silicon and the wafer was heated, a large drop in effective lifetime resulted. This was not recovered by removal of the nitride and re-passivation of the surface nor was the damage limited to within a few microns of the surface.
Figure 5.4: The effect of no oxide layer beneath a nitride during a nitrogen anneal. All curves are for wafers after: oxide/nitride stack formation (37nm of nitride, oxide thickness indicated in the legend), nitrogen anneals (for 1 hour each at 900°C and 1000°C), oxide/nitride stack removal, growth of a second, 150nm thick oxide and 400°C FGA. The top three curves are for wafers that did have an oxide under the nitride. (These wafers are the same as those shown in figure 5.2). The bottom curve is for a wafer that did not have an oxide underneath the nitride.
Figure 5.5: The depth of damage caused by a nitrogen anneal for a wafer with nitride and no oxide. Effective lifetime curves are shown for the wafer after light phosphorous diffusion, oxidation and 400°C FGA (stars), after oxide strip and nitride deposition (x), after nitrogen anneal for 1 hour at 1000°C (□) and after nitride removal, growth of a second oxide, oxide removal, removal of 12μm of silicon from each side, a second light phosphorous diffusion, growth of a 25nm thick oxide and 400°C FGA (o).
Figure 5.6: An oxide/nitride stack showing the four regions that are significant in the hydrogen loss model.

5.4 Hydrogen Loss Model

The effect of annealing a wafer with an oxide/nitride stack in a high temperature nitrogen ambient is on the surface, not on the silicon bulk, and can therefore be characterised by the effect it has on emitter saturation current, $J_{oc}$, provided wafers have a diffusion. This section introduces a model, developed using evidence both from the literature and experiments, to explain the effect of high temperature nitrogen anneals on wafers with an oxide/nitride stack. The essence of the model is that during an anneal in nitrogen, hydrogen is removed from the silicon interface, resulting in an increase in the density of unpassivated sites, and therefore an increase in surface recombination. To introduce the model, consider the four sections of an oxide/nitride stack on silicon, as shown in figure 5.6. These sections are: the silicon nitride, which is the outermost layer, and in direct contact with the nitrogen ambient; the silicon oxide, which acts as an intermediate layer between the silicon and the silicon nitride; the silicon/silicon oxide interface and the silicon bulk.

5.4.1 The Silicon Bulk

Hydrogen diffuses readily in crystalline silicon [35]. It can be both beneficial, in that it is able to passivate defects, and detrimental, in that it can induce defects [94]. Much is still unknown about the behaviour of hydrogen in silicon, which has been described as ‘anything but simple’ [64]. At elevated temperatures, molecular hydrogen is known to dissociate into monatomic species in intrinsic silicon and it forms complexes with acceptors, donors and probably itself. Both the $\text{H}^+$ and $\text{H}^-$ forms have been shown to be stable and highly mobile in silicon [148].

Even with intrinsic silicon, the diffusion coefficient of atomic hydrogen remains under
debate and in the medium temperature range (300–1000K) estimates vary from experiment to experiment and from experiment to theory by more than two orders of magnitude [35]. Diffusion is known to be influenced by impurities, defects and, at lower temperatures, quantum effects [35, 301]. At temperatures above 1000K, there is closer agreement between theory and experiment.

The most extensive experimental data available for temperatures above 1000K was published in 1956 by Wieringen and Warmoltz [348]. Diffusion rates were measured in the temperature range 1092–1200°C for what is now thought to have been H⁺ ions. A reasonable Arrhenius fit to these results was obtained using a simulation developed by Boucher and DeLeo [64]. The simulation uses temperatures from 1050K to almost 2000K. The simulated results give $D_0 = 9.41 \times 10^{-3} \text{cm}^2/\text{s}$ and $E_A = 0.45\text{eV}$ in the equation:

$$D(T) = D_0 \exp\left(-\frac{E_A}{k_BT}\right).$$

This results in a diffusion coefficient for atomic hydrogen in silicon of $8.0 \times 10^{-5} \text{cm}^2/\text{s}$ at 900°C and $11.4 \times 10^{-5} \text{cm}^2/\text{s}$ at 1000°C.

Since, at elevated temperatures, the diffusion rate of hydrogen from an LPCVD silicon nitride into the silicon bulk is only a few percent of the diffusion rate into the gas ambient [20], the passivation of bulk defects in the silicon by heating an oxide/nitride stack on silicon is unlikely.

For the purposes of this model, the silicon bulk is a region in which hydrogen diffuses readily. It is not a source of hydrogen and it does not benefit from the out-diffusion of hydrogen originally in the nitride.

### 5.4.2 The Silicon/Silicon Oxide Interface

A thermally grown oxide provides good surface passivation as many of the dangling bonds at the silicon surface are terminated by oxygen atoms. Nevertheless, a number of un-passivated sites remain. The configuration of these sites and their densities depends on the crystallographic orientation of the silicon surface. The sites create energy states in the forbidden energy gap that can act as recombination sites. Many of these sites can be passivated by hydrogen, which may be introduced in atomic or molecular form. Atomic hydrogen is thought to be more effective at passivation and excellent surface passivation has been demonstrated by annealing (depositing a thin layer of aluminium and annealing at approximately 400°C) wafers with a thin oxide [179] and by depositing a plasma silicon nitride layer [1]. Both of these methods are thought to provide atomic hydrogen at the silicon interface.
On a bare silicon surface, there are 10 dangling bonds per unit cell face for (100) orientated silicon and 6 for (111) orientated silicon [151]. At a silicon/silicon oxide interface, the exact nature of defects is not well known. Until recently, the only positively identified defect at a (111) silicon/oxide interface was the ‘P₆’ centre [236]. P₆ centres are a dangling bond on a silicon atom that is attached to three other silicon atoms, i.e., they are of the form: oSi ≡ Si₃. P₆ centres can be passivated by molecular hydrogen and have a surface density of approximately 1×10¹³/cm² [297]. The P₆ centre was initially reported to have a single activation energy of 1.66eV [78]. Later it was found to have, not a single activation energy, but a Gaussian spread (of 0.06eV) around a mean activation energy of 1.51eV [298].

At a (100) silicon/oxide interface there are two centres similar to the P₆ centre, termed P₆₀ and P₆₁. They also have a non-singular activation energy. A Gaussian spread of approximately 0.14 and 0.15eV and mean activation energies of 1.51 and 1.57±0.3eV have been calculated for the P₆₀ and P₆₁ centres respectively [297]. The density of these defects and their exact configuration has not been determined.

Recently, Georghita and Ogryzlo [122] published details of a second type of defect that occurs at a (111) silicon/oxide interface [122]. They called this the ‘R’ centre and again, the exact configuration is not known. Approximately 54% of the defects at a (111) silicon/oxide interface were found to be P₆ centres and 27% were found to be R centres. The P₆ and R centres could be passivated by molecular hydrogen at temperatures up to 280°C, unlike the remaining 19% of defects [122].

For the purposes of this model, it is sufficient to consider the silicon interface to contain a number of dangling bonds that may be passivated by hydrogen from a molecular or atomic source. At elevated temperatures, hydrogen bonds are broken and hydrogen will diffuse away from the interface, leaving unpassivated defect states. Unless the hydrogen is replaced, there will be a corresponding rise in surface recombination velocity, which will result in a rise in the surface recombination rate. The magnitude of this rise is dependent on the details of the high temperature step and on the sensitivity of the surface to hydrogen loss. The sensitivity of the surface to hydrogen loss is influenced by the wafer orientation and the sheet resistance of the surface diffusion.

### 5.4.3 The Silicon Oxide

Molecular hydrogen is known to diffuse readily through oxide at temperatures as low as 135°C [122] and oxide is unlikely to act as a diffusion barrier to either molecular or atomic hydrogen [20]. In the absence of a barrier layer, passivation of a silicon/oxide interface with molecular hydrogen at low temperatures is reaction rate limited, not diffusion limited.
After deposition of an LPCVD silicon nitride layer on a thermally grown oxide on silicon, there is very little hydrogen in the underlying oxide [134].

For the purposes of the model, the effect of the oxide is three-fold. Firstly, the oxide provides some passivation at the silicon/oxide interface. Secondly, small amounts of hydrogen, originally from either the nitride or the silicon/oxide interface, may remain in the oxide after a high temperature step. During a lower temperature step, hydrogen in the oxide is mobile and may move to and passivate the silicon/oxide interface. Experimental evidence in support of this suggestion is given in the first half of section 5.8.

Thirdly, the oxide is necessary to protect the silicon wafer against stresses exerted by the silicon nitride. With no oxide, the bulk lifetime of the wafer is reduced by nitride deposition and high temperature anneal. With a very thin oxide, some strain is exerted on the wafer surface. This introduces surface states, which may be passivated by molecular hydrogen or possibly annealed out at elevated temperatures. Experimental evidence in support of this suggestion is given in the second half of section 5.8.

5.4.4 The Silicon Nitride

The silicon nitride is not in contact with the silicon surface and therefore does not directly provide atoms to terminate dangling bonds at this site. The nitride is an intermediate layer between the silicon oxide and the ambient gas and so can act as a diffusion barrier to hydrogen. The role of the nitride is complicated because an as-deposited LPCVD nitride contains some hydrogen, typically between 2–10 atomic% [134, 295, 296]. The majority (70–80%) of the bonded hydrogen is contained in N–H bonds and the remainder in Si–H bonds [20]. This section discusses firstly the removal and secondly the re-introduction of hydrogen to a nitride layer. Although this section is concerned with the hydrogen concentration levels in the nitride, the measurements of $J_\infty$ presented in this thesis reflect the hydrogen concentration at the silicon interface. Hydrogen levels in the nitride are important because, in order to reach the silicon interface from the ambient, hydrogen must first pass through the nitride. The amount of hydrogen required to achieve good passivation of the silicon surface is considerably less than is available in the nitride immediately after deposition.

When an LPCVD silicon nitride layer is subjected to high temperatures in a vacuum or inert gas ambient, the amount of hydrogen in the nitride layer decreases [20, 134, 349]. Most of the hydrogen is lost into the ambient. The diffusion rate into the silicon bulk is thought to be only a few percent of the diffusion rate into the gas ambient [20, 134]. In an LPCVD silicon nitride, hydrogen loss is thought to occur by the diffusion of bonded hydrogen within the nitride to the surface regions and subsequent desorption [20]. Si–H
Hydrogen Loss Model

<table>
<thead>
<tr>
<th>Ambient</th>
<th>Anneal time</th>
<th>Anneal temperature</th>
<th>Hydrogen content</th>
</tr>
</thead>
<tbody>
<tr>
<td>As deposited</td>
<td>–</td>
<td>–</td>
<td>3 atomic %</td>
</tr>
<tr>
<td>Vacuum</td>
<td>1.5 hours</td>
<td>900°C</td>
<td>1.9 atomic %</td>
</tr>
<tr>
<td>Vacuum</td>
<td>1.5 hours</td>
<td>1000°C</td>
<td>0.4 atomic %</td>
</tr>
<tr>
<td>7%H₂ in N₂</td>
<td>1 hour</td>
<td>1000°C</td>
<td>1.6 atomic %</td>
</tr>
</tbody>
</table>

Table 5.2: Hydrogen content of an LPCVD nitride after various high temperature anneals from Habraken et al. [134].

bonds in an LPCVD silicon nitride break above temperatures of 800°C and N–H bonds at higher temperatures [134]. The hydrogen concentration as a function of nitride thickness is uniform after deposition and remains so after annealing in a nitrogen or hydrogen-containing ambient. For hydrogen loss from an LPCVD silicon nitride, the rate limiting step was determined to be the breaking of N–H bonds and the diffusion coefficient was found to be between $1.5 \times 10^{-17}$ and $6.5 \times 10^{-14}$ cm²/s for temperatures between 700 and 1000°C. Table 5.2 shows the hydrogen concentrations that were measured in an LPCVD silicon nitride after various high temperature anneals.

Hydrogen can be re-introduced to an LPCVD nitride. The rate of re-introduction of atomic hydrogen has been determined to increase only slightly in the temperature range 800–1000°C [20]. The diffusion rate of atomic hydrogen in nitride has been found to be dependent on the thermal history of the wafer [20]. The diffusion coefficient at 900°C was measured to be $0.7 \times 10^{-14}$ cm²/s in as-deposited silicon nitride and $0.2 \times 10^{-14}$ cm²/s in a nitride that had been previously annealed at 900°C. The reason suggested for this was the lower number of available sites due to an increased number of Si–N and N–N bonds following the high temperature nitrogen anneal [20, 97]. For the purposes of this work, the molecular hydrogen that diffuses through the nitride and oxide to the silicon/oxide interface is also of importance. No literature was found on this topic.

For the purposes of this model, the silicon nitride has two roles. Firstly, it acts as a diffusion barrier to hydrogen at low temperatures. At higher temperatures, hydrogen may diffuse through the nitride and oxide to passivate the silicon interface. Diffusion probably occurs as both atomic and molecular hydrogen. The diffusion rate of atomic hydrogen is influenced by the thermal history of the wafer, the temperature and the concentration of hydrogen in the ambient. Secondly, the nitride acts as a limited hydrogen source and hydrogen from the silicon nitride may diffuse towards the substrate and passivate the silicon interface. For anneals in a nitrogen ambient, most of the hydrogen in the nitride diffuses out into the gas ambient.
5.5 The Effect of Nitrogen Anneal Temperature on $J_{oe}$

To determine the effect of the temperature of the nitrogen anneal on $J_{oe}$ for wafers with an oxide/nitride stack, eight wafers were prepared as described in table 5.1. The emitter sheet resistance immediately after light phosphorous diffusion was $\sim 930 \Omega/\square$ and oxide thicknesses were 100, 150, 225 and 310nm. Two nitride thicknesses were used, 14 and 24nm. Nitrogen anneals were done for 60 minutes at $750^\circ C$–$1000^\circ C$ in $50^\circ$ increments. The same wafers were used for each high temperature step and so the effect of the nitrogen anneals is cumulative.

Figure 5.7 shows $J_{oe}$ values for the wafer with 100nm of oxide and 24nm of nitride. These results suggest that higher nitrogen anneal temperatures resulted in higher $J_{oe}$ values. As the same wafer was used for each step, the results could also imply that a longer time in a nitrogen ambient results in an increase in $J_{oe}$. The same trend was seen with all eight wafers. Also shown in figure 5.7 are the results for a separate batch of wafers with 100nm of oxide and no nitride. Four wafers were used for this experiment and annealed at 800, 900, 950 and 1000$^\circ$C. The ‘oxide’ measurement is an average of the initial $J_{oe}$ values after light phosphorous diffusion, oxidation and 400$^\circ$C FGA for all four wafers.

The results shown in figure 5.7 can be understood within the context of the hydrogen loss model. The increase in $J_{oe}$ that occurred with a nitrogen anneal may be attributed to a loss of hydrogen from the silicon interface. Hydrogen bonds at the silicon interface were more stable at lower temperatures. As the temperature was increased, more hydrogen bonds were broken and hydrogen diffused away from this region. Replacement hydrogen was not available from the gas ambient during a nitrogen anneal and so the net amount of hydrogen at the interface decreased. A similar increase in $J_{oe}$ was not seen for wafers with an oxide only. For these wafers, sufficient hydrogen supply probably came from the trace quantities of water vapour in the nitrogen lines.

The effect of nitrogen anneal temperature on wafers with an oxide/nitride stack is, in general, further complicated because the nitride is itself a limited source of hydrogen. This is discussed in section 5.7.

5.6 The Effect of Nitrogen Anneal Time on $J_{oe}$

The nitrogen anneals typically used for the results discussed in this thesis were done for 60 minutes. Such long, high temperature steps may be avoided in solar cell production if rapid thermal processing (RTP) is used. RTP is potentially advantageous in commercial cell processing due to a lower thermal budget and because it allows continuous, or ‘in-line’
Figure 5.7: The effect of the temperature of the nitrogen anneal on $J_{oe}$ for a wafer with 100nm of oxide underneath 24nm of nitride compared with the effect on wafers with a 100nm thick oxide and no nitride. The ‘oxide’ measurement was made after light phosphorous diffusion, oxide growth and FGA. The ‘nitride’ measurement was made immediately after nitride deposition. For the wafers with a nitride, nitrogen anneals were done for 1 hour at each temperature, so the effect is cumulative.
processing to be done. In this section, the effect of both RTP and shorter nitrogen anneals in a conventional, quartz-tube furnace on $J_{oe}$ are discussed.

### 5.6.1 Conventional Furnace Processing

Figure 5.8 shows the effect of the time duration of a 900°C nitrogen anneal on $J_{oe}$. These wafers had an oxide thickness of 150nm and a nitride thickness of 33nm. Nitrogen anneals were done for 15, 30, 45 and 60 minutes for four separate wafers. The results shown in this figure show that as the nitrogen anneal time was increased, $J_{oe}$ also increased. For these wafers, $J_{oe}$ was essentially at a maximum after approximately 45 minutes. Two of the wafers were given further anneals to a total of 120 minutes to confirm this. Other results discussed in this chapter suggest that the saturation time is dependent on oxide and nitride thickness and on anneal temperature.

The wafer that had been annealed in nitrogen for 15 minutes was given another three 15 minute nitrogen anneals (each with a half hour FGA at 400°C). This wafer had then

![Figure 5.8: The effect of nitrogen anneal time (at 900°C) on $J_{oe}$. Four wafers were used in this experiment and annealed in nitrogen for 15, 30, 45 or 60 minutes. The $J_{oe}$ value shown for 0 minutes, is an average of the $J_{oe}$ of the four wafers after oxide/nitride stack formation. There are two 120 minute results, one for the 60 minute wafer, which had a second 60 minute nitrogen anneal, and the other for the 15 minute wafer, which had a further 3 15 minute nitrogen anneals and then a single 60 minute nitrogen anneal. All of these wafers had a 150nm thick oxide and a 33nm thick nitride. The emitter sheet resistance after phosphorous diffusion was 730Ω/□.](image-url)
spent a total of 1 hour in nitrogen at 900°C. The $J_{oe}$ was $\sim 1600 \text{fA/cm}^2$/side, which was similar to that of the wafer that underwent a single, 1 hour, nitrogen anneal at 900°C ($\sim 2600 \text{fA/cm}^2$/side). This result suggests that the total time spent at any one temperature determines the increase in $J_{oe}$. Consequently, high temperature treatments could not be done as a series of short steps in preference to a single, longer step.

5.6.2 Rapid Thermal Processing

To test the effect of very short anneal times, two wafers were given an RTP treatment. The approximate thermal profile is shown in figure 5.9. Wafers were held for two minutes in a nitrogen ambient at 900 or 1000°C. The wafers had a 25nm thick oxide and a $\sim 30$nm thick nitride. Two minutes was chosen for the processing time as this is ample time in which to do a phosphorous diffusion [55]. The emitter sheet resistance of the wafers after phosphorous diffusion was $1350 \Omega/\square$.

$J_{oe}$ values after RTP are compared with those of wafers that had a nitrogen anneal in a conventional quartz tube furnace in table 5.3. The $J_{oe}$ values after RTP were significantly lower than those for the wafers that were annealed in nitrogen for 1 hour in a conventional, quartz tube furnace. The result for the 1000°C RTP is probably too high to be useful for most cell applications. After 2 minutes at 900°C, however, $J_{oe}$ had increased only slightly, and low temperature rapid thermal processes in conjunction with an oxide/nitride stack shows promise as a processing technique. The 900°C RTP result can not be directly

![Figure 5.9: Approximate thermal profile for the wafers during RTP. The furnace was flushed with nitrogen at 5l/min for the first 180s, after which the flush rate was reduced to 2l/min for the remainder of the process. Two RTP temperatures were used; 900 and 1000°C. The time required to reach temperature was 8 or 9s for the 900 and 1000°C cases respectively. The time spent at temperature was 120s in both cases.](image-url)
Table 5.3: $J_{oc}$ values for wafers after RTP compared with wafers that had a nitrogen anneal in a conventional quartz tube furnace (CQTF). Sheet resistances were measured after light phosphorous diffusion. The $J_{oc}$ values for all wafers after oxide/nitride stack formation were in the range 14–22$fA/cm^2/side$.

<table>
<thead>
<tr>
<th>Process</th>
<th>Oxide/Nitride thickness (nm)</th>
<th>$R_{sheet}$ $(\Omega/\square)$</th>
<th>Time (minutes)</th>
<th>Temperature $(^\circ C)$</th>
<th>$J_{oc}$ $(fA/cm^2/side)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTP</td>
<td>25/30</td>
<td>1350</td>
<td>2</td>
<td>900</td>
<td>55</td>
</tr>
<tr>
<td>RTP</td>
<td>25/30</td>
<td>1350</td>
<td>2</td>
<td>1000</td>
<td>1660</td>
</tr>
<tr>
<td>CQTF</td>
<td>25/30</td>
<td>1050</td>
<td>60</td>
<td>900</td>
<td>930</td>
</tr>
<tr>
<td>CQTF</td>
<td>25/30</td>
<td>1050</td>
<td>60</td>
<td>1000</td>
<td>4250</td>
</tr>
</tbody>
</table>

compared with the values shown in figure 5.8 because the oxide thickness and emitter sheet resistivity were significantly different.

5.6.3 Summary: Nitrogen Anneal Time

The results discussed in this section are consistent with the hydrogen loss model; as the amount of time a wafer spent at high temperature was increased, more hydrogen was lost from the silicon interface and so $J_{oc}$ values increased.

5.7 The Effect of Nitride Thickness on $J_{oc}$

This section discusses the effect of nitride thickness on $J_{oc}$ for wafers with an oxide/nitride stack that underwent a high temperature nitrogen anneal. Figure 5.10 shows $J_{oc}$ values after a 1 hour, 900$^\circ C$ nitrogen anneal for wafers with 25 and 225nm thick oxides. These results show that for both oxide thicknesses, thicker nitrides resulted in a much lower $J_{oc}$ after nitrogen anneal. Figure 5.11 shows results for the same wafers after an additional 1 hour, 1000$^\circ C$ nitrogen anneal. For the wafers with the 225nm thick oxide, the nitride thickness appeared to have no influence on $J_{oc}$. For the wafers with the 25nm thick oxide, there was a slight increase in $J_{oc}$ with increasing nitride thickness.

The observation that a thicker nitride resulted in a lower $J_{oc}$ for a 900$^\circ C$ nitrogen anneal can be explained by considering the nitride as a limited hydrogen source. At high temperatures, bonded hydrogen in the silicon nitride was released and while most of the hydrogen diffused out into the gaseous ambient, a small amount diffused towards the silicon interface. With thicker nitrides, there was a greater total amount of hydrogen and therefore a greater chance of passivation at the silicon interface after the wafer had cooled from the nitrogen anneal. After the 1000$^\circ C$ nitrogen anneal, the results imply that all available hydrogen in the nitride had been removed and so $J_{oc}$ was relatively independent of nitride thicknesses. The slight increase in $J_{oc}$ with increasing nitride thickness for the
Figure 5.10: The effect of nitride thickness on $J_{oe}$ for a 60 minute 900°C nitrogen anneal. Oxide thicknesses were 25 and 225nm, and are indicated in the legend. $J_{oe}$ values for these wafers after oxide/nitride stack formation were 8–22fA/cm²/side. The emitter sheet resistance after diffusion was 1040Ω/□ for the wafers with the 25nm thick oxide and 560Ω/□ for the wafers with the 225nm thick oxide. After oxidation, these would have reduced to approximately 590 and 370Ω/□, respectively.

Figure 5.11: The effect of nitride thickness on $J_{oe}$ for a 60 minute 1000°C nitrogen anneal. Oxide thicknesses were 25 and 225nm, and are indicated in the legend. $J_{oe}$ values for these wafers after oxide/nitride stack formation were 8–22fA/cm²/side. These wafers are the same as those shown in figure 5.10.
wafers with the thin oxide and 1000°C nitrogen anneal may be due to the formation of additional ‘surface states’, which are discussed in the next section.

The wafers shown in figure 5.10 were processed in two separate batches (divided by oxide thickness). It is not rigorous to use these figures to compare results for different oxide thicknesses. Such cross-batch comparisons are tenuous at best, especially in this case where the anneal temperature was only 900°C. At this temperature, small amounts of hydrogen may have remained in the oxide/nitride stack system and the amount that remained would be different for the two batches depending on the surface roughness and the cooling rate after anneal. Results for both oxide thicknesses are included to illustrate that a similar dependence of $J_{oe}$ on the nitride thickness occurs for a range of oxide thicknesses. For the results shown in figure 5.11, the anneal temperature was much higher and most of the hydrogen had probably been removed from the system, so cross-batch comparisons are more acceptable.

### 5.8 The Effect of Oxide Thickness on $J_{oe}$

Figure 5.12 shows $J_{oe}$ values as a function of oxide thickness for four wafers that were processed in the same batch. The wafers were annealed for 1 hour at 50°C intervals between 750–1000°C and the $J_{oe}$ values after anneals at 750, 800, 850 and 1000°C are shown in this figure. The two wafers with the thicker oxides clearly show a lower $J_{oe}$ than the wafers with the thinner oxides, especially after the anneals at lower temperatures. After the anneal in nitrogen at 1000°C, for this range of oxide thicknesses, there is not a clear effect of nitride thickness. A slight complication of these results is that the oxides were grown separately, which means that the diffusion profiles of the wafers were slightly different. The oxidations were all done at the same temperature (1100°C), which would have limited the variation, but the time was varied. Retrospectively, it would have been more rigorous to use nitrogen anneals to ensure that all wafers were subjected to the same thermal profile. A second option would have been to grow all the oxides in a single step and selectively thin the oxides, but this may have introduced pinholes.

Figure 5.13 shows the effect of a 400°C anneal in forming gas on $J_{oe}$ after 900°C nitrogen anneals for 15, 30, 45 and 60 minutes. For all nitrogen anneal times shown in figure 5.13, a 30 minute anneal in forming gas at 400°C resulted in a drop in $J_{oe}$ and the effect was greater after shorter nitrogen anneals. The same result was seen when the 400°C forming gas anneal was replaced with a 400°C nitrogen anneal, and is therefore related to the temperature rather than the gas composition. These results may be explained by assuming that one way in which the oxide thickness may affect $J_{oe}$ after a high temperature
Figure 5.12: $J_{oe}$ as a function of oxide thickness for 1 hour anneals in nitrogen at 750, 800, 850 and 1000°C. The anneal temperature is shown in the legend. These wafers had a 24nm thick nitride.

The results shown in figure 5.13 suggest that, in cases where hydrogen is still present in the system, the wafer cooling rate is important. The cooling rate is influenced by the withdrawal rate of the wafers from the furnace and the time spent at the mouth of the furnace before final unloading.

Figure 5.14 shows the effect on $J_{oe}$ values of oxide and nitride removal with repassivation compared with removal of the nitride only. The wafer shown in this figure initially had an oxide/nitride stack (O/N 1), formed by deposition of an LPCVD nitride on a thermally oxidised wafer, at which point the $J_{oe}$ value was low, as expected. The wafer was then annealed in nitrogen at elevated temperatures, including 1 hour at 1000°C (NA 1), after which the $J_{oe}$ was again high, as expected. The oxide/nitride stack was removed and a second oxide was grown and nitride deposited (O/N 2). $J_{oe}$ had recovered to approximately the initial value at this stage. The wafer was then annealed in nitrogen for 1 hour at 1000°C, and $J_{oe}$ was again very high. The nitride (but not the oxide) was
Figure 5.13: The effect of a 400°C FGA, after a 900°C nitrogen anneal, on wafers with an oxide/nitride stack as a function of anneal time. Four wafers were used in this experiment and annealed in nitrogen at 900°C for 15, 30, 45 or 60 minutes. The $J_{oc}$ value shown for 0 minutes is an average of the $J_{oc}$ of the four wafers after oxide/nitride stack formation. All of these wafers had a 150nm thick oxide and a 33nm thick nitride.

then removed in orthophosphoric acid. At this point, $J_{oc}$ remained high, implying that the orthophosphoric acid etch did not re-introduce any hydrogen to the silicon interface. The wafer was given a 400°C FGA and $J_{oc}$ decreased. If the high $J_{oc}$ values after high temperature nitrogen anneal of a wafer were due only to a lack of hydrogen then the $J_{oc}$ at this stage (‘FGA 0.5’ in figure 5.14) should be approximately equal to the values at ‘O/N 1’ and ‘O/N 2’. The fact that it is slightly higher, 30fA/cm$^2$/side, compared with 11 and 12fA/cm$^2$/side after oxide/nitride stack formation, may be explained if additional ‘surface states’ were created by the high temperature nitrogen anneals. The oxide was thinned (from 150nm to 125nm), to ensure that the higher $J_{oc}$ was not due to nitride remaining on the wafer. $J_{oc}$ had a very slight decrease after this step. After further forming gas anneals, for 4 and then 3 hours, $J_{oc}$ continued to decrease, suggesting that the surface states were passivated with molecular hydrogen at 400°C or that they were ‘annealed out’ during a 400°C anneal. A second way in which oxide thickness may affect $J_{oc}$ after a high temperature anneal is therefore to influence the introduction of surface states. The surface states may be strain induced, due to the mismatch in linear thermal expansion coefficients for silicon and silicon nitride.

The introduction of surface states may also explain the higher $J_{oc}$ values for the wafers with the thinner oxides and the slight increase in $J_{oc}$ with increasing nitride thickness after
Figure 5.14: The effect of nitride removal on $J_{\text{ne}}$. ‘O/N 1’ and ‘O/N 2’ were the first and second oxide/nitride stacks, respectively. The first stack was a 100nm thick oxide and a 37nm thick nitride. The second was a 150nm thick oxide and a 43nm thick nitride. ‘NA 1’ and ‘NA 2’ were the first and second nitrogen anneals, respectively. The first was several high temperature steps, including 1 hour at 1000°C. The second nitrogen anneal was done for 1 hour at 1000°C. ‘NS’ was the nitride strip, in hot orthophosphoric acid. ‘OT’ was an oxide thin, done using 10% HF solution in water (~ 25μm of silicon oxide was removed). ‘FGA 0.5’, 4 and 3 were all 400°C FGA done for 0.5, 4 and 3 hours, respectively.

In conclusion, oxide thickness may influence the $J_{\text{ne}}$ that results from a high temperature nitrogen anneal of a wafer with an oxide/nitride stack in two ways. Firstly, some hydrogen may remain in the oxide. As the wafer cools or during a lower temperature anneal, this hydrogen may diffuse to and passivate the silicon interface. Secondly, a thin oxide may allow the introduction of additional surface states. The surface states were shown to be either passivated with molecular hydrogen or annealed out at high temperatures.

5.9 Recovery after High Temperature Nitrogen Anneal

The essence of the hydrogen loss model is that, for wafers with an oxide/nitride stack, during a high temperature nitrogen anneal, hydrogen bonds at the silicon interface are broken and hydrogen diffuses away from this region. Surface passivation cannot be recovered with a standard, 400°C FGA because the silicon nitride acts as a hydrogen diffusion barrier at this temperature. The wafer bulk is not damaged during nitrogen anneal. It should,
therefore, be possible to recover $J_{oc}$ values by re-introducing hydrogen to the silicon/oxide interface. This section discusses recovery of the wafers, firstly by nitride removal and secondly by hydrogen re-introduction.

### 5.9.1 Recovery by Nitride Removal

The most drastic measure that may be taken to recover effective lifetimes after degradation with a nitrogen anneal is to strip both the oxide and nitride and re-grow a second passivating oxide. As nitride deposition does not alter effective lifetime if the wafer is not heated, a second nitride may also be deposited to obtain a good ARC. The growth of a second oxide was demonstrated in section 5.3. A more practical method of lifetime recovery is to strip the nitride only. This can be done in hot (165°C) orthophosphoric acid. Figure 5.14 shows $J_{oc}$ values for a wafer that has been recovered using both methods. These results show that $J_{oc}$ was recovered by significantly stripping the nitride and giving the wafer a 30 minute 400°C FGA. Further thinning of the oxide had negligible effect on $J_{oc}$ but $J_{oc}$ decreased again after longer forming gas anneals.

### 5.9.2 Recovery by Hydrogen Reintroduction

$J_{oc}$ recovery was attempted using a 30 minute forming gas anneal at 840°C. The result is shown in figure 5.15, and the wafer had a 100nm thick oxide and a 33nm thick nitride. The nitrogen anneal was done at 900°C for 60 minutes. As expected, the effective lifetime for the wafer with light phosphorous diffusion and oxide/nitride stack was initially high but dropped after nitrogen anneal. Following an anneal in forming gas at 840°C, the effective lifetimes were completely recovered and actually slightly higher than those of the wafer immediately after oxide/nitride stack formation. These results strongly support the hypothesis that the drop in effective lifetime for wafers with an oxide/nitride stack following high temperature anneal was due to a drop in surface passivation which in turn was due to a loss of hydrogen from the silicon interface.

### 5.10 Conclusions

High temperature anneals in nitrogen of wafers with an oxide/nitride stack caused a drop in effective lifetime. This was shown to be due to a loss of hydrogen from the silicon interface. The presence of the silicon nitride did not cause significant irreversible damage to the wafer when an oxide/nitride stack on silicon was heated, in cases where the oxide thickness was 25nm or greater. The presence of the oxide was necessary to reduce damage, probably caused by stress due to the mismatch in coefficients of linear thermal expansion.
Figure 5.15: Effective lifetime recovery using an 840°C FGA. Lifetime curves for a wafer after light phosphorous diffusion and oxide/nitride stack formation (□), nitrogen anneal at 900°C for 60 minutes (x) and after a 30 minute forming gas anneal at 840°C (○). The oxide was 100nm thick and the nitride 33nm thick. The $J_{oc}$ values were 15, 1510 and 9fA/cm²/side after oxide/nitride stack formation, nitrogen anneal and recovery in forming gas, respectively. The corresponding implied $V_{oc}$ values were 694, 592 and 706mV.
between silicon and silicon nitride. Considerable permanent damage occurred to the wafer if an oxide was not interposed between the nitride and the silicon and the wafer was heated. Complete recovery of the effective lifetime (after a 60 minute nitrogen anneal at 900°C) was demonstrated for a wafer with a 100nm thick oxide and 33nm thick nitride using a 30 minute forming gas anneal at 840°C.

A hydrogen loss model has been developed to explain the behaviour of oxide/nitride stacks during a high temperature step. The essence of this model is that when a wafer with an oxide/nitride stack was subjected to high temperatures in an inert gas ambient, there was a loss of hydrogen from the silicon interface. The effect was found to be greater with higher temperatures or longer times. Thicker oxides provided some protection against hydrogen loss for two reasons. Firstly, some hydrogen remained in the oxide at the end of a nitrogen anneal and this was free to diffuse as the wafer cooled. The amount of hydrogen that remained in the oxide was dependent on anneal temperature and time. It was probably insignificant after a 1000°C nitrogen anneal for all oxide thicknesses used in this work. Secondly, the oxide mediated strain on the silicon surface caused by the nitride. This strain resulted in surface states, which could be passivated by molecular hydrogen or annealed out at high temperatures. A thicker oxide resulted in less strain. Thicker nitrides resulted in less increase in $J_{oc}$ with a 900°C nitrogen anneal because the nitride acted as a limited hydrogen source.

The broader implications of this work are that in order to take advantage of the physical and chemical properties of the nitride layer and therefore deposit the nitride in the early stages of cell fabrication, an additional recovery step must be added to any cell processing sequence. Methods of possible hydrogen re-introduction through an oxide/nitride stack after nitrogen anneal are discussed in the next chapter.
For the oxide/nitride stack on silicon shown in figure 5.15, the drop in effective lifetime that occurred during a nitrogen anneal was shown to be reversible by re-introducing hydrogen using a high temperature forming gas anneal. This chapter discusses various methods of hydrogen re-introduction, assessed by comparing emitter saturation current, $J_{\text{oe}}$, values. There is an emphasis on high temperature forming gas anneals. Recovery of $J_{\text{oe}}$ values was also attempted using hydrogen plasmas, alneals, wet oxidations and second LPCVD depositions. The time necessary for successful $J_{\text{oe}}$ recovery was shown to be dependent on the nitride thickness and on the temperature of the nitrogen anneal. The most successful method of hydrogen re-introduction was a high temperature forming gas anneal. In this case, $J_{\text{oe}}$ recovery was demonstrated after nitrogen anneals at both 900 and 1000°C and with an optimised anti-reflection coating. The plasma methods showed promise.

### 6.1 Introduction

In order to use an oxide/nitride stack on silicon, formed in the early stages of cell fabrication, for solar cell applications, the increase in emitter saturation current, $J_{\text{oe}}$, that occurs during a high temperature step must be addressed. Since the increase is apparently due to a loss of hydrogen from the silicon interface, a logical way to recover $J_{\text{oe}}$ values is to re-introduce hydrogen to the silicon interface. In this chapter, recovery was attempted using both atomic and molecular hydrogen.

Hydrogen re-introduction was attempted using five different methods; high temperature forming gas anneals (FGA), alneals, immersions in a hydrogen plasma, second LPCVD depositions and wet-oxidations. Table 6.1 shows the temperatures and times necessary for each hydrogen re-introduction method. In each case, the oxide and nitride thickness was varied, and recovery was attempted after nitrogen anneals at both 900°C and 1000°C.
Table 6.1: Hydrogen re-introduction experiments. The ‘time’ column refers to the time spent at high temperature. In the case of the alneal significant time was also required to deposit and strip the aluminium, but this was not done at high temperature.

Of the five methods of hydrogen re-introduction attempted, four are standard processing techniques; namely PECVD nitride deposition, LPCVD nitride deposition, wet oxidation and alneal. Although a 400°C FGA is a standard processing technique, higher temperature FGA are not standard. This chapter therefore includes an additional section that discusses the effect of high temperature FGA on wafers with an oxide only. The aim of this section was to establish a baseline effect of high temperature FGA on wafers with an oxide only before assessing the effect of high temperature FGA on wafers with an oxide/nitride stack.

The high temperature FGA is a source of molecular hydrogen, while the other four treatments were all hoped to be sources of atomic hydrogen. This is a significant difference because atomic hydrogen may be able to diffuse through the nitride faster than molecular hydrogen. Conversely, the diffusion of atomic hydrogen through the nitride may be slower as it reacts more readily with the nitride. Atomic hydrogen is generally able to provide excellent surface passivation on a silicon surface, as demonstrated with an alneal or a PECVD nitride passivation [1, 179].

6.2 Experimental Conditions

The wafers used for this work were 100–400Ωcm, (100) orientated, p-type FZ. They were prepared in the same way as the wafers discussed in the previous chapter, with the addition of an attempted hydrogen re-introduction step after the nitrogen anneal. Wafer preparation is summarised in table 6.2. Note that the passivating diffusion remains very light in order to increase the sensitivity to surface passivation.

6.3 High Temperature FGA: Wafers with an Oxide Only

This section discusses the effect of high temperature forming gas anneals on wafers with an oxide only. The intention was to determine a baseline effect, and therefore place in
### Table 6.2: Processing steps for the wafers discussed in this chapter. The starting material was 100–400Ω·cm, (100) orientated, p-type FZ. The lifetime measurements were used to determine the effect of the previous steps on the wafer.

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Saw damage etch</td>
<td>1:10 HF:HNO₃ To remove approximately 20μm from each side (usually ~5 minutes).</td>
</tr>
<tr>
<td>2</td>
<td>RCA (Radio Corporation America) clean</td>
<td>10 minutes in a 5:1:1 H₂O:NH₃:H₂O₂ solution plus 10 minutes in a 5:1:1 H₂O:HCl:H₂O₂ solution, both at 80°C.</td>
</tr>
<tr>
<td>3</td>
<td>HF dip</td>
<td>in 10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>4</td>
<td>Light phosphorous diffusion on both sides</td>
<td>830°C for 30 minutes with a main flow of N₂: 180l/hour, O₂: 130cc/min and N₂ through the POCl₃: 45cc/min. Rₓ: 600–1800Ω/□.</td>
</tr>
<tr>
<td>5</td>
<td>Phosphorous glass deglaze</td>
<td>10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>6</td>
<td>Oxidation</td>
<td>For thickness ≥100nm: 1100°C with TCA, thickness controlled by varying the time. For thickness ~25nm: 900°C for 60 minutes with TCA. For all: O₂ flow rate 100l/hour and 30 minute N₂ anneal before unloading at 1000°C (flow rate 100l/hour).</td>
</tr>
<tr>
<td>7</td>
<td>Forming gas anneal (FGA)</td>
<td>30 minutes at 400°C in forming gas (5% H₂ in Ar).</td>
</tr>
<tr>
<td>8</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities</td>
</tr>
<tr>
<td>9</td>
<td>RCA clean and LPCVD nitride deposition</td>
<td>Deposition pressure 0.5torr, temperature 750°C. Flow ratio of DCS:NH₃ 1:4. Nitride thickness controlled by varying the deposition time.</td>
</tr>
<tr>
<td>10</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>11</td>
<td>RCA clean and nitrogen anneal</td>
<td>Anneal in N₂, flow rate 100l/hour. Varying temperature and time.</td>
</tr>
<tr>
<td>12</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>13</td>
<td>RCA clean and hydrogen re-introduction</td>
<td>One of: high temperature FGA, anneal, immersion in hydrogen plasma, 2nd LPCVD deposition or wet oxidation. (Processing details given in the appropriate sections).</td>
</tr>
<tr>
<td>14</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities</td>
</tr>
</tbody>
</table>
some context the effect of a high temperature FGA on wafers with an oxide/nitride stack.

The loading and unloading conditions depended on the forming gas temperature. For FGA at 900°C or less, wafers were loaded and unloaded at the anneal temperature with the forming gas flowing. For anneals done at higher temperatures, wafers were loaded and unloaded at 900°C after a 2–5 minute cool down with the nitrogen flowing.

To determine the effect of a high temperature FGA on wafers with an oxide only, wafers were subjected to anneals in forming gas at between 600–1000°C. The wafers had a light phosphorous diffusion, oxidation and FGA at 400°C. They were then given a high temperature FGA. The effect on $J_{oc}$ is shown in figure 6.1 and table 6.3 shows the effect on the maximum effective lifetime. All wafers had initial $J_{oc}$ values of 9–16fA/cm²/side. These results show that for higher temperature FGA, there was a slight increase in $J_{oc}$ and a decrease in the maximum effective lifetime observed. The maximum effective lifetime of the wafer after 1000°C FGA is slightly misleading because the $J_{oc}$ value is too high to make a fair comparison with other wafers in this batch. The lifetime measured after the initial oxidation was also significantly lower for this wafer.
Table 6.3: Effect of a high temperature FGA on the maximum $\tau_{\text{eff}}$ observed for wafers with no nitride. These wafers had a light phosphorous diffusion (7,500$\Omega \cdot \text{cm}$ for the wafers annealed at 600–900°C and 15,400$\Omega \cdot \text{cm}$ for the wafer annealed at 1000°C), oxidation and forming gas anneal at (400°C) prior to the high temperature forming gas anneal, which was done for 30 minutes.

<table>
<thead>
<tr>
<th>Anneal temperature (°C)</th>
<th>maximum $\tau_{\text{eff}}$ before FGA (ms)</th>
<th>maximum $\tau_{\text{eff}}$ after FGA (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600</td>
<td>4.2</td>
<td>3.3</td>
</tr>
<tr>
<td>700</td>
<td>4.7</td>
<td>1.9</td>
</tr>
<tr>
<td>800</td>
<td>4.1</td>
<td>0.55</td>
</tr>
<tr>
<td>900</td>
<td>4.1</td>
<td>1.8</td>
</tr>
<tr>
<td>1000</td>
<td>1.4</td>
<td>0.36</td>
</tr>
</tbody>
</table>

The results shown in table 6.3 show that the maximum value of $\tau_{\text{eff}}$ had dropped after FGA. If the surface passivation had not also been worse (indicated by the higher $J_{\text{oc}}$ values) then it would be reasonable to say that some contamination, caused either by hydrogen or an impurity in the forming gas, had damaged the lifetime. The higher $J_{\text{oc}}$ values indicate a loss of surface passivation, which may be due to either a loss of hydrogen from the silicon/oxide interface or to the presence of a contaminant in the emitter region. If it is due to a loss of hydrogen, then comparisons are not meaningful. Since the $J_{\text{oc}}$ values for the wafers annealed at 600–900°C are similar, meaningful comparisons can be made between the effective lifetime of these wafers after FGA. The effective lifetime is quite variable, despite the similar initial effective lifetime values. The lack of any trend in effective lifetime after FGA suggests the presence of a contaminant in the forming gas.

Following high temperature FGA, the surface of some wafers was etched back and they were re-passivated. This should ensure that the surface passivation of the wafers was close to that of the initial wafer and therefore a meaningful comparison between the maximum effective lifetimes can be made. Two sets of two wafers were used. For one wafer in each set, the oxide was stripped and they were re-oxidised and given a FGA at 400°C. For the other two wafers, the oxide was removed and $\sim 10\mu$m of silicon was stripped from each side of the wafers. They were given a light phosphorous diffusion, second oxidation and standard FGA at 400°C. The effective lifetime curves are shown in figure 6.2. The processing details of these wafers are shown in the first half of table 6.4. The second half of this table shows $J_{\text{oc}}$ and maximum $\tau_{\text{eff}}$ values for the wafer initially and after the re-passivating step.

After the repassivation step, the silicon/oxide interface should have been similar to after the original passivation. $J_{\text{oc}}$ values were higher and maximum $\tau_{\text{eff}}$ values lower, suggesting that the high temperature FGA had a detrimental effect on the wafers. The rise in $J_{\text{oc}}$ can most likely be attributed to increased recombination in the emitter region.
Figure 6.2: Depth of the damage caused by a high temperature forming gas anneal for wafers with an oxide only. All wafers had a light phosphorous diffusion, oxidation and 400°C FGA (o). All wafers were given a forming gas anneal, mm64e had 30 minutes at 1000°C, mm64d had 30 minutes at 900°C and both mm88e and c had 60 minutes at 1000°C. The oxide was stripped from all four wafers and silicon was stripped from mm64d (12µm per side) and mm88c (8µm per side). mm64d and mm88c had a light phosphorous diffusion and all wafers had a second oxidation and FGA at 400°C (□).
### High Temperature FGA: Wafers with an Oxide/Nitride Stack

A high temperature forming gas anneal to recover wafers with an oxide/nitride stack could be easily incorporated into a cell processing sequence since a forming gas anneal at 400°C in a conventional quartz tube furnace is a standard step. The main disadvantage of using a high temperature forming gas anneal is that it introduces the complications of an additional high temperature step. These include increased economic and energy costs and a greater risk of contamination or degradation from a high temperature step. In addition, high temperature annealing after metallisation is precluded.

For wafers with an oxide/nitride stack, $J_{\infty}$ after a high temperature FGA will be

<table>
<thead>
<tr>
<th>wafer number</th>
<th>$R_\square$ ($\Omega/\square$)</th>
<th>FG temperature (°C)</th>
<th>FG time</th>
<th>silicon stripped (per side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64d</td>
<td>620</td>
<td>900</td>
<td>30 min</td>
<td>12μm</td>
</tr>
<tr>
<td>64e</td>
<td>1540</td>
<td>1000</td>
<td>30 min</td>
<td>none</td>
</tr>
<tr>
<td>88c</td>
<td>1260</td>
<td>1000</td>
<td>60 min</td>
<td>8μm</td>
</tr>
<tr>
<td>88e</td>
<td>1260</td>
<td>1000</td>
<td>60 min</td>
<td>none</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>wafer number</th>
<th>$J_{\infty}$ initial (fA/cm²/side)</th>
<th>$J_{\infty}$ stripped (fA/cm²/side)</th>
<th>max. $\tau_{\text{eff}}$ initial (ms)</th>
<th>max. $\tau_{\text{eff}}$ stripped (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>64d</td>
<td>13</td>
<td>20</td>
<td>4.2</td>
<td>1.2</td>
</tr>
<tr>
<td>64e</td>
<td>9</td>
<td>34</td>
<td>1.3</td>
<td>0.54</td>
</tr>
<tr>
<td>88c</td>
<td>26</td>
<td>31</td>
<td>8.7</td>
<td>0.70</td>
</tr>
<tr>
<td>88e</td>
<td>12</td>
<td>57</td>
<td>16</td>
<td>0.84</td>
</tr>
</tbody>
</table>

Table 6.4: The first half of this table shows processing details for the wafers shown in figure 6.2. The second half shows $J_{\infty}$ and maximum $\tau_{\text{eff}}$ values for these wafers. Initial $J_{\infty}$ and maximum $\tau_{\text{eff}}$ were measured after light phosphorous diffusion, growth of the original oxide and 400°C FGA. ‘Stripped’ measurements were made after silicon strip (if applicable), second light phosphorous diffusion (if applicable), second oxidation and 400°C FGA.

Similarly, the drop in effective lifetime can be attributed to increased recombination in the bulk region. The increased recombination may be due to either impurities in the forming gas or damage caused by the hydrogen. There was a greater increase in $J_{\infty}$ for the wafers that were not stripped, suggesting that the impurities or hydrogen-related damage was concentrated near the surface.

In conclusion, high temperature FGA resulted in increased recombination in both the bulk and emitter regions. It is not clear whether this was due to hydrogen-induced defects or to a contaminant in the forming gas. It is clear from the results that contamination occurred in at least some instances.
determined by a combination of three effects. Firstly, at the higher temperatures, hydrogen bonds at the silicon/oxide interface are broken and hydrogen is lost from this region, thereby increasing $J_{oc}$. Secondly, increased recombination in the emitter region (caused by either contaminants in the forming gas or hydrogen-related damage, as discussed in section 6.3) may result in an increase in $J_{oc}$. Lastly, hydrogen from the ambient may diffuse through the nitride and oxide to passivate the silicon/oxide interface, thereby resulting in a decrease in $J_{oc}$.

The results in section 6.3 showed that a drop in effective lifetime (and rise in $J_{oc}$) could occur with a high temperature FGA. If this was due to hydrogen, then it may also occur with an oxide/nitride stack. If it was due to an impurity in the forming gas, then it is possible that the nitride may act as a diffusion barrier. The temperature and time necessary for $J_{oc}$ recovery using a forming gas anneal may need to be carefully balanced so as to allow hydrogen through the nitride, without compromising the performance of the finished wafer.

This section discusses the effectiveness of a high temperature FGA in recovery of $J_{oc}$ values for wafers with an oxide/nitride stack after high temperature nitrogen anneal. Oxide thickness, nitride thickness, nitrogen anneal temperature, FGA temperature and FGA time have all been varied.

### 6.4.1 Effect of FGA Temperature

A high temperature FGA of wafers with an oxide/nitride stack was first done without a nitrogen anneal. The results are shown in figure 6.3. $J_{oc}$ was found to increase for higher anneal temperatures. This figure probably gives a lower bound on the $J_{oc}$ that can be expected of a particular FGA temperature. The increase in $J_{oc}$ values with increased temperature is probably due, in part, to a lack of hydrogen at the silicon/oxide interface. Even though the wafers were in a hydrogen-containing ambient, the high temperatures cause hydrogen bonds at the silicon/oxide interface to break and at these temperatures, it is possible that the rate of bond formation is lower than the rate of bond breakage.

Figure 6.4 shows wafers that had a single forming gas anneal at 40° intervals between 800–1000°C following a 1 hour nitrogen anneal at 900°C. These wafers had 100nm of oxide and ~33nm of nitride. The nitrogen anneal was done for 1 hour at 900°C and the forming gas anneals were done for 30 minutes. The FGA allowed almost complete hydrogen re-introduction in the range 800–880°C.

From figure 6.4, FGA at 920°C and above did not result in a decrease in $J_{oc}$. The wafers annealed at 920–1000°C were given a second FGA, for 30 minutes at 800°C. The results are shown in figure 6.5. The considerable drop in $J_{oc}$ that occurred after this FGA
Figure 6.3: Effect of forming gas anneal temperature on $J_{oe}$ for wafers with an oxide/nitride stack that did not have a high temperature nitrogen anneal. The oxide thickness was 25nm and the nitride thickness 51nm. FGA were done for 1 hour. $J_{oe}$ values after oxide nitride stack formation were 14–16fA/cm$^2$ for all wafers.
Figure 6.4: The effect of forming gas anneal temperature on $J_{oe}$ for wafers with an oxide/nitride stack after nitrogen anneal. These wafers had an oxide thickness of 100nm and a nitride thickness of 33nm. The nitrogen anneal was done for 1 hour at 900°C. There were six wafers, and they each spent 30 minutes in the high temperature forming gas ambient, followed by a 2-5 minute flush and cool down in nitrogen for the wafers with anneal temperatures greater than 900°C. The $J_{oe}$ values for these wafers after oxide/nitride stack formation were 12-18fA/cm²/side. After nitrogen anneal, $J_{oe}$ values were 640-1510fA/cm²/side.
Figure 6.5: Recovery from a higher temperature FGA using a lower temperature FGA. These wafers are the same as those shown in figure 6.4. They had oxide/nitride stack formation (100/33nm), nitrogen anneal for 1 hour at 900°C and attempted recovery for 30 minutes in forming gas at elevated temperatures (FG 1). They then had a second FGA for 30 minutes at the same temperature (not shown) and the wafers that had FG 1 and 2 at 920-1000°C had an additional FGA at 800°C (FG 3). The x-axis shows forming gas temperatures for FG1 and FG2.

suggests that the high $J_{oc}$ seen in figure 6.4 can be attributed, in large part, to a lack of hydrogen at the silicon interface.

6.4.2 Effect of the Time Duration of the FGA

The effect of the time duration of the FGA on $J_{oc}$ recovery was assessed using FGA at 600, 700 and 800°C. The results are shown in figure 6.6 for wafers that underwent a nitrogen anneal at 900°C. Forming gas anneals were done on each wafer for for 1, 4 and 24 hours. There was no response to the 600°C FGA, even after a total of 29 hours. After a total anneal time of 29 hours at 700°C, the $J_{oc}$ had recovered completely. For the 800°C anneals, after 5 hours $J_{oc}$ was completely recovered, but after 29 hours, $J_{oc}$ had increased again. This effect remains unexplained, at present. It is possibly due to a contaminant from the forming gas that has resulted in increased recombination in the emitter region.

6.4.3 Effect of Oxide Thickness

Table 6.5 shows $J_{oc}$ values for wafers with 25nm and 225nm thick oxides after oxide/nitride stack formation, nitrogen anneal and 2 and 6 hour forming gas anneals. The $J_{oc}$ after the
Figure 6.6: The effect of long, moderate temperature forming gas anneals on $J_{oe}$ for wafers with an oxide/nitride stack after a 900°C nitrogen anneal. These wafers had a 25nm oxide and 53nm nitride. The legend shows the FGA temperature. ‘Oxide’ refers to the wafers after light phosphorous diffusion, oxidation and standard FGA for 30 minutes at 400°C. ‘Nitride’ refers to the wafer after nitride deposition. The nitrogen anneal was done for 1 hour at 900°C. FG 1, 2 and 3 were done for 1, 4 and 24 hours respectively, at the temperature indicated on the legend. The same wafer was used for each step, so any effect is cumulative.
Table 6.5: Effect of oxide thickness on \( J_{\text{oc}} \) recovery using a high temperature FGA. Nitride thickness was 65nm for both wafers. The nitrogen anneal was done for 1 hour at 900°C. The emitter sheet resistance after phosphorous diffusion was 1400Ω for both wafers, but after oxidation, the wafer with the 225nm thick oxide would have had a deeper diffusion.

<table>
<thead>
<tr>
<th>Oxide thickness (nm)</th>
<th>( J_{\text{oc}} ): oxide/nitride stack (fA/cm²/side)</th>
<th>( J_{\text{oc}} ): N₂ annealed (fA/cm²/side)</th>
<th>( J_{\text{oc}} ): FGA (2 hours) (fA/cm²/side)</th>
<th>( J_{\text{oc}} ): FGA (6 hours) (fA/cm²/side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>6</td>
<td>88</td>
<td>40</td>
<td>26</td>
</tr>
<tr>
<td>225</td>
<td>12</td>
<td>73</td>
<td>29</td>
<td>24</td>
</tr>
</tbody>
</table>

6.4.4 Effect of Nitride Thickness

The effect of nitride thickness on \( J_{\text{oc}} \) recovery for an oxide/nitride stack after a high temperature nitrogen anneal can be seen in figure 6.7. Two wafers are shown, both with an oxide thickness of 25nm and with nitride thicknesses of 21nm and 65nm. As expected, after nitrogen anneal (at 900°C for 1 hour), the wafer with the thinner nitride had the higher \( J_{\text{oc}} \). Recovery for this wafer was faster, so that after a FGA for only 30 minutes (at 840°C), the wafer with the thinner nitride had the lower \( J_{\text{oc}} \). The \( J_{\text{oc}} \) of the wafer with the 65nm thick nitride was not affected by the first FGA, probably because the time was too short to allow hydrogen diffusion through the nitride. After a further 90 minutes in forming gas (again at 840°C), the wafer with the thicker nitride maintained the higher \( J_{\text{oc}} \). The difference between the two wafers was smaller. After a further 4 hours, there was negligible difference between the two wafers. These results imply that hydrogen re-introduction through an oxide/nitride stack was slowed, but not prevented, by the thicker nitride. \( J_{\text{oc}} \) values did not recover to their initial values. Again, this indicates that not all of the dangling bonds that can be passivated by hydrogen have been passivated, or that there were increased recombination rates in the emitter.
Figure 6.7: $J_{oe}$ recovery using a high temperature FGA with a 21nm thick nitride compared with a 65nm thick nitride. The sheet resistance after phosphorous diffusion was 1400Ω/□ and both wafers had a 25nm thick oxide. ‘Oxide’ refers to the wafers after light phosphorous diffusion, oxidation and 400°C FGA and ‘nitride’ refers to the wafers immediately after nitride deposition. The nitrogen anneal was done for 1 hour at 900°C and the FGA were done at 840°C for the indicated times. Note that the final recovery point is approximately equal for both wafers.
6.4.5 Effect of Nitrogen Anneal Temperature/Time on \( J_{\infty} \) Recovery

The nitrogen anneal temperature may affect hydrogen re-introduction because silicon nitride changes structurally at high temperatures. In an inert gas ambient, hydrogen is lost and the silicon becomes more dense as the number of N–N and Si–N bonds increases [20]. This could affect the diffusion of molecular hydrogen and atomic hydrogen that does not form bonds in the nitride simply because the material is denser. For atomic hydrogen that does form bonds in the nitride, diffusion will be affected because the number of bonding sites is reduced. For this work, nitrogen anneals were done at both 900 and 1000°C. This brackets the likely temperature range for cell fabrication steps after oxide/nitride stack formation. An experiment was done using wafers with a 100nm thick oxide and a 25nm thick nitride. Wafers had a nitrogen anneal at 900°C or 1000°C for 15 or 60 minutes and recovery consisted of two forming gas anneals, the first at 800°C for 30 minutes and the second at 840°C for 4 hours.

The results are shown in figure 6.8. After the first recovery attempt (FGA 1), the samples that had been annealed in nitrogen at 900°C had both recovered to the same point and \( J_{\infty} \) values were significantly lower than either of the samples that had been annealed in nitrogen at 1000°C. Interestingly, the sample annealed in nitrogen for 60 minutes at 900°C had recovered to approximately the same point as the sample annealed 15 minutes at 900°C, even though the \( J_{\infty} \) value after the 15 minute anneal was much lower than after the 1 hour anneal. This suggests that hydrogen diffusion through the nitride annealed at 900°C is rapid.

Of the samples annealed in nitrogen at 1000°C, the wafer given the 15 minute treatment had made a greater improvement than the wafer given the 60 minute treatment. This suggests that although hydrogen levels in the nitride were depleted after both 1000°C anneals, as evidenced by the high and similar \( J_{\infty} \) values, the structure of the nitrides was different. For the wafer that had the 1 hour anneal, the nitride was presumably much denser than for the wafer that had the 15 minute anneal and hence hydrogen diffusion through the wafer annealed for 1 hour was slowed. After the second recovery attempt (FGA 2), all the wafers recovered to approximately the same level. This suggests that the nitrogen anneal temperature and time affected the time required to re-introduce hydrogen to the silicon/oxide interface, but not the final recovery point.

6.4.6 Comparison to the work of King

Recovery of \( J_{\infty} \) values using a high temperature FGA should be compared to results reported by King [183], who did a brief investigation on the effects of high temperature
Figure 6.8: Effect of nitrogen anneal temperature/time on $J_{oe}$ recovery for wafers with a 100nm thick oxide and 25nm thick nitride. Nitrogen anneals were done at 900 or 1000°C for 15 or 60 minutes, as indicated in the legend, before attempted recovery in a forming gas ambient. ‘Oxide’ refers to the wafers after light phosphorous diffusion, oxidation and 400°C FGA and ‘nitride’ refers to the wafers immediately after nitride deposition. The first recovery attempt (FGA 1) was done at 800°C for 30 minutes and the second (FGA 2) was done at 840°C for 4 hours.
FGA on wafers with an oxide/LPCVD nitride stack. King also used high resistivity FZ material but reported $\tau_{\text{eff}}$, rather than $J_{\text{oc}}$ values. The material was of high quality, as evidenced by a $\tau_{\text{eff}}$ for an undoped surface with a 90nm thick oxide after a 30 minute FGA at 450°C of 1.0ms.

There are some differences between the technique used by King and that reported here. King deposited at slightly higher temperatures (805 compared with 750°C), lower pressures (0.3 compared with 0.6 torr) and with a higher DCS:NH$_3$ flow rate (0.33 compared with 0.25). The forming gas used by King had a slightly higher hydrogen content (5% compared with 4%).

The results reported by King are distinctly different to those reported in this thesis. The primary difference is that after nitride deposition, King found that the effective lifetime was too low to measure. In contrast, for the work in this thesis, effective lifetimes were at least several milliseconds for most wafers and unaffected by nitride deposition. The low lifetimes observed by King were probably due to a lack of hydrogen, since they could be recovered with a high temperature FGA. The deposition method used by King may have had similar effects to that used by Xie et al. [349], who found that after deposition of an LPCVD nitride, hydrogen was lost from the underlying oxide. If this happened to King also, the surface passivation after nitride deposition may have not been sufficient to see good bulk lifetimes.

For wafers with a 90nm thick oxide and a 14nm thick nitride, King saw an increase in $\tau_{\text{eff}}$ with increased forming gas temperature. In one particular batch, wafers had a 30 minute, 450°C FGA following nitride deposition and for a wafer with an oxide only, $\tau_{\text{eff}}$ was 1.0ms but too short to measure for a wafer with oxide and nitride. In a second batch, wafers had a 90 minute, 1000°C FGA after nitride deposition and for wafers in this batch with an oxide only, $\tau_{\text{eff}}$s of 0.76 and 0.56ms were measured. For wafers in this batch with oxide and nitride $\tau_{\text{eff}}$ was 1.7ms after FGA. The fact that such high lifetimes were measured after a 1000°C FGA support the hypothesis that a drop in effective lifetime after a high temperature FGA is due to contaminants in the FG, not to damage caused by the hydrogen.

6.4.7 High Temperature Forming Gas Anneals: Conclusions

High temperature forming gas anneals on wafers with an oxide resulted in a modest reduction in bulk lifetime and an increase in $J_{\text{oc}}$. It could not be discerned whether this was due to an impurity in the forming gas or to damage caused by the hydrogen. Several results suggest that the drop in effective lifetime was due to an impurity in the forming gas.
A forming gas anneal of a wafer with an oxide/nitride stack after nitrogen anneal was beneficial, allowing complete $J_{oc}$ recovery, provided conditions were chosen carefully. The oxide thickness had negligible effect on recovery. Nitride thickness and the thermal history of the wafer were shown to be important. Thicker nitrides meant a slower rate of recovery, but did not limit the final recovery point. Wafers that had been annealed in nitrogen at higher temperatures, or at a given temperature for longer times, required a longer time in the forming gas ambient to recover. This was possibly due to the increased bonding between silicon and nitrogen atoms in the nitride slowing diffusion through the nitride. If FGA temperatures were too high, removal of hydrogen from the silicon/oxide interface was significant and this effect was in competition with the re-introduction of hydrogen.

### 6.5 Alneal

An alneal is normally done on an oxidised wafer. Aluminium is evaporated onto the wafer in a vacuum chamber. The wafer is then annealed in forming gas. During this anneal, aluminium reacts with hydroxyl ions in the oxide to produce atomic hydrogen [26]. Enough of this hydrogen diffuses to and passivates the interface to result in significant improvements in surface passivation. The aluminium is stripped from the wafer in hot ($\sim 90^\circ C$) orthophosphoric acid.

The effectiveness of an alneal as a method of hydrogen re-introduction through an oxide/nitride stack after nitrogen anneal was investigated. For these experiments, 2000Å of aluminium was evaporated and forming gas anneals were done at $400^\circ C$ for 30 minutes. Complete recovery was not demonstrated. Significant improvement in $J_{oc}$ was seen for wafers with a thin nitride that had been annealed in nitrogen at $900^\circ C$. No improvement was seen for wafers that had been annealed in nitrogen at $1000^\circ C$. Table 6.6 shows the effect of an alneal on $J_{oc}$ for selected wafers after a $900^\circ C$ nitrogen anneal. Also shown are the results for a wafer that had no nitride. The last two wafers shown in table 6.6 have a good ARC and in this case, the alneal resulted in a slight increase in $J_{oc}$ values. For the wafers with a 150nm thick oxide, it is possible that some of the decrease in $J_{oc}$ was due to hydrogen remaining in the oxide being released and diffusing to the silicon interface. The magnitude of the change is similar to that shown in figure 5.13, for a 30 minute, $400^\circ C$ FGA following a 1 hour $900^\circ C$ nitrogen anneal. This could not have been the case for the wafers with 225nm thick oxides as the ‘$N_2$ anneal’ measurements shown in table 6.6 were made after a 30 minute, $400^\circ C$ FGA.
<table>
<thead>
<tr>
<th>Oxide thickness (nm)</th>
<th>Nitride thickness (nm)</th>
<th>Sheet res. (Ω/□)</th>
<th>$J_{oc}$ N$_2$ anneal (fA/cm$^2$/side)</th>
<th>$J_{oc}$ annealed (fA/cm$^2$/side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>0</td>
<td>620</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>225</td>
<td>33</td>
<td>900</td>
<td>3100</td>
<td>1400</td>
</tr>
<tr>
<td>225</td>
<td>33</td>
<td>900</td>
<td>2500</td>
<td>710</td>
</tr>
<tr>
<td>150</td>
<td>33</td>
<td>930</td>
<td>130</td>
<td>58</td>
</tr>
<tr>
<td>150</td>
<td>33</td>
<td>930</td>
<td>160</td>
<td>73</td>
</tr>
<tr>
<td>150</td>
<td>60</td>
<td>930</td>
<td>66</td>
<td>36</td>
</tr>
<tr>
<td>150</td>
<td>60</td>
<td>930</td>
<td>91</td>
<td>45</td>
</tr>
<tr>
<td>25</td>
<td>60</td>
<td>620</td>
<td>270</td>
<td>360</td>
</tr>
<tr>
<td>25</td>
<td>60</td>
<td>620</td>
<td>630</td>
<td>905</td>
</tr>
</tbody>
</table>

Table 6.6: The effect of an anneal on $J_{oc}$ after a 900°C nitrogen anneal. The sheet resistance was measured after phosphorous diffusion. These wafers all had a $J_{oc}$ in the range 14-17fA/cm$^2$/side after nitride deposition. The first set of results are for a wafer with no nitride.

6.6 Hydrogen Plasma

A hydrogen-containing plasma is an obvious source of atomic hydrogen. At Universität Konstanz, a hydrogen plasma has been successfully integrated into a silicon nitride LPCVD system. The plasma is generated remotely using microwave induction from a He/H$_2$ gas mixture. The wafers are exposed to the hydrogen plasma immediately prior to and immediately after nitride deposition. On multi-crystalline material, a doubling in effective minority carrier lifetimes has been attributed to the hydrogen plasma [243].

A PECVD nitride deposition is well known to enhance surface passivation properties for bare silicon wafers or wafers with an oxide only. This has been demonstrated by many groups including ISFH with their high efficiency bifacial cells and the MIS-IL cells developed by Hezel et al. [1].

Two attempts were made to recover $J_{oc}$ values using a hydrogen plasma. Both were in a plasma enhanced chemical vapour deposition (PECVD) chamber. The first method involved deposition of a PECVD silicon nitride and the second did not. When deposition occurred, the plasma was formed from both ammonia (NH$_3$) and silane (SiH$_4$) gas. In the absence of deposition, the plasma was formed from NH$_3$ gas only. The disadvantage of depositing silicon nitride was that the nitride thickness increased, thereby increasing the barrier through which the hydrogen had to diffuse. The advantage of depositing silicon nitride was that, in the system used for this work, the plasma was stronger. Conversely, with a plasma formed from ammonia gas, the nitride thickness did not increase during exposure, but the plasma was much weaker.

After plasma treatment, wafers were given an RCA clean and 30 minute FGA at 400°C to remove any residual charging. The PECVD deposition system is line-of-sight only and so two runs were necessary to expose both sides of the wafer to the plasma. The results
are discussed firstly for hydrogen plasma with PECVD nitride deposition and secondly for exposure to an ammonia plasma without nitride deposition.

### 6.6.1 Hydrogen Plasma with PECVD Nitride Deposition

PECVD silicon nitride was deposited at Electronic Materials Engineering (EME), ANU. Reactant gases were ammonia (NH$_3$) and silane (SiH$_4$). The silane was 5% silane in nitrogen. The flow rate of silane plus nitrogen to ammonia was approximately 7 to 1. The deposition chamber was at low pressure (0.6 torr) and the sample was placed on a plate that was heated to 400°C. Plasma was generated directly above the wafer.

Silicon nitride deposition using the PECVD system was done in two wafer batches and is summarised in table 6.7. The wafers in the first batch all had nitrogen anneals between 750–1000°C in 50°C increments. For these wafers, improvement after PECVD deposition was found to be weakly dependent on oxide thickness and strongly dependent on nitride thickness. Figure 6.9 shows results for the wafers with 14nm of LPCVD nitride and figure 6.10 shows results for wafers with 24nm of LPCVD nitride. The wafers with 14nm of LPCVD nitride had improved considerably after the second PECVD deposition.

Further treatment may not show improvement at the same rate since the increased nitride thickness could slow the rate at which hydrogen reaches the silicon interface. The wafers with 24nm of LPCVD nitride showed a slight improvement in $J_{oc}$ after PECVD nitride deposition. It is highly unlikely that the decrease in $J_{oc}$ after PECVD nitride deposition was due to hydrogen that remained in the oxide and diffused to the silicon interface since the wafer had already had a 30 minute 400°C FGA prior to the ‘N2 anneal’ measurement.

<table>
<thead>
<tr>
<th>Oxide thickness (nm)</th>
<th>LPCVD nitride thickness (nm)</th>
<th>1st PECVD deposition (s/side)</th>
<th>2nd PECVD deposition (s/side)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>First wafer batch</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td>14</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>150</td>
<td>14</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>100</td>
<td>24</td>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td>150</td>
<td>24</td>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Second wafer batch</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>35</td>
<td>15</td>
<td>–</td>
</tr>
</tbody>
</table>

*Table 6.7: PECVD depositions for wafers with an oxide/nitride stack after high temperature nitrogen anneals.*

The second set of wafers to undergo PECVD silicon nitride deposition had nitrogen anneals at 900°C or 1000°C and a more effective ARC (25nm of oxide and ~35nm of nitride). They were given a 15 minute PECVD deposition on each side. There was negligible change in surface passivation or implied $V_{oc}$ after nitride deposition. This is
Figure 6.9: Effect of PECVD nitride deposition on wafers with 14nm of LPCVD silicon nitride. These wafers had 100 and 150nm thick oxides, as shown in the legend. A wafer with 100nm of oxide and no LPCVD nitride is also shown. Nitrogen anneal for these wafers included an hour at 1000°C. 'Oxide' refers to the wafers immediately after light phosphorous diffusion, oxidation and standard FGA at 400°C. PECVD 1 was done for 30s/side. PECVD 2 was done for 40s/side.

Figure 6.10: Effect of PECVD nitride deposition on wafers with 24nm of LPCVD silicon nitride. These wafers had 100 and 150nm thick oxides, as shown in the legend. A wafer with 100nm of oxide and no LPCVD nitride is also shown. Nitrogen anneal for these wafers included an hour at 1000°C. 'Oxide' refers to the wafers immediately after light phosphorous diffusion, oxidation and standard FGA at 400°C. PECVD 1 was done for 30s/side. PECVD 2 was done for 60s/side.
possibly due to the thicker nitride (both LPCVD and PECVD) acting as a diffusion barrier to the hydrogen ions.

### 6.6.2 Using an Ammonia Plasma

Hydrogen re-introduction to the silicon interface was also attempted in the PECVD deposition system without nitride deposition. Plasma was created using ammonia as a source gas. Deposition was done at 0.6torr, 400°C and with an NH$_3$ flow rate of 100sccm. Exposure times of 5, 10 and 15 minutes/side were used for wafers that had undergone nitrogen anneals at both 900°C and 1000°C. In all cases, the oxide was 25nm thick and the LPCVD nitride was ~35nm thick. Figure 6.11 shows final J$_{oc}$ values after ammonia plasma treatment.

In the case of the 900°C nitrogen anneal, J$_{oc}$ values improved after exposure to the plasma, suggesting that hydrogen was able to diffuse through the nitride. It is possible that some of the improvement seen with these wafers was due to the hydrogen remaining in the oxide being released and diffusing to the silicon interface. This is unlikely to be a significant effect given the results shown in figure 5.13, which shows only a small improvement in J$_{oc}$ with a 400°C treatment after a 1 hour 900°C nitrogen anneal. In the case of the 1000°C nitrogen anneal, the plasma treatment had no effect on J$_{oc}$ and it is unlikely that hydrogen ions diffused through this nitride. The observation that it is more difficult for atomic hydrogen to diffuse through a nitride after a 1000°C anneal is probably explained by the increased silicon–nitrogen bonding that has occurred due to the loss of hydrogen [20].

### 6.6.3 Hydrogen Plasma: Conclusions

Encouraging results for J$_{oc}$ recovery of wafers with an oxide/nitride stack, were seen with hydrogen-containing plasmas after a high temperature nitrogen anneal. With a stronger plasma, and simultaneous PECVD nitride deposition, partial J$_{oc}$ recovery was seen even after annealing in nitrogen at 1000°C with a thin nitride. A weaker plasma and no PECVD nitride deposition enabled J$_{oc}$ recovery after annealing in nitrogen at 900°C, but negligible J$_{oc}$ recovery was evident after annealing in nitrogen at 1000°C. Experiments with both plasma types (weaker and stronger) were done with relatively thin LPCVD nitride layers.

The fact that surface passivation quality substantially recovered at 400°C in a plasma ambient, whereas there was negligible change in a 400°C forming gas ambient indicates that, at 400°C, atomic hydrogen was far more mobile in the nitride than molecular hydrogen.
Figure 6.11: Effect of a 400°C ammonia plasma on $J_{oe}$ after a 1 hour nitrogen anneal at 900 and 1000°C as a function of exposure time. The oxide thickness was 25nm and the LPCVD nitride was ~35nm thick in all cases. The $J_{oe}$ values for these wafers after oxide/nitride stack formation were 14–21fA/cm²/side.
6.7 LPCVD

As was discussed in section 4.2, both molecular and atomic hydrogen are present in the LPCVD furnace. To determine if a second LPCVD deposition could be used for \( J_{oc} \) recovery, experiments were done with two wafers. After standard stack formation (oxide thickness of 20nm, nitride thickness of 20nm) and nitrogen anneal (60 minutes at 900\(^\circ\)C or 1000\(^\circ\)C), a second LPCVD nitride was deposited. This second nitride was 74nm thick and the samples spent approximately 16 minutes in the chamber with the reactant gases flowing. \( J_{oc} \) values for these wafers are shown in figure 6.12. In the case of the 900\(^\circ\)C nitrogen anneal, there was an improvement after the second LPCVD deposition. In the case of the 1000\(^\circ\)C nitrogen anneal, the second LPCVD deposition did not affect \( J_{oc} \). Again, this is probably due to the structural change of the silicon nitride after the 1000\(^\circ\)C anneal.

The wafers spent only 16 minutes in the furnace for the second LPCVD deposition and it is possible that further \( J_{oc} \) recovery would be seen with longer exposure. This would result in the deposition of a very thick nitride layer and therefore compromise the ARC. Thus, the potential of a second LPCVD deposition to recover \( J_{oc} \) values is not good. For practical purposes, a second LPCVD nitride layer is not ideal as an additional cell fabrication step would be required to remove some of this second nitride in order to contact the cell.

6.8 Wet Oxidation

To do a ‘wet oxidation’, water vapour, with oxygen as a carrier gas, is introduced to the furnace. Dissociation of the water molecules occurs and silicon oxide grows on the exposed silicon or on silicon oxide. On a silicon wafer, the reaction proceeds according to:

\[
H_2O + Si \rightarrow SiO_2 + H_2. \tag{6.1}
\]

On a silicon nitride layer, oxide growth occurs very slowly [264]. Nevertheless, hydrogen would be produced, and this may be able to diffuse through the oxide/nitride stack to passivate the silicon interface.

Figure 6.13 shows \( J_{oc} \) values for two wafers after oxide/nitride stack formation, nitrogen anneal and wet oxidation. In this case, nitrogen anneals were done for an hour at both 900 and 1000\(^\circ\)C. The wet oxidation was done for 1 hour at 840\(^\circ\)C. Oxide thickness was 25nm and the nitride was kept thin, at approximately 20nm. The wet oxidation caused a marginal improvement after a nitrogen anneal at 1000\(^\circ\)C, but had negligible effect after
Figure 6.12: Attempts to recover $J_{oe}$ using a second LPCVD deposition. The legend shows nitrogen anneal temperature. ‘Oxide’ refers to the wafers immediately after light phosphorous diffusion, oxidation and standard FGA at 400°C. ‘Nitride’ refers to the wafers immediately after nitride deposition. The nitrogen anneal was done for 1 hour and the oxide and initial LPCVD nitride were both 20nm thick. The second LPCVD nitride deposition took 16 minutes and resulted in deposition of an additional 74nm of nitride.
a nitrogen anneal at 900°C. Wet oxidations were also done for 30 minutes at 900°C, and the results were very similar to those shown in figure 6.13. The high $J_{oe}$ values after wet oxidations suggest that this was not a successful method of hydrogen re-introduction.

6.9 Conclusions

This chapter discussed various methods of $J_{oe}$ recovery. The methods were chosen based on the assumption that recovery of $J_{oe}$ after a high temperature anneal in nitrogen for wafers with an oxide/nitride stack could be achieved by re-introducing hydrogen. The most important parameters in determining the success of $J_{oe}$ recovery were found to be thickness of the nitride layer and temperature of the nitrogen anneal. Complete recovery of $J_{oe}$ was demonstrated using high temperature forming gas anneals and partial recovery was demonstrated with other methods. Table 6.8 summarises the success of the different methods of $J_{oe}$ recovery.

To determine the baseline effect of a high temperature FGA, wafers with an oxide and no nitride were subjected to high temperature forming gas anneals. It was found that higher temperatures or longer times at lower temperatures resulted in an increase in
J_{oc} and a drop in effective lifetime. It is not clear whether this was due to impurities in the forming gas or to defects induced by the high temperature hydrogen. Some results implied that impurities in the forming gas are the more likely explanation. For wafers with an oxide/nitride stack, a high temperature FGA was used to recover J_{oc} values after a high temperature nitrogen anneal. The time and temperature needed for this anneal were found to be dependent on the thickness of nitride and on the thermal history of the wafer. Wafers with a thicker nitride or that underwent higher temperature nitrogen anneals required a longer time or higher temperature forming gas anneal to affect full recovery of J_{oc}. For temperatures greater than approximately 900°C, hydrogen removal from the silicon interface became significant, resulting in increased J_{oc} values. In this case, J_{oc} values were shown to be recoverable using a forming gas anneal at lower temperatures.

Anneals were unsuccessful at J_{oc} recovery for wafers that had been annealed in nitrogen at 1000°C. Some success was seen for wafers that had been annealed in nitrogen at 900°C. With a 900°C nitrogen anneal and a near-ideal ARC, J_{oc} values increased slightly with an anneal.

A stronger plasma (co-incident with PECVD nitride deposition) was beneficial in J_{oc} recovery for wafers with a thin LPCVD nitride irrespective of nitrogen anneal temperature. This was only attempted with a maximum LPCVD nitride thickness of 24nm. With a weaker plasma (and without PECVD nitride deposition) and oxide/nitride thicknesses of 25/35nm, the nitrogen anneal temperature was found to be important. In this case, no improvement was seen for wafers after a 1000°C nitrogen anneal.

The fact that surface passivation quality substantially recovered at 400°C in a plasma ambient, whereas there was negligible change in a 400°C forming gas ambient indicates that atomic hydrogen was far more mobile in the nitride than molecular hydrogen.

A second LPCVD deposition enabled some recovery of J_{oc} for wafers that had been annealed in nitrogen at 900°C. After a nitrogen anneal at 1000°C, a second LPCVD deposition had negligible effect on J_{oc}.

A wet oxidation resulted in minimal J_{oc} recovery for wafers that had been annealed in nitrogen at 1000°C. A wet oxidation had negligible effect on wafers that had been annealed in nitrogen at 900°C.

The most consistently successful method of J_{oc} recovery for a wafer with an oxide/nitride stack following a high temperature nitrogen anneal was a high temperature forming gas anneal. This has the advantages of being relatively inexpensive and easy to implement but the disadvantage of being a further high temperature step. Promising results for J_{oc} improvement were seen with a hydrogen plasma and further investigation may show this to be a sound method for J_{oc} recovery.
Table 6.8: A summary of the success of various methods of $J_{oc}$ recovery for chemically polished wafers with an oxide/nitride stack after nitrogen anneals at 900 and 1000°C. An optimised anti-reflection coating was taken to be approximately 25nm of oxide under approximately 50nm of nitride.

<table>
<thead>
<tr>
<th>Technique</th>
<th>Recovery after N$_2$ anneal at 900°C</th>
<th>Recovery after N$_2$ anneal at 1000°C</th>
<th>Recovery with an optimised ARC</th>
</tr>
</thead>
<tbody>
<tr>
<td>High temperature FGA Aneal</td>
<td>complete</td>
<td>complete</td>
<td>complete</td>
</tr>
<tr>
<td>H plasma (PECVD dep.)</td>
<td>partial</td>
<td>negligible</td>
<td>negligible</td>
</tr>
<tr>
<td>H plasma (NH$_3$ only)</td>
<td>not attempted</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>2nd LPCVD dep.</td>
<td>very good</td>
<td>negligible</td>
<td>not attempted</td>
</tr>
<tr>
<td>Wet oxidation</td>
<td>partial</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td></td>
<td>negligible</td>
<td></td>
<td>not attempted</td>
</tr>
</tbody>
</table>
In this chapter, the effects of high temperature anneals in both nitrogen and forming gas are again determined for wafers with an oxide/LPCVD nitride stack. The focus of this chapter is on using a range of silicon wafers. In particular, the effects of emitter sheet resistance, wafer resistivity, dopant type and surface texture have been determined. The optimal emitter sheet resistance was found to be independent of nitrogen anneal temperature. No clear influence of wafer resistivity or type on $J_{oc}$ values after nitride deposition, nitrogen anneal or high temperature FGA could be discerned. With textured wafers, recovery of $J_{oc}$ values after a high temperature nitrogen anneal was not demonstrated for wafers with a thin oxide. This was shown to be due to a lack of surface passivation at the silicon/oxide interface.

7.1 Introduction

Experiments reported in the previous chapters were done using chemically polished, high resistivity, float zone wafers with a very light phosphorous diffusion. These conditions were designed to enable a sensitive measurement of the wafer surface, rather than to optimise cell performance. The results discussed in this chapter are for oxide/nitride stacks on wafers using parameters (such as the emitter sheet resistance) and features (such as texturing) likely to be useful for solar cell fabrication.

To form textured wafers, a KOH solution was used. On a planar, (100) orientated wafer, KOH texturing results in random pyramids with sides of (111) orientation. Therefore, as a preliminary step to the work on textured wafers, the effect of nitrogen anneals and high temperature forming gas anneals on planar, polished (111) compared with (100) orientated wafers was determined.
7.2 Experimental Conditions

The wafers in this chapter were prepared similarly to those reported in chapters 5 and 6. The steps are shown in table 7.1. After a high temperature nitrogen anneal, hydrogen re-introduction was attempted using forming gas anneals at 840°C for various times.

7.3 Varying Emitter Sheet Resistance

On a p-type wafer, diffusion of an n-type dopant such as phosphorous creates the p-n junction of a solar cell. With higher temperature steps the junction is driven further into the wafer and the sheet resistance decreases. The sheet resistance, $R_{\square}$, is given by:

$$R_{\square} = 1/ \int_{0}^{x_j} q \mu(x) N(x) \, dx,$$  \hspace{1cm} (7.1)

where $x_j$ is the junction depth, $\mu(x)$ is the majority carrier mobility and $N(x)$ is the total impurity concentration.

With lower sheet resistances (and therefore higher doping levels), the rates of all recombination processes are increased [129]. A lower emitter sheet resistance therefore usually results in a higher $J_{sc}$ and a lower $V_{oc}$. An exception is the case where the front surface has a very high recombination rate. In this case, a more heavily doped emitter may result in a net reduction in recombination in the combined emitter and surface regions because a more heavily doped emitter more effectively ‘shields’ minority carriers in the base from the surface of the cell under forward bias. Emitter sheet resistances less than approximately 80Ω/□ cause a reduction in $J_{sc}$ due to the formation of a ‘dead layer’; a region in which the probability of minority carrier collection is low. Lower wavelength, higher energy light is more likely to be absorbed in the emitter region, since this is closest to the surface. A cell with a very low emitter sheet resistance is therefore often described as having a poor ‘blue’ response [345].

The benefits of a lower sheet resistance are four-fold; there is a reduced series resistance in the emitter; there is reduced contact resistance between the silicon and the metal fingers; there is reduced recombination at the surface if the surface has a high recombination velocity (for example, at the metal contacts) and there is a reduced risk of shunting from the metal through the diffusion.

A compromise between high and low emitter sheet resistance can be reached with the use of a selective emitter. In this case, the blue response of the cell can be preserved while the contact resistance and recombination at the silicon/metal interface can be minimised. The higher doping, higher recombination rate areas are confined to the small volume under
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Saw damage etch</td>
<td>1:10 HF:HNO₃ To remove approximately 20μm from each side (usually ~5 minutes).</td>
</tr>
<tr>
<td>1a</td>
<td>KOH texturing step</td>
<td>(for wafers discussed in section 7.5 only). Described in section 7.5.2.</td>
</tr>
<tr>
<td>2</td>
<td>RCA (Radio Corporation America) clean</td>
<td>10 minutes in a 5:1:1 H₂O:NH₃:H₂O₂ solution plus 10 minutes in a 5:1:1 H₂O:HCl:H₂O₂ solution, both at 80°C.</td>
</tr>
<tr>
<td>3</td>
<td>HF dip</td>
<td>in 10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>4</td>
<td>Phosphorous diffusion on both sides</td>
<td>For section 7.3 details are given in section 7.3.1. Otherwise: 850°C (section 7.4) or 830°C (section 7.5) for 30 minutes with a main flow of N₂: 180l/hour. O₂: 130cc/min and N₂ through the POCl₃: 45cc/min. Rₛ: 600-1800Ω/□.</td>
</tr>
<tr>
<td>5</td>
<td>Phosphorous glass deglaze</td>
<td>10% HF solution until hydrophobic.</td>
</tr>
<tr>
<td>6</td>
<td>Oxidation</td>
<td>For thickness ≥100nm: 1100°C with TCA, thickness controlled by varying the time. For thickness ~25nm: 900°C for 60 minutes with TCA. For all: O₂ flow rate 100l/hour and 30 minute N₂ anneal before unloading at 1000°C (flow rate 100l/hour).</td>
</tr>
<tr>
<td>7</td>
<td>Forming gas anneal (FGA)</td>
<td>30 minutes at 400°C in forming gas (5% H₂ in Ar).</td>
</tr>
<tr>
<td>8</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>9</td>
<td>RCA clean and LPCVD nitride deposition</td>
<td>Deposition pressure 0.6torr, temperature 750°C. Flow ratio of DCS:NH₃ 1:4. Nitride thickness controlled by varying the deposition time.</td>
</tr>
<tr>
<td>10</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>11</td>
<td>RCA clean and nitrogen anneal</td>
<td>Anneal in N₂, flow rate 100l/hour. Varying temperature and time.</td>
</tr>
<tr>
<td>12</td>
<td>Lifetime measurement</td>
<td>Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
<tr>
<td>13</td>
<td>RCA clean and hydrogen re-introduction</td>
<td>(not for wafers discussed in section 7.3). Forming gas anneal at 840°C for various times.</td>
</tr>
<tr>
<td>14</td>
<td>Lifetime measurement</td>
<td>(not for wafers discussed in section 7.3). Using QSSPC apparatus, usually at 3 different light intensities.</td>
</tr>
</tbody>
</table>

**Table 7.1:** Processing steps for the wafers discussed in this chapter. The wafers used for sections 7.3 and 7.5, were 100-400Ωcm, p-type FZ in the case of the (100) orientated wafers and 500Ωcm, p-type FZ in the case of the (111) orientated wafers. Details of the wafers discussed in section 7.4 are given in section 7.4.1.
the metal contacts.

The effect of emitter sheet resistance on $J_{oc}$ after nitrogen anneals for wafers with an oxide/nitride stack was determined for sheet resistances of between 22–590Ω/□ (measured at the end of the process). The aim of this work was to determine if a heavier phosphorous diffusion could remove the need for hydrogen re-introduction.

### 7.3.1 Experimental Conditions

High resistivity float zone wafers were used for this work so that the effect of varying emitter sheet resistance could be clearly seen. Figure 7.1 shows the phosphorous diffusion recipes used to obtain the various emitter sheet resistances. In all cases, the diffusion was done for 30 minutes and the emitter sheet resistance was varied by varying the diffusion temperature. Table 7.2 shows the sheet resistances obtained. The oxide thickness was 22nm and the nitride thickness 39nm for all wafers.

![Recipe 1](image)

Recipe 1

![Recipe 2](image)

Recipe 2

**Figure 7.1:** The recipes used for the phosphorous diffusion. The ‘POCl₃’ flow is actually N₂ bubbled through a liquid POCl₃ source. $T_D$ is the diffusion temperature. Details of the emitter sheet resistances obtained with these recipes are given in table 7.2. These recipes are essentially the same, for diffusions at temperatures greater than 900°C; wafers were loaded at 900°C and the furnace was brought up to temperature before the diffusion gas was turned on.
Table 7.2: Emitter sheet resistances for the wafers used in this work. See figure 7.1 for the recipes. Measurements of sheet resistance were made at the end of the process, after all high temperature steps.

<table>
<thead>
<tr>
<th>Sheet resistance (Ω/□)</th>
<th>Diffusion temperature (°C)</th>
<th>Recipe number</th>
<th>Number of wafers</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>930</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>48</td>
<td>910</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>200</td>
<td>890</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>250</td>
<td>860</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>310</td>
<td>850</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>500</td>
<td>840</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>590</td>
<td>830</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

7.3.2 Results and Discussion

Figure 7.2 shows $J_{oe}$ values as a function of emitter sheet resistance for the wafers after oxide growth and at the end of the process with both the oxide and nitride removed. For the oxide passivated wafers, $J_{oe}$ values were higher for lower emitter sheet resistances, due to increased recombination in these more heavily doped regions. For the un-passivated wafers, (the ‘Bare silicon’ curve in figure 7.2) $J_{oe}$ values were lower for lower emitter sheet resistances. This is because the higher doping levels in this region partially shield the minority carriers from the surface. With higher emitter sheet resistances and no surface passivation, was more strongly influenced by recombination at the silicon/oxide interface.

After deposition of a 39nm thick nitride, these wafers were annealed in nitrogen for an hour each at 900°C, 950°C and 1000°C. The effect on $J_{oe}$ is shown in figure 7.3. The $J_{oe}$ for the wafers with lower emitter sheet resistances increased less after nitrogen anneal and for the sheet resistances of 22 and 48Ω/□, $J_{oe}$ values showed negligible change after the nitrogen anneal. Again, this is because the diffusion shields the minority carriers from the surface and $J_{oe}$ is dominated by recombination in the emitter rather than by recombination at the silicon/oxide interface.

The wafers with a sheet resistance of 590Ω/□ had a slightly rougher surface finish and so $J_{oe}$ values may be slightly higher than for a similar emitter sheet resistance on a polished wafer. All other wafers shown in figures 7.2 and 7.3 were highly polished. One possible interpretation of the results shown in figure 7.3 is that they indicate the relative amounts of dangling bond passivation provided by the oxide and the hydrogen.

From figure 7.3, the emitter sheet resistance that results in the lowest $J_{oe}$ value (in the absence of hydrogen re-introduction) can be estimated to be between 60–200Ω/□ for all anneal temperatures.
Figure 7.2: $J_{oc}$ as a function of sheet resistance after phosphorous diffusion, oxide growth and 400°C FGA (‘Oxide only’) and for the plain silicon wafer at the end of the process (‘Bare silicon’). The number of wafers measured with each emitter sheet resistance is indicated in table 7.2. Results for two wafers are an average value.
Varying Emitter Sheet Resistance

Figure 7.3: $J_{oe}$ as a function of emitter sheet resistance for wafers with a 22nm thick oxide and 39nm thick nitride. Values are shown with oxide only, after 1 hour anneals in nitrogen at 900, 950 and 1000°C and after removal of both the oxide and nitride. The same wafers were used for each nitrogen anneal and so the effect is cumulative. The emitter sheet resistance was measured at the end of the process. The number of wafers measured with each emitter sheet resistance is indicated in table 7.2. Results for two wafers are an average value.
7.4 Varying Resistivity and Dopant Type

Wafer resistivity is important as it influences both $V_{oc}$ and $J_{sc}$. With very high doping levels, the diffusion length decreases, leading to a reduction in both $V_{oc}$ and $J_{sc}$. Very low doping levels can also result in a reduction in $V_{oc}$, if a back surface field is not used. The optimum wafer resistivity will be dependent on the wafer characteristics and cell design.

This section presents the results of experiments done using oxide/nitride stacks on wafers of different resistivity and dopant type. The effect of nitride deposition and anneals in both nitrogen and forming gas on $J_{oc}$ and on the effective lifetime has been studied. The surfaces of the wafers were again lightly doped to enable a sensitive measurement of the silicon/oxide interface.

7.4.1 Experimental Conditions

For this work, wafers were prepared as described in table 7.1 using the wafers shown in table 7.3. The sheet resistance after phosphorous diffusion was 350$\Omega$/sq for p-type wafers and 385$\Omega$/sq for n-type wafers. Oxide thickness was 25nm and nitride thickness was 54 or 60nm in all cases.

<table>
<thead>
<tr>
<th>Wafer type (n or p)</th>
<th>Resistivity ($\Omega$cm)</th>
<th>Growth method</th>
<th>Wafer thickness ($\mu$m)</th>
<th>Nitride thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>100–400</td>
<td>FZ</td>
<td>460</td>
<td>54</td>
</tr>
<tr>
<td>p</td>
<td>5–12</td>
<td>unknown</td>
<td>360</td>
<td>54</td>
</tr>
<tr>
<td>p</td>
<td>1</td>
<td>Cz</td>
<td>225</td>
<td>60</td>
</tr>
<tr>
<td>p</td>
<td>0.4</td>
<td>FZ</td>
<td>250</td>
<td>60</td>
</tr>
<tr>
<td>n</td>
<td>500–900</td>
<td>FZ</td>
<td>260</td>
<td>54</td>
</tr>
<tr>
<td>n</td>
<td>10</td>
<td>unknown</td>
<td>190</td>
<td>54</td>
</tr>
<tr>
<td>n</td>
<td>0.5–3</td>
<td>FZ</td>
<td>295</td>
<td>60</td>
</tr>
<tr>
<td>n</td>
<td>0.4–0.6</td>
<td>Cz</td>
<td>620</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 7.3: The different resistivity and type material used for the experiments described in section 7.4. All wafers were (100) orientated.

7.4.2 Results and Discussion

Nitride Deposition

Figures 7.4 and 7.5 show effective lifetime curves before and after silicon nitride deposition for the different resistivity p and n-type material, respectively. For both dopant types, the high resistivity wafers were unaffected by nitride deposition. For the lower resistivity p-type material, effective lifetimes had decreased slightly after nitride deposition and for the lower resistivity n-type material, effective lifetimes had increased significantly after
nitride deposition.

![Graphs showing effective lifetime curves before and after nitride deposition for different resistivity p-type material.](image)

**Figure 7.4:** Effective lifetime curves before and after nitride deposition for the different resistivity p-type material. The ‘after oxide growth’ curve is after light phosphorous diffusion (350Ω·cm), thin oxide growth (25nm) and 400°C FGA. The ‘after nitride deposition’ curve was for the same wafers, measured immediately after nitride deposition. The nitride was 54nm thick for the 100–400 and 5–12Ω·cm wafers and 60nm thick for the 1 and 0.4Ω·cm wafers.

These results suggest that, with the lower resistivity material, the nitride deposition had a different effect on p-type and n-type material. Since the deposition was done at 750°C and the wafers had already experienced a 1000°C anneal (directly after the oxidation) the change in effective lifetimes was associated with the nitride deposition, not the high temperatures. It is possible that the effect was due to the diffusion of atomic hydrogen into the silicon bulk and that the net effect was different for the different dopant types.

For the 1Ω·cm p-type material and the 0.4–0.6Ω·cm n-type material, both grown using the Czochralski method, the apparently high lifetimes at low injection levels are due to trapping of minority carriers. Trapping was reported in 1955 in p-type single crystalline silicon by Hornbeck and Haynes [153] and in n-type single crystalline silicon by Haynes and Hornbeck [142]. More recently, trapping has been described in multi-crystalline silicon by Macdonald and Cuevas [200]. Recently Schmidt et al. [275] suggested that traps in p-type Cz material are associated with oxygen atoms. At least some of the traps in the n-type material shown in figure 7.5 appear to have been passivated during the nitride deposition.
Figure 7.5: Effective lifetime curves before and after nitride deposition for the different resistivity n-type material. The ‘after oxide growth’ curve is after light phosphorous diffusion (385Ω/□), thin oxide growth (25nm) and 400°C FGA. The ‘after nitride deposition’ curve was for the same wafers, measured immediately after nitride deposition. The nitride was 54nm thick for the 500–900 and 10Ωcm wafers and 60nm thick for the 0.5–3 and 0.4–0.6Ωcm wafer.
High Temperature Anneals in Nitrogen and Forming Gas - Higher Resistivities

Figure 7.6 shows the effect of nitride deposition, nitrogen anneal and high temperature forming gas anneal on \( J_{oe} \) for the 5–12\( \Omega \)cm and 100–400\( \Omega \)cm p-type wafers. After the anneals in nitrogen and forming gas, the 5–12\( \Omega \)cm wafers had slightly lower \( J_{oe} \) values than the 100–400\( \Omega \)cm wafers, but this may be the result of variations in emitter sheet resistance and in surface roughness. After high temperature FGA, \( J_{oe} \) values had decreased for all wafers.

Figure 7.6: \( J_{oe} \) values for the 100–400 and 5–12\( \Omega \)cm p-type wafers after phosphorous diffusion, oxide growth and 400\(^\circ\)C FGA (‘oxide’), nitride deposition (‘nitride’), 1 hour anneal in nitrogen at 900\(^\circ\)C or 1000\(^\circ\)C (‘N2 anneal’) and a forming gas anneal at 840\(^\circ\)C for 1 hour (‘FGA’). The solid lines represent wafers annealed in nitrogen at 900\(^\circ\)C and the dotted lines represent wafers annealed in nitrogen at 1000\(^\circ\)C.

Figure 7.7 shows the effect of nitride deposition, nitrogen anneal and high temperature forming gas anneals on \( J_{oe} \) for the 500–900\( \Omega \)cm and 10\( \Omega \)cm n-type material. The 10\( \Omega \)cm wafers clearly had a lower \( J_{oe} \) after both nitrogen anneal and forming gas anneal than the 500–900\( \Omega \)cm wafers. The n-type wafers showed the same general response to anneals in nitrogen and in forming gas as the p-type wafers, probably because the silicon/oxide interface was similar for both wafer types. There was a significant difference in \( J_{oe} \) values after the FGA for the wafers that were annealed at 1000\(^\circ\)C in nitrogen. The reason for this difference is not clear at present.

The high resistivity n-type wafer that was annealed in nitrogen at 1000\(^\circ\)C was given a second FGA at 840\(^\circ\)C for 4.5 hours and the result is shown in figure 7.8. \( J_{oe} \) recovery
to the original value was demonstrated, implying that the silicon/oxide interface for the high resistivity n-type material behaves similarly to the interface for the high resistivity p-type material.

**High Temperature Anneals in Nitrogen and Forming Gas - Lower Resistivities**

$J_{oc}$ values could not easily be separated from bulk lifetimes for the lower resistivity material. The effects of nitrogen anneal and high temperature forming gas anneal on these wafers have therefore been assessed using effective lifetime curves. Figure 7.9 shows effective lifetime curves for the 1Ωcm and 0.4Ωcm p-type wafers after nitride deposition, 1 hour anneal in nitrogen at 1000°C and a 1 hour anneal in forming gas at 840°C. For both wafers, effective lifetimes were degraded by the nitrogen anneal and recovered, to some extent, by the forming gas anneal. The trapping evident in the p-type 1Ωcm wafer apparently persisted through the various processes.

Figure 7.10 shows effective lifetime curves for the 0.5–3Ωcm and 0.4–0.6Ωcm n-type wafers after nitride deposition, 1 hour anneal in nitrogen at 1000°C and a 1 hour anneal in forming gas at 840°C. Once again, effective lifetimes were degraded by the nitrogen anneal and recovered, to some extent, by the forming gas anneal. The traps evident in
Figure 7.8: $J_{ce}$ values for the 500-900Ωcm n-type material. Values are shown after phosphorus diffusion, oxidation and 400°C FGA (‘oxide’), after nitride deposition (‘nitride’), after a 1 hour anneal in nitrogen at 1000°C (‘N2 anneal’), after the first forming gas anneal, at 840°C for 1 hour (FGA 1) and after the second forming gas anneal, at 840°C for 4.5 hours (FGA 2).

Figure 7.9: Effective lifetime curves for the 1Ωcm and 0.4Ωcm p-type wafers after nitride deposition (60nm), anneal in nitrogen (1 hour at 1000°C) and anneal in forming gas (1 hour at 840°C).
Figure 7.10: Effective lifetime curves for the 0.5–3Ωcm and 0.4–0.6Ωcm n-type wafers after nitride deposition (60nm), anneal in nitrogen (1 hour at 1000°C) and anneal in forming gas (1 hour at 840°C).

Figure 7.5 for the 0.4–0.6Ωcm wafer appeared to be passivated after the nitride deposition and did not recur after the high temperature nitrogen or forming gas anneals. This is particularly interesting given that trapping was still evident for the 1Ωcm p-type wafer after nitride deposition. It is possible that atomic hydrogen passivated the traps in the n-type material, but not in the p-type material.

Surface Versus Bulk

Following the high temperature FGA, the oxide and nitride were stripped from these wafers and the surface was re-passivated with a 25nm thick oxide and 400°C FGA. Table 7.4 shows $J_{oc}$ values both initially (after oxide growth, but before nitride deposition) and after the re-passivation step for the higher resistivity wafers. They were equivalent for all of the wafers, supporting the view that the higher $J_{oc}$ values after the nitrogen anneal can be attributed to a lack of hydrogen at the silicon/oxide interface.

The effective lifetime curves at the beginning and end of the process are compared in figures 7.11 and 7.12 for p and n-type wafers, respectively. The results are shown for the wafers that had the 1000°C nitrogen anneal. Wafers that had the 900°C anneal showed a similar general response. The lowest resistivity wafers (both p and n-type) are not shown.
Table 7.4: $J_{oc}$ values for the higher resistivity n and p-type wafers after initial oxidation compared with values after removal of the oxide and nitride and re-passivation.

<table>
<thead>
<tr>
<th>Dopant type</th>
<th>Wafer resistivity ($\Omega \text{cm}$)</th>
<th>Growth method</th>
<th>N$_2$ anneal temperature ($^\circ$C)</th>
<th>Initial $J_{oc}$ (fA/cm$^2$/side)</th>
<th>Re-passivated $J_{oc}$ (fA/cm$^2$/side)</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>100–400</td>
<td>FZ</td>
<td>900</td>
<td>14</td>
<td>15</td>
</tr>
<tr>
<td>p</td>
<td>100–400</td>
<td>FZ</td>
<td>1000</td>
<td>18</td>
<td>12</td>
</tr>
<tr>
<td>p</td>
<td>5–12</td>
<td>unknown</td>
<td>900</td>
<td>16</td>
<td>13</td>
</tr>
<tr>
<td>p</td>
<td>5–12</td>
<td>unknown</td>
<td>1000</td>
<td>17</td>
<td>15</td>
</tr>
<tr>
<td>n</td>
<td>500–900</td>
<td>FZ</td>
<td>900</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>n</td>
<td>500–900</td>
<td>FZ</td>
<td>1000</td>
<td>12</td>
<td>13</td>
</tr>
<tr>
<td>n</td>
<td>10</td>
<td>unknown</td>
<td>900</td>
<td>13</td>
<td>14</td>
</tr>
<tr>
<td>n</td>
<td>10</td>
<td>unknown</td>
<td>1000</td>
<td>16</td>
<td>13</td>
</tr>
</tbody>
</table>

because they were not stripped and re-passivated.

For the Cz wafer (p-type, 1$\Omega$cm) and both wafers of unknown growth method (p-type 5–12$\Omega$cm and n-type 10$\Omega$cm), the effective lifetimes at the end of the process were considerably reduced. It is likely that the material of unknown growth method was Cz. From this experiment alone, it is not possible to conclude whether the reduction in effective lifetimes was due to the presence of the silicon nitride during the high temperature nitrogen anneal, to hydrogen in the 840$^\circ$C FGA or to the thermal treatment.

Effective lifetimes at the end of the process were slightly higher for the n-type, high resistivity, FZ material. Further experiments could be done to determine if this is a statistically significant effect and if so, if it is due to the high temperature FGA. For the p-type, high resistivity FZ material, effective lifetimes after re-passivation were slightly lower compared to after the initial oxidation. The drop was comparable to that seen previously with similar wafers, for example, in figure 5.3.

For the low resistivity float zone material (n-type, 0.5–3$\Omega$cm), the improvement in effective lifetimes after nitride deposition persisted through the various high temperature treatments so that the effective lifetimes at the end of the process were significantly higher than after the initial oxidation. This is a very interesting and possibly useful result. It may be due to passivation of the bulk by atomic hydrogen.

7.4.3 Varying Resistivity and Dopant Type: Conclusions

Wafers with an oxide/nitride stack of both dopant types and all resistivities showed a drop in effective lifetimes after a high temperature nitrogen anneal. Complete recovery of $J_{oc}$ values for high resistivity, FZ, n-type wafers after a 1 hour, 1000$^\circ$C nitrogen anneal was demonstrated using a high temperature FGA.

After removal of the oxide/nitride stack and re-passivation, the effective lifetime of
Figure 7.11: Effective lifetime curves for the p-type material at the beginning and end of the process. Values are shown after phosphorous diffusion, oxidation and 400°C FGA (‘oxide 1’) and again after nitride deposition, 1 hour anneal in nitrogen at 1000°C, high temperature FGA and after the oxide and nitride were stripped and the surface re-passivated with a 25nm thick oxide and 400°C FGA (‘oxide 2’).
**Figure 7.12:** Effective lifetime curves for the n-type material at the beginning and end of the process. Values are shown after phosphorous diffusion, oxidation and 400°C FGA (‘oxide 1’) and again after nitride deposition, 1 hour anneal in nitrogen at 1000°C, high temperature FGA and after the oxide and nitride were stripped and the surface re-passivated with a 25nm thick oxide and 400°C FGA (‘oxide 2’).
the two n-type, FZ wafers had improved. This improvement was remarkable in the case of the 0.5–3Ωcm wafer and was possibly due to passivation of the bulk by atomic hydrogen. Effective lifetimes of the Cz material and the material of unknown growth method had dropped considerably. The material of ‘unknown’ growth method was probably Cz. Some traps in the 0.4–0.6Ωcm n-type material appeared to be passivated after the nitride deposition, possibly as a result of atomic hydrogen present during the nitride deposition. This section of work raised a number of questions and further experiments are needed to understand the various changes in effective lifetime.

7.5 Wafers with a Textured Surface

Gains in solar cell efficiency can be realised by maximising the number of photons that are absorbed by a cell. Optimal results are achieved by combining an anti-reflection coating (ARC) with surface texturing, whereby reflected photons have a second (or further) chance of entering the cell. The texturing reported in this work was done using a KOH solution, which, on a (100) orientated surface, results in random, upright pyramids, with sides of (111) orientation.

This section is in two parts. Firstly, the effects of nitride deposition, nitrogen anneals and high temperature forming gas anneals on \( J_{oc} \) for planar silicon of (100) and (111) orientation are compared. Secondly, the effect of nitride deposition, nitrogen anneal and high temperature forming gas anneal on textured compared with planar wafers is discussed.

All wafers used for this work were p-type FZ. The (100) orientated wafers were 100–400Ωcm and the (111) orientated wafers were 50Ωcm. The wafers were prepared as shown in table 7.1. The emitter diffusion was again very light in order to increase the sensitivity to surface passivation. Oxide growth rate is different on (100) compared with (111) orientated silicon. For thick oxides, the thickness for both orientations was estimated using the colour thickness charts. On the (100) orientated wafers, the thickness of the thin oxides was measured using a polished test wafer and the Filmetrics system. On the (111) orientated wafers, the thickness of the thin oxides was estimated using the measured thickness on the (100) orientated wafer and standard graphs of oxide growth [169].

7.5.1 A Comparison of (100) and (111) Orientated Wafers

Figure 7.13 shows \( J_{oc} \) values after nitride deposition, nitrogen anneal (at 900 and 1000°C) and high temperature forming gas anneal for (100) and (111) orientated wafers. With both crystallographic orientations, there was a rise in \( J_{oc} \) after the nitrogen anneal. As expected, for the (100) orientated wafers, \( J_{oc} \) was higher for the wafer annealed at 1000°C. For the
(111) wafers, $J_{oe}$ values after nitrogen anneals were the same for both anneal temperatures. This implies that, for the (111) orientated wafers, all of the available hydrogen had been removed from the silicon/oxide interface after the 1 hour, 900°C nitrogen anneal.

This experiment did not produce very clear results. The (111) orientated wafers had a relatively low bulk lifetime, and the relatively high $J_{oe}$ values measured for these wafers after initial oxidation and nitride deposition may have been dominated by recombination in the emitter region. The maximum effective lifetime after oxidation was only 300$\mu$s compared with 8.6ms for the (100) orientated wafers. In spite of this, the high $J_{oe}$ values after the nitrogen anneal are likely to be predominantly due to high recombination rates due to the lack of hydrogen. Therefore, the results shown in figure 7.13 suggest that, after the nitrogen anneal, the (111) orientated wafers had a higher surface recombination rate. The (100) orientated wafers behaved as expected, except for the slight increase in $J_{oe}$ after the 4 hour FGA for the wafer that had been annealed in nitrogen at 1000°C. It is unlikely that this was caused by contaminants in the forming gas since all wafers were processed together.

After the first FGA, $J_{oe}$ values for both (100) orientated wafers had decreased, as
expected. For the (111) orientated wafers, \( J_{oc} \) had decreased for the wafer annealed at 900°C, but remained unchanged for the wafer annealed at 1000°C. On its own, this result implies that the (111) orientated surface took longer to passivate with molecular hydrogen than the (100) orientated surface. After the second FGA, the \( J_{oc} \) value of the (111) orientated wafer annealed at 1000°C had decreased, which could be expected. The unchanged \( J_{oc} \) of the (111) orientated wafer annealed in nitrogen at 900°C after this second FGA is less easy to explain. Further investigation is necessary to determine if this is a real effect.

In conclusion, it is likely that similar mechanisms are occurring at a silicon/oxide interface under a nitride layer for both (100) and (111) orientated silicon. It is likely that hydrogen is removed from both interfaces with high temperature anneals in a nitrogen ambient and that, at least in some cases, it can be reintroduced with high temperature anneals in a forming gas ambient. The difference in quality of the (111) and (100) wafers used for this work makes any deeper comparisons less rigorous.

### 7.5.2 KOH Texturing

KOH texturing was done on (100) orientated wafers and produced upright, square-based pyramids with (111) orientated facets and a base length mostly in the range 5–10\( \mu \)m. Figure 7.14 shows a wafer after KOH texturing. There were four texturing steps;

- 20 minutes in a 10% KOH solution at 80°C;
- 1 minute in a 44% KOH solution at 90–100°C;
- 30 minutes in a 3% KOH solution with added isopropanol at 75°C and
- 20 seconds in a 1:20 HF:HNO\(_3\) solution, to round off the edges slightly and remove any contaminants.

### 7.5.3 Textured Wafers

In studying the effect of oxide/nitride stacks with textured wafers, firstly, the effect of nitride deposition, nitrogen anneal and high temperature forming gas anneal on \( J_{oc} \) was determined for textured, compared with planar wafers with a thick oxide. Secondly, the effect of oxide thickness and nitrogen anneal temperature on \( J_{oc} \) for textured wafers was determined. Oxide thickness was supposed to be important based on the results from section 5.8. The planar wafers referred to in this section were (100) orientated.
Figure 7.14: A scanning electron microscope image of a wafer after KOH texturing. The original wafer was (100) orientated.

Effect of Planar Compared with Textured Wafers

Figure 7.15 shows $J_{oc}$ values for a planar compared with textured wafer with an oxide/nitride stack. After passivation with a light phosphorous diffusion (1400Ω/□, measured immediately after diffusion), thick oxide (225 and 250nm on the planar and textured wafers, respectively) and 400°C FGA, both wafers had low $J_{oc}$ values. After nitride deposition (21nm thick) there was very little change in $J_{oc}$ values. After a nitrogen anneal (at 900°C for 1 hour) $J_{oc}$ values had increased for both wafers, the textured wafer to a slightly greater extent than the planar wafer. The value for the textured wafer is higher than the limit described in equation 4.20 and hence it is possible that this $J_{oc}$ value is underestimated. This would imply that the recombination rates were higher for the (111) orientated surfaces on the textured wafer. After a total of 6 hours in forming gas at 840°C, $J_{oc}$ values had recovered to approximately original values for both wafers. The planar wafer had a much faster recovery in forming gas than the textured wafer. This may indicate that a longer time was required to passivate the (111) surfaces using molecular hydrogen.

Effect of Oxide Thickness

To determine the effect of oxide thickness on $J_{oc}$ for textured wafers with an oxide/nitride stack, four different oxide thicknesses were used. These were approximately: 40nm, 75nm, 125nm and 250nm. Figure 7.16 shows the $J_{oc}$ values for these wafers at various stages.
Figure 7.15: $J_{se}$ values for a textured wafer compared with a polished wafer. The oxide was thick, approximately 225nm for the planar wafer and 250nm for the textured wafer. The nitride was approximately 21nm thick. ‘Oxide’ refers to the wafers after light phosphorous diffusion, oxidation and 400°C FGA. ‘Nitride’ refers to the wafers immediately after nitride deposition. The nitrogen anneal was done for 1 hour at 900°C and the forming gas anneals were done at 840°C for the indicated times. The sheet resistance after phosphorous diffusion was 1400Ω/□, and probably reduced to approximately 300Ω/□ after oxidation.
The wafers with the 40 and 250nm thick oxides were processed together and the nitride was 65nm thick. The wafers with the 75 and 125nm thick oxides were processed together and the nitride was 72nm thick. Nitrogen anneals were done for 1 hour at 900°C for all wafers. Once again, the $J_{\text{oc}}$ values after the nitrogen anneal were much higher than can accurately be determined for most wafers. It is clear, however, that passivation at the silicon/nitride interface was extremely poor at this point.

These results are similar to what might be expected for planar, (100) orientated wafers, except in the case of the 40nm thick oxide. The wafers with the thicker oxides recovered to approximately the same point and it is possible that the small variations were due to variations in the emitter sheet resistance and/or a result of being processed in different batches. For the wafer with the 40nm thick oxide, there was very little change in $J_{\text{oc}}$ after the high temperature FGA. Section 7.5.3 describes the result of an experiment to determine if this was a surface effect or due to bulk damage.

The slight increase in $J_{\text{oc}}$ for the wafer with the 250nm thick oxide after the 30 minute FGA is difficult to explain. The anneal time was probably too short for hydrogen to diffuse through the nitride (since no decrease in $J_{\text{oc}}$ was observed for any of the wafers). It is therefore possible that the higher temperatures resulted in the loss of more hydrogen from the silicon/nitride interface but since hydrogen from the ambient gas was not yet available at the interface, the hydrogen was not replaced and $J_{\text{oc}}$ increased.

**Bulk versus Surface Effect**

The wafers shown in figure 7.16 were annealed in nitrogen at 900°C. A similar lack of $J_{\text{oc}}$ recovery was seen for a second textured wafer with a 40nm thick oxide that was annealed in nitrogen at 1000°C, suggesting that the lack of response is a real effect, rather than an artifact of such a small sample size. To determine if the bulk of the wafer shown in figure 7.16 with the thin oxide had degraded, the oxide and nitride were stripped from the surfaces and they were re-passivated with a second 40nm thick oxide and a 400°C FGA. The results are shown in figure 7.17. These results show that the maximum effective bulk lifetime had dropped, but remained relatively high and the drop was comparable to that seen for the polished, (100) orientated wafers shown in figure 5.3. With this repassivation step, $J_{\text{oc}}$ decreased to 23fA/cm$^2$/side (compared with 17fA/cm$^2$/side after the initial oxidation), consistent with the view that the high $J_{\text{oc}}$ values seen in figure 7.16 were due to a lack of hydrogen at the silicon/nitride interface. The current hydrogen loss model does not explain the effect of a textured wafer with a thin oxide. It may be that with the (111) orientated surfaces, hydrogen bonds are broken at lower temperatures and a lower temperature FGA is required to reduce $J_{\text{oc}}$ values. This suggestion is supported
Figure 7.16: $J_{oc}$ values for textured wafers with oxide thicknesses as shown in the legend. The wafers with the 40 and 250nm thick oxides were processed together and had a 65nm thick nitride and an emitter sheet resistance of 1260Ω/□ immediately after phosphorous diffusion. The wafers with the 75 and 125nm thick oxide were processed together and had a 72nm thick nitride and an emitter sheet resistance of 1610Ω/□ immediately after the phosphorous diffusion. ‘Oxide’ refers to the wafers immediately after light phosphorous diffusion, oxidation and 400°C FGA and ‘nitride’ refers to the wafers immediately after nitride deposition. The nitrogen anneal was done at 900°C for 1 hour and the forming gas anneals were done at 840°C for the indicated times.
Figure 7.17: Irreversible influence of nitrogen anneal on effective lifetime for a textured silicon wafer with a thin oxide under a relatively thick nitride. The initial oxide thickness was 25nm and the nitride thickness was 65nm. The wafer underwent a nitrogen anneal for 1 hour at 900°C. The oxide and nitride were then stripped and a second, 25nm thick oxide was grown. Two data sets are shown. The ‘o’ marks represent wafers after light phosphorus diffusion, first oxide growth and 400°C FGA. The ‘x’ marks represent the same wafer after subsequent nitride deposition, nitrogen anneal, oxide/nitride removal, second oxidation and 400°C FGA.

by the results shown in figure 7.16 where there was a slight increase in $J_{oc}$ after a 30 minute FGA at 840°C for the wafer with the 250nm thick oxide, but this does not explain why $J_{oc}$ values were recovered for the wafers with the thicker oxides. Another possibility is that with the thinner oxide, a greater number of surface states were created at the (111) silicon/oxide interface and these could not be passivated with molecular hydrogen.

Effect of Nitrogen Anneal Temperature

Figure 7.18 shows textured wafers with 75 or 125nm of oxide and 72nm of nitride that were annealed in nitrogen at 900°C and 1000°C. As was seen with polished (111) orientated wafers, $J_{oc}$ values after nitrogen anneal were similar at both temperatures, possibly because the hydrogen bonds at a (111) silicon/oxide interface were broken more easily than the hydrogen bonds at a (100) silicon/oxide interface and hence all the hydrogen was removed after an hour long anneal at 900°C. After the second high temperature forming gas anneal, nitrogen anneal temperature did appear significant; both wafers that were annealed in nitrogen at 900°C had recovered further than those annealed in nitrogen at 1000°C. After
The oxide measurement was made after light phosphorous diffusion, oxidation and 400°C FGA. The nitride measurement was made immediately after nitride deposition. The nitrogen anneals were done for 1 hour at the temperature shown on the legend. High temperature FGA were done at 840°C for the indicated time. The sheet resistance after phosphorous diffusion was 1610Ω/□ for these wafers.

a further 4 hours in forming gas at 840°C, all wafers had recovered to approximately the same point. The greater time required to introduce hydrogen through a silicon nitride layer annealed at 1000°C is probably caused by the increased nitride density resulting from the 1000°C nitrogen anneal.

7.5.4 Textured Wafers: Comparison to King

The results described in this section should be compared with those reported by King [183]. King also used high resistivity (100) orientated FZ wafers and investigated the effect of high temperature forming gas anneals for textured compared with planar wafers with an oxide/nitride stack. A major difference between the work done by King and that reported here is that King was aiming to deposit a ‘low stress’ nitride and therefore used a very high flow ratio for the DCS to NH₃ of 6. (For the work done here the ratio was 0.25). This would have resulted in a silicon rich silicon nitride that is likely to have had different properties (possibly including significant absorption of light) compared with the nearly stoichiometric silicon nitride used in this work.

After nitride deposition, King found that lifetimes were too low to measure for both polished and textured wafers. King was able to substantially recover lifetimes of planar,
7.5.5 Textured Wafers: Conclusions

There was a slight decrease in $J_{\infty}$ for textured wafers after nitride deposition with thick oxides. No difference in $J_{\infty}$ after nitrogen anneals at 900 or 1000°C was discerned. The difference between the nitrogen anneal temperatures was apparent after a high temperature forming gas anneal. Recovery of textured wafers using a high temperature forming gas anneal was found to be dependent on oxide thickness. For a textured wafer with a 40nm thick oxide and a 65nm thick nitride, $J_{\infty}$ values were not recovered with an 840°C FGA. This was shown to be due to a lack of passivation at the silicon/oxide interface. Other methods or forming gas anneals at lower temperatures should be tried as a hydrogen re-introduction method for textured wafers with thin oxides.

7.6 Hydrogen Loss Model Revisited

At this point it is pertinent to revisit the hydrogen loss model, originally introduced in section 5.4.

In both the silicon and the silicon oxide, hydrogen solubility is relatively low and the diffusion coefficient is high [20, 35, 122]. Neither of these regions act as a significant hydrogen reservoir or as a diffusion barrier to hydrogen. The silicon/oxide interface and the silicon nitride are therefore the regions of primary interest. There are two aspects to consider;

- removal of hydrogen from the region and
- re-introduction of hydrogen to the region.

These two aspects are considered firstly for the silicon/oxide interface and secondly for the silicon nitride. Hydrogen concentrations at the silicon/oxide interface were inferred from the measurements of $J_{\infty}$. This is probably one of the more sensitive ways to measure the very small quantity of hydrogen present at the silicon/oxide interface.

7.6.1 The Silicon/Silicon Oxide Interface

Hydrogen Removal

At the silicon/oxide interface, hydrogen loss is governed by the rate at which hydrogen bonds are broken. Hydrogen bonds are broken more readily at higher temperatures and
as long as there is no supply of hydrogen to the interface, with increasing temperature, 
$J_{oc}$ values will continue to increase until all of the bonds have been broken and all of the 
hydrogen has diffused away from the interface. This situation was approximated by a 
wafer with a thin silicon nitride layer that was annealed in a nitrogen ambient, as shown 
in figure 5.7.

**Hydrogen Re-introduction**

The amount of hydrogen that remains at the silicon/oxide interface after a high tempera-
ture anneal will be dependent on a number of factors, including:

- the diffusion of hydrogen to this area from or through the nitride;
- the diffusion of hydrogen away from this area into the silicon;
- the hydrogen capture cross-section of dangling bonds at the silicon/oxide interface 
  and
- the relative rates at which hydrogen bonds form and break at the silicon/oxide 
  interface.

These factors are, in turn, influenced by a number of factors, including:

- the anneal temperature;
- the anneal time;
- the thickness of the nitride;
- the hydrogen concentration in the ambient gas;
- the initial hydrogen concentration in the oxide/nitride stack system;
- the surface structure of the silicon (including crystal orientation and the number of 
  surface states) and
- the cooling rate after the anneal.

The case of high temperatures and variable hydrogen supply was illustrated by anneal-
ing wafers with varying nitride thicknesses in a nitrogen ambient. The hydrogen supply 
was the nitride and the results appear in figure 5.10 for an anneal at 900°C. This figure 
shows that, even with an anneal at 900°C, $J_{oc}$ values may remain low provided the nitride 
is of sufficient thickness to be a substantial hydrogen reservoir. (Figure 5.11 shows the
same wafers after an additional anneal at 1000°C when all of the hydrogen had probably been removed and the nitride no longer acted as a reservoir).

The competition between removal of hydrogen from the silicon/oxide interface due to bonds breaking at high temperature and the re-introduction of hydrogen, through a nitride layer, from a forming gas ambient was illustrated by using a wafer with an oxide/nitride stack that did not have a nitrogen anneal (to remove the hydrogen), but did have a forming gas anneal. These results appear in figure 6.3 and show an increase in $J_{\text{on}}$ values for higher temperature forming gas anneals. The results shown in this figure are probably specific to the particular oxide thickness, nitride thickness and gas composition. They show that, for these conditions, at 840°C, the removal of hydrogen from the interface was only slightly faster than the re-introduction. At higher temperatures, there was a net loss of hydrogen from the silicon/oxide interface.

### 7.6.2 The Silicon Nitride

#### Hydrogen Removal

In the silicon nitride, hydrogen profiles have been measured, using nuclear reaction analysis, after deposition and after anneals in nitrogen and forming gas by Habraken et al. [134] and Xie et al. [349]. The salient points are that:

- hydrogen profiles are uniform throughout the nitride and
- hydrogen loss from an LPCVD silicon nitride is governed by bond breaking, not diffusion.

Habraken et al. measured the hydrogen concentration for an 80nm thick silicon nitride on a thermally grown silicon oxide of less than 29nm thickness. Profiles were measured after nitride deposition, after 1.5 hour anneals in a vacuum at 900 and 1000°C (comparable to the anneals in nitrogen discussed in this thesis) and after a 1 hour anneal in a 7% hydrogen-in-nitrogen ambient at 1000°C. Xie et al. measured hydrogen concentrations in a 150nm thick LPCVD silicon nitride on a 100nm thick CVD silicon oxide. Profiles were measured after nitride deposition, after a 30 minute anneal in a 3% hydrogen-in-argon ambient at 450°C and after a 30 second rapid thermal anneal in oxygen at 1000°C. In all cases, the hydrogen profile through the silicon nitride was found to be uniform, which implies that, in the nitride, hydrogen loss is limited by bond breaking, rather than by diffusion [134]. If diffusion were the rate limiting step, then a concentration gradient would exist.
Figure 7.19 shows possible hydrogen profiles through an oxide/nitride stack on silicon after deposition and after subsequent anneals in nitrogen. It is based on measurements made by Habraken et al. [134] and Xie et al. [349]. Part a) of figure 7.19 shows the situation immediately after deposition of the nitride. The concentration of hydrogen in the nitride is uniform and high (approximately 2–10 atomic% [134, 295, 296]). The concentration at the silicon/oxide interface is high and surface passivation is unaffected by nitride deposition. Part b) shows the situation after an anneal in a high temperature nitrogen ambient. The hydrogen concentration in the nitride remains uniform, but is decreased. The hydrogen concentration at the silicon/oxide interface is also decreased. Part c) shows the situation after a nitrogen anneal at a higher temperature than used for part b). Hydrogen is almost completely removed from the silicon/oxide interface and levels are low, but uniform, in the nitride. (For a 1.5 hour anneal in a vacuum at 1000°C, Habraken et al. [134] observed that the hydrogen concentration dropped from approximately 3 atomic % after deposition to approximately 0.3 atomic %). As mentioned earlier, the relative rates of increase and decrease in hydrogen concentration levels at the silicon/oxide interface will also be influenced by the nitride thickness, since the nitride acts as a limited hydrogen source.

**Hydrogen Re-introduction**

Hydrogen movement through the nitride is important as it influences the amount that reaches the silicon/oxide interface. Diffusion of hydrogen through the silicon nitride is complicated by the reaction of hydrogen with the nitride. It is, however, illuminating to first consider the simple case where hydrogen does not react with the nitride. Assuming also that the hydrogen comes from an unlimited supply, then the surface concentration is constant, which will result in error function concentration profiles in the nitride.

Assuming firstly a constant nitride thickness, constant temperature and only one diffusing species, then figure 7.20 shows possible hydrogen profiles at successively later times. With L equal to the diffusion length for a given time and W equal to the nitride thickness, the profiles are shown for the cases where L/W<1 (curve a), L/W≈1 (curve b) and L/W>1 (curve c). If measurements of \( J_{oc} \) were made at three times where, for the first two, L/W<1, but for the third, L/W>1, then a step-function improvement in \( J_{oc} \) would be seen. At the other extreme, if the three measurements were all made with L/W>1, then a gradual improvement in \( J_{oc} \) values would have been seen (assuming \( J_{oc} \) values were not completely recovered after time 1).

As stated, the three curves shown in figure 7.20 could represent diffusion of the same species in the same material at different times. It is also possible to move from a situation where L/W<1 (curve a) to a situation where L/W>1 (curve c) either by decreasing the
Figure 7.19: Possible hydrogen profiles for the removal of hydrogen from an oxide/nitride stack on silicon. Part a) shows the situation immediately after nitride deposition, part b) after a high temperature anneal in nitrogen and part c) after a second (higher temperature) anneal in nitrogen. The profiles in the nitride are inferred, based on the results of Habraken et al. [134] and Xie et al. [349].
Figure 7.20: Possible hydrogen profiles for the re-introduction of hydrogen to the silicon/oxide interface through a nitride layer. The three curves indicate three different times, of increasing length. For this scenario, only time c results in an appreciable increase in hydrogen levels at the silicon/oxide interface. Curve a illustrates the situation where $L/W < 1$, curve b where $L/W \approx 1$ and curve c where $L/W > 1$.

nitride thickness or by increasing the diffusion coefficient. A different diffusion coefficient could be realised with:

- a different diffusing hydrogen species, for example atomic versus molecular hydrogen;

- a different temperature or

- a change in the properties of the nitride layer (for example, silicon nitride is more dense after anneals at higher temperatures due to an increased density of Si–N and N–N bonds).

Figure 6.11 showed that a 15 minute, 400°C ammonia plasma treatment reduced $J_{sc}$ for a wafer previously annealed at 900°C (but not at 1000°C). The hydrogen reaching the interface can be assumed to be atomic because the temperature was only 400°C and it was shown previously that with a molecular hydrogen source at 400°C, hydrogen did not diffuse through the nitride. These results imply that, at 400°C, atomic hydrogen diffuses more readily through the nitride than molecular hydrogen. The hydrogen reaching the silicon/oxide interface can be assumed to be directly from the plasma because Si–H and N–H bonds are not broken at 400°C [295], and so hydrogen in the nitride (or hydrogen from the plasma that was subsequently incorporated into the nitride) would not have been released. For the wafers shown in figure 6.11 that were annealed at 900°C, it is therefore
likely that, for these times, \( L/W > 1 \). For the wafer annealed at 1000°C, significant amounts of hydrogen did not reach the silicon/oxide interface. It is possible that this was because:

- the nitride structure was different (denser due to the higher temperature anneal) and meant that \( L/W < 1 \) or

- diffusion was prevented because the hydrogen concentration in the nitride had not reached a sufficient level to allow diffusion through to the oxide.

In reality, diffusion of hydrogen through the nitride is complicated because the hydrogen reacts with the nitride. The measurements reported in this thesis were concerned with hydrogen levels at the silicon/oxide interface. Direct measurements of hydrogen levels in the nitride were not made. Hydrogen from both atomic and molecular sources will be incorporated into the nitride (as evidenced by the fact that a molecular hydrogen source can be used to increase bonded hydrogen levels in the nitride after they have been reduced during a high temperature anneal [295]). At elevated temperatures, \( \text{N-H} \) and \( \text{Si-H} \) bonds in the nitride will be broken and formed simultaneously. Starting from a nitride that has been depleted of hydrogen, levels will increase to a steady-state value, which will depend on the temperature. The solubility of hydrogen in silicon nitride therefore directly affects the diffusion of hydrogen through the nitride to the silicon/oxide interface.

In conclusion, two salient points may be made about hydrogen re-introduction through a silicon nitride layer. Firstly, at about 400°C, hydrogen from an atomic source diffuses through much more readily than hydrogen from a molecular source. Secondly, at about 840°C, hydrogen from a molecular source is able to diffuse through a nitride. This diffusion is slowed in the case of a thicker nitride or a nitride that has been annealed at 1000°C. Hydrogen re-introduction through a nitride layer with a high temperature atomic source has not been attempted, but it is likely that this would be rapid.

The hydrogen loss model may provide a framework for understanding surface passivation with a silicon nitride capping layer. It is not, as yet, an analytic tool and therefore does not provide answers to questions such as:

- What is the exact profile of hydrogen in the nitride?

- What proportion of the molecular hydrogen reacts with the nitride? What proportion diffuses through to the oxide?

- If hydrogen is present in the nitride and oxide in both molecular and atomic forms, to what extent does it swap between the two? The results of experiments done with the hydrogen-containing plasmas (section 6.6) suggest that at least some of the atomic
hydrogen remains as atomic hydrogen (otherwise there would be no improvement in $J_{oc}$ at the low plasma treatment temperatures).

- What is the capture cross-section for different interface states and dangling bond configurations?

This chapter (and the two previous) present the results of a large number of wafer batches. Unless noted, the wafers shown in each figure were, as much as possible, processed together. Making comparisons between wafers shown in different figures is complex as it involves cross-batch comparisons. Even within a single batch there were unavoidable variations in emitter sheet resistance and in surface roughness. Both these factors were shown to be significant in this chapter. Cross-batch comparisons introduce larger variations in emitter sheet resistance, oxide thickness and in nitride thickness. Even when these attributes are equivalent, the thermal history of the wafers is important.

### 7.7 Conclusions

In this chapter the effect of oxide/nitride stacks on wafers that could be used for cell fabrication was investigated. In particular, the effects of varying emitter sheet resistance, of using p- and n-type wafers of varying resistivity and of textured wafers was determined.

Chemically polished wafers with a heavier phosphorous diffusion were found to be less sensitive to nitrogen anneals and therefore probably less sensitive to a loss of hydrogen from the silicon interface. For wafers with a 22nm thick oxide under 39nm thick nitride (a combination with relatively good anti-reflection properties), the optimum sheet resistance after nitrogen anneal was 60–200Ω/□ for all nitrogen anneal temperatures.

Experiments with different ‘type’ wafers did not show a clear influence of wafer resistivity on $J_{oc}$ values after nitride deposition, nitrogen anneal or forming gas anneal. Complete recovery of $J_{oc}$ for a high resistivity n-type wafer using a high temperature FGA was demonstrated. For an n-type, FZ 0.5–3Ωcm wafer, effective lifetimes improved considerably after nitride deposition, possibly due to passivation of the bulk by atomic hydrogen, and remained high after high temperature anneals in both nitrogen and forming gas.

In the case of textured wafers, nitride deposition was shown to improve $J_{oc}$ values for KOH textured wafers except in the case of the thinnest oxide (40nm). Recovery of a textured wafer with an oxide/nitride stack using a high temperature forming gas anneal was demonstrated for the oxide thicknesses of 75nm and greater, but not for wafers with a thin oxide (40nm). Experiments suggest that with a thinner oxide, $J_{oc}$ values are limited
by a lack of hydrogen, rather than by any permanent damage to the wafer bulk. Further work needs to be done to determine why this was the case.
Conclusions and Suggestions for Further Work

This thesis discussed thin-film silicon layers and oxide/LPCVD nitride stacks on silicon. Thin-film silicon layers were fabricated using the epilift technique and various aspects of layer growth were studied. The effects of nitride deposition and subsequent high temperature treatments on silicon wafers were investigated. A hydrogen-loss model was developed to explain the behaviour of wafers with an oxide/nitride stack under high temperatures. This model was used in the investigation of the recovery of surface passivation for the wafers after anneals in a high temperature nitrogen ambient.

8.1 Liquid Phase Epitaxy for the Epilift Technique

The epilift technique is a method for producing thin layers of silicon that can be processed into solar cells. It uses liquid phase epitaxy and a reusable, patterned substrate. Work in this area concentrated on layer growth.

The morphology resulting from different seeding patterns was discussed. Seeding line width and cooling rate were varied using square grids and grids with lines angled at 60° relative to each other. A method of dislocation generation was proposed but found not to be suitable as a means for introducing dislocations to the epitaxial layer. Effective lifetimes on n-type material grown using barrier layers of both oxide and carbonised photoresist were measured. The lifetimes were found to be more than adequate for the the production of good solar cells. A significant difference between the layers grown using carbonised photoresist and oxide as masking layers could not be discerned.

The incorporation of boron into silicon layers grown using liquid phase epitaxy and a tin melt was studied. Boron incorporation was shown to be a function of both time and temperature. The segregation coefficient for boron from liquid tin into solid silicon was inferred to be temperature dependent and to decrease with decreasing temperature. Boron incorporation decreased with time, probably due to the formation of either boron
precipitates that remained in the tin melt or volatile boron hydrides that were removed from the system. Boron incorporated into the epitaxial layer was determined to be spatially uniform and electrically active. By choosing appropriate growing conditions, an abrupt and heavily doped p-type region was formed at the substrate/epitaxial layer interface. This could be useful as a back surface field for epilift solar cells.

Work on this project continues and is commercial-in-confidence. For this reason, suggestions for further work are not discussed here.

8.2 Oxide/LPCVD Nitride Stacks on Silicon

8.2.1 Conclusions

A nitride deposited in the early stages of cell fabrication allows the possibility of increased processing flexibility and the realisation of novel cell structures due to many properties of the silicon nitride. The nitride can also behave as an effective anti-reflection coating and the anti-reflection properties of an oxide/nitride stack were determined theoretically as a function of oxide and nitride thickness.

Low pressure chemical vapour deposition (LPCVD) was chosen as the deposition method because it is a mature, reliable technique that is well suited to batch-mode applications. Using high resistivity, float-zone grown wafers and a light phosphorous diffusion, deposition of an LPCVD nitride over an oxide was found to have no significant influence on effective lifetimes for a range of oxide and nitride thicknesses.

A potentially large disadvantage of a nitride layer deposited on an oxide-coated silicon wafer in the early stages of cell fabrication is that when heated in an inert gas ambient, there was a substantial drop in effective lifetimes. For the high resistivity, float zone wafers used for this work, and with an intermediate oxide layer, this was shown to be due to a loss of surface passivation at the silicon/oxide interface, rather than to any irreversible damage to the wafer bulk. Without an oxide, heating a wafer with a deposited nitride resulted in a drop in effective lifetimes that was not recovered by stripping the nitride and re-passivating the surface. This drop in effective lifetimes was probably a result of stress damage to the bulk due to the mismatch in coefficients of linear thermal expansion for silicon and silicon nitride.

Studies were done on the effect of high temperature anneals in nitrogen on the passivation at the silicon/oxide interface, which was characterised by $J_{oc}$. Oxide thickness, nitride thickness, nitrogen anneal temperature and nitrogen anneal time were all varied. A hydrogen loss model was developed to explain the observations. The essence of this model is that when a wafer with an oxide/nitride stack was subjected to higher temperatures in
an inert gas ambient, there was a loss of hydrogen from the system.

Hydrogen re-introduction through an oxide/nitride stack was attempted using anneals, wet oxidations, plasma sources, second LPCVD nitride depositions and high temperature forming gas anneals. The most important parameters in determining the success of $J_{oc}$ recovery were found to be thickness of the nitride layer and the thermal history of the wafer. Complete recovery of $J_{oc}$ was demonstrated using high temperature forming gas anneals and partial recovery was demonstrated with the other methods in some cases.

A hydrogen plasma (co-incident with PECVD nitride deposition) was beneficial in $J_{oc}$ recovery irrespective of nitrogen anneal temperature. This was only done with a maximum LPCVD nitride thickness of 24nm. With a weaker plasma (and without PECVD nitride deposition) and oxide/nitride thicknesses of 25/35nm, no improvement in $J_{oc}$ was seen for wafers after a 1000$^\circ$C nitrogen anneal, but almost complete $J_{oc}$ recovery was seen after a 900$^\circ$C nitrogen anneal. This method shows promise and should be investigated further, with a dedicated hydrogen plasma source.

The fact that surface passivation quality substantially recovered at 400$^\circ$C in a plasma ambient, whereas there was negligible change in a 400$^\circ$C forming gas ambient indicates that, at 400$^\circ$C, atomic hydrogen was far more mobile in the nitride than molecular hydrogen.

With a high temperature forming gas anneal, the time and temperature needed to recover $J_{oc}$ values were found to be dependent on the thickness of the nitride and on the thermal history of the wafer. Wafers with a thicker nitride or that underwent higher temperature nitrogen anneals required a longer forming gas anneal to effect full recovery of $J_{oc}$. As the forming gas anneal temperature was increased, hydrogen removal from the silicon/oxide interface became increasingly significant.

Finally, the effect of oxide/nitride stacks on wafers that could be used for cell fabrication was investigated. In particular, the effects of varying sheet resistance, on p- and n-type wafers of varying resistivity and on textured wafers was determined.

Wafers with a heavier phosphorous diffusion were found to be less sensitive to nitrogen anneals and therefore inferred to be less sensitive to a loss of hydrogen from the silicon interface. From experiments with different ‘type’ wafers, no influence of wafer resistivity or type on the response of a wafer with oxide/nitride stack to nitride deposition, nitrogen anneal or high temperature FGA could be concluded. Complete recovery of $J_{oc}$ for a high resistivity n-type wafer using a high temperature FGA was demonstrated. In the case of an n-type, FZ 0.5–3Ωcm wafer, considerable improvement in effective lifetimes were seen after silicon nitride deposition. This improvement persisted even after various high temperature treatments and was postulated to be due to passivation of the bulk by atomic
hydrogen.

In the case of textured wafers, nitride deposition was shown to improve $J_{oc}$ values for KOH textured wafers, except in the case of thin oxides. For a textured wafer with a 40nm thick oxide and a 65nm thick nitride (a reasonable ARC), $J_{oc}$ values were not recovered with an 840°C FGA. This was shown to be due to a lack of passivation at the silicon/oxide interface. Other methods of hydrogen re-introduction or forming gas anneals at lower temperatures should be used for thin oxides and thick nitrides on textured wafers.

8.2.2 Further Work

Series interconnected cells are a novel cell design that could potentially benefit from a nitride layer deposited in the early stages of cell fabrication. If both metal contacts are placed on the rear to avoid shading losses, then shunting and pinhole formation can become a concern. These problems may be reduced with the use of an oxide/nitride stack. A series interconnected cell design is likely to involve all three of the considerations discussed in chapter 7.

To obtain reasonable light trapping and anti-reflection properties while maintaining good surface passivation, it is desirable to have a thin oxide under a thicker nitride. The minimum oxide thickness used in this work was 25nm, but better reflection control and excellent surface passivation can be achieved with thinner oxides. It would therefore be useful to study oxide thicknesses in the range 0-25nm. In line with this work the supposed interface states introduced when an oxide/nitride stack with a thin oxide is heated, should be investigated in more detail. Can the interface states be ‘annealed out’ in a high temperature nitrogen ambient? Since the states were introduced with high temperatures, the temperature may need to be kept below some maximum. The cooling rate will probably be significant.

Experiments with a thinner oxide on a textured surface did not realise the re-passivation of the silicon/oxide interface. This structure is highly desirable for light trapping and anti-reflection control and therefore it would be useful to test other methods of hydrogen re-introduction. Using a forming gas anneal, more success may be achieved with a lower temperature anneal (for an extended period of time) or an ambient with a higher hydrogen content. This could be combined with a study on high quality, high resistivity, (111) orientated FZ wafers. In particular the temperature dependence of the removal of hydrogen from and re-introduction of hydrogen to the (111) orientated silicon/oxide interface should be studied in more detail.

$J_{oc}$ recovery times were very long for some of the wafers used in this work and these may be reduced with the use of an ambient with a higher hydrogen concentration. Experiments
could be done to determine recovery time as a function of hydrogen concentration for various oxide/nitride thicknesses, for polished and textured wafers and for (100) versus (111) orientated surfaces.

The introduction of atomic hydrogen through the use of a hydrogen-containing plasma showed promise, but was limited by the relatively weak plasma that was available. Further work needs to be done to determine the potential of this process. In particular the effects of hydrogen concentration in the plasma and the temperature could be studied.

Throughout this thesis, the cooling rate was rapid and the results suggested that the cooling rate after a nitrogen or forming gas anneal could be significant. In particular, with a forming gas ambient, at higher temperatures the rate of hydrogen de-trapping from the silicon/oxide interface becomes more significant and the cooling rate is likely to strongly influence this. It is possible that faster \( J_{\infty} \) recovery could be achieved by doing a relatively short forming gas anneal at a high temperature, followed by a longer ‘cooling-down’ period.

The hydrogen loss model has been tested using hydrogen levels inferred through measurements of \( J_{\infty} \), which is probably very sensitive to the hydrogen quantity at the silicon/oxide interface. It would be interesting to combine these measurements with some more direct measurements of atomic hydrogen concentration levels in the oxide and the nitride. Techniques such as nuclear reaction analysis could be appropriate.

It was discovered that the nitride acts as an effective barrier to molecular hydrogen at low temperatures and, since hydrogen is known to diffuse readily in silicon, this characteristic could perhaps be used to determine further information about the diffusion of hydrogen in silicon. A possible experiment is the following. Using high resistivity, float zone wafers etched to various thicknesses, perform a light phosphorous diffusion and oxidation. Then deposit nitride on both sides, heat the wafers in a nitrogen ambient for sufficient time to ensure most of the hydrogen is removed from the silicon/oxide interface. Next, remove the nitride from one side only and place the wafers in a low temperature forming gas ambient and monitor \( J_{\infty} \) values. A plot of silicon thickness against the time taken to recover \( J_{\infty} \) values should reveal some information about hydrogen diffusion in silicon. There are many complications associated with this suggestion. A good \( J_{\infty} \) value indicates that hydrogen is bound to the silicon dangling bonds, in which case the measurement will probably combine atomic hydrogen diffusion, molecular hydrogen diffusion, the dissociation rate of molecular hydrogen and the reaction rate of hydrogen ions with silicon dangling bonds at the silicon/oxide interface.

Information about the diffusion rate of hydrogen in silicon could also be inferred using the 0.5–3\( \Omega \)cm, n-type material shown in figure 7.12. This material showed a marked increase in effective lifetimes after the silicon nitride deposition and it was suggested that
this was due to passivation of bulk defects as a result of the in-diffusion of atomic hydrogen. It would be interesting firstly to determine if an increase in effective lifetimes also occurs with a molecular hydrogen source and secondly to determine the rate of improvement with either molecular or atomic sources as a function of temperature.

The results discussed in chapter 6 suggested that either hydrogen or impurities in the forming gas caused a drop in effective lifetimes. This situation remained somewhat ambiguous, but could be clarified by using an ultra-pure hydrogen source. If hydrogen is able to cause damage, then this may be reduced by using a lower cooling rate, giving the hydrogen time to leave the silicon.
Appendix A

List of Publications

Publications arising from the work in this thesis:

Journal Papers


Book Chapter

K.J. Weber, M. Stocks, A.W. Blakers and M. McCann Transfer of mono-crystalline Si films for thin film solar cells (chapter in *Growth, characterisation and electronic application of amorphous and crystalline Si thin films* To be published.

Conference Talks


**Conference Papers**


**Related Publications**

Bibliography


[87] Professor Paul K. Chu. Course notes, AP4120, Microelectronic materials and processing. City University of Hong Kong.


[150] Naoko Hiroshimaya, Kou Sato, Yoshimasa Haraguchi, Takeshih Matsushita, Akiko Nagasawa, and Hiroshi Tayanaka. 10cm×10cm single-crystalline silicon thin-film


Page 3, line 14: “The electron and hole are to in about the cell” should read: “The electron and hole are free to move about in the cell”.

Page 5, equation 1.4: the symbol t should be replaced with the symbol T.

Page 12, line 20: “dilatant” should be replaced with “dilutant”.

Page 16, lines 3 – 4: The sentence: “Most other groups are still working on layer deposition.” should be removed.

Page 19, line 21: “Debye Institute” should read “Debye Institute”.

Page 54, line 8: “resutled” should read “resulted”.

Page 69, lines 16 – 18: The sentence: “Back junction cells also have a potential advantage in that the emitter does not need to be optically transparent and so can be thicker in order to reduce series resistance losses.” should be replaced with: “Back junction cells also have a potential advantage in that the emitter does not need to be optically transparent and so can be optimised to minimise contact losses.”.

Page 82, line 24: “diffuse light well” should read “scatter light well”.


Page 97, the sentence beginning on the second last line should read “For example; ‘carbonised’ photoresist (formed by annealing in a forming gas ambient at 1000ºC for 30 minutes) was found, in earlier experiments by the author, to be a suitable masking material that, under appropriate conditions, has very weak adhesion to the epitaxial layer.

Page 104, equation 3.2: the F in the first line should be HF, ie the equation should read; 
\[ \text{Si} + 2\text{HF} + 2\text{h}^+ \rightarrow \text{SiF}_2 + 2\text{H}^+ \]

As stated in the text, this is only one possible reaction pathway; others are mentioned in the literature. As an example of this point, SiF₂ is a very unstable molecule with a short half-life\(^1\) and there are therefore a number of different ways in which it can react.

Page 105, The last paragraph of section 3.4.1 should read:
“Lifetime measurements were made on detached epilayers using the microwave photoconduction decay (MWPCD) technique. One of the wafers grown using the carbonised photoresist layer was detached in three separate pieces, thereby enabling the lifetime to be measured in different areas of the epitaxial layer. The MWPCD technique uses a measurement of the reflection of incident microwave radiation to determine the effective minority carrier lifetime. For measurement, a silicon sample is illuminated with a pulse of laser light, thereby exciting carriers to the conduction band. Microwaves are then concentrated onto the sample and the mobile electrons in the conduction band act as a mirror for these microwaves. For small changes in conductivity, the amplitude of the reflected microwave signal is proportional to the excess carrier concentration in the sample. The decay in the amplitude of the reflected microwave signal can therefore be used to determine the minority carrier lifetime.”

Page 117, equation 4.1 should read: 
\[ 3\text{SiH}_2\text{Cl}_2(g) + 4\text{NH}_3(g) \rightarrow \text{Si}_3\text{N}_4(s) + 3\text{Cl}_2(g) + 9\text{H}_2(g) \]

Page 127, line 5: The sentence: “Each of these terms has a bulk and surface component.” should be removed.

Page 127, line 5: “which has a decay time of 2.3ms” should be replaced by “which has a decay time of about 20µs in the transient mode and about 2.3ms in the QSS mode”.