Formation and Characterization of Aluminium Contacts to n-type Silicon

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Declaration

This thesis is an account of research undertaken between February 2004 and October 2004 at the Centre for Sustainable Energy Systems, The Australian National University, Canberra, Australia.

Except where acknowledged in the customary manner, the material presented in this thesis is, to the best of my knowledge, original and has not been submitted in whole or part for a degree in any university.

David P. Weinholz

October, 2004

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Abstract

Samples were prepared by performing phosphorus diffusions with $POCl_3$ on Sb doped (100) silicon wafers. 99.9% (3N) purity Al or 99.999% (5N) purity Al dots of diameter 0.7 mm and thickness between 0.2 μm or 1.0 μm were then deposited onto quarters of these wafers. The quarters were then subsequently cleaved into 1 cm^2 pieces which were annealed at temperatures ranging from 400°C to 650°C for durations of time between 10 minutes and 2 hours. The speed with which these samples were cooled was also varied. After annealing, 3N Al or 5N Al was then deposited on the rear of the samples to a thickness of 1 μm to ensure a low resistance ohmic contact was formed on the rear.

Characterisation of these contacts was carried out by measuring the IV characteristics of the contacts and by removing the Al from the front and making observations of the surface topology under an optical microscope and/or by utilizing a scanning electron microscope (SEM). Also, secondary ion mass spectrometry (SIMS) was used to check the diffusion profile of Al, P, and the concentration of Sb dopant in the wafers.

Results showed that samples which had 0.3 μm Al deposited in dots on the front, when sintered at temperatures over the eutectic temperature, exhibited rectifying properties evidenced by IV curves characteristic of diodes with turn on voltages of 0.6 mV. The corresponding samples with 1.0 μm appeared to have similar IV curves. However, the turn on voltage was about 0.5 mV. On inspection of the interface, the 0.3 μm Al deposited samples appeared to have formed large, well rounded holes in the silicon and the 1.0 μm Al deposited samples showed localized spiking and no large, well rounded holes.

The samples that were sintered at less than the eutectic temperature, showed very poor rectifying contact properties in their IV curves and their interfaces varied from minimal pitting at lower temperatures to large degrees of pitting at higher temperatures.

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Introduction

1.1 Conventional Photovoltaic Cells

As can be seen in Figure 1.1, photovoltaic cells are two terminal devices having contacts to both the n and p-type region. On the front, n-type region, there is usually a metal grid contact and on the rear a blanket layer of metal is used to form the contact to the p-type substrate. By arranging the contacts as such, it can be ensured that they are not made near the boundary of the two regions and thus the risk of causing a shunt, metal overlapping both regions, is quite small. The n-type region is created by diffusing an n-type dopant, usually phosphorus, into the base p-type (usually boron doped) substrate. This produces an n^+ region near the metal contacts and likewise a p^+ region is produced on the rear of the cell by diffusing a p-type dopant (usually boron) into these areas.

As illustrated by the equivalent circuit of a photovoltaic cell in Figure 1.2, a photovoltaic cell is essentially a diode in parallel with a constant current source with finite series and shunt resistances. Diodes are characterised by their reverse saturation currents, I_0. This is the current flowing though the diode when it is under reverse bias voltage.

The constant current generator, I_L, represents the current produced due to the electron/hole formation in the silicon cell when the cell is illuminated. The internal series resistance, R_s, represents the resistance in the metal fingers, the resistance of the semiconductor and the resistance at the metal/semiconductor contact while the shunt resistance, R_{sh}, represents the resistance of alternative paths for the current such as through metal that is overlapping the p and n-type regions. R_L represents the resistance of the load that is to utilise the current, I, and voltage, V, produced.

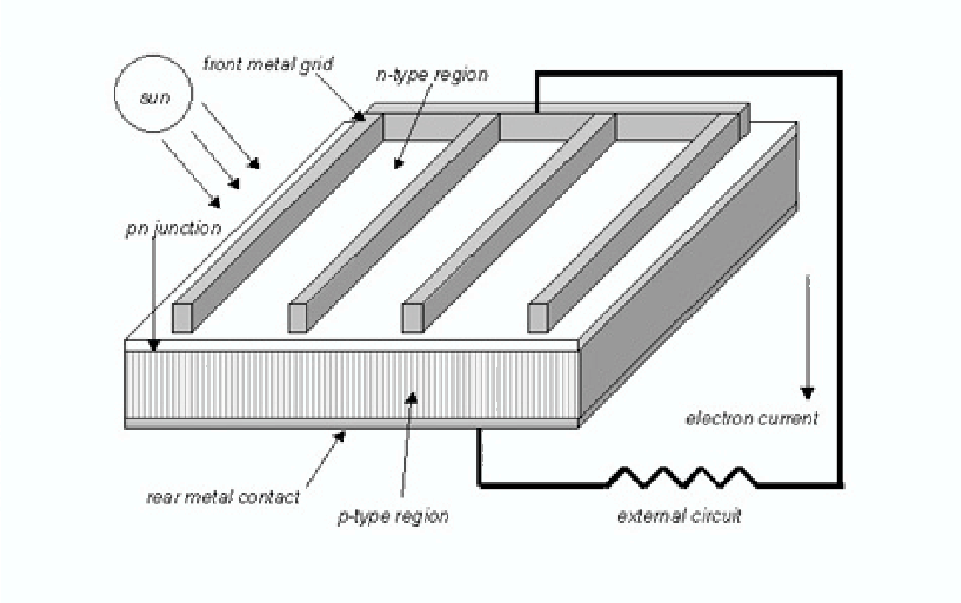


Figure 1.1: Conventional photovoltaic (PV) cell

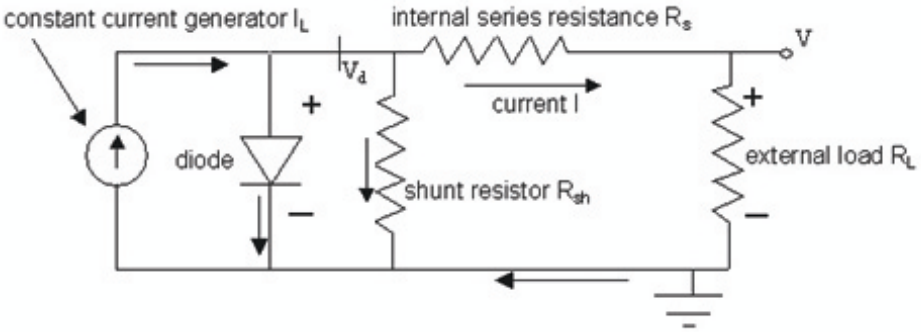


Figure 1.2: Equivalent solar cell

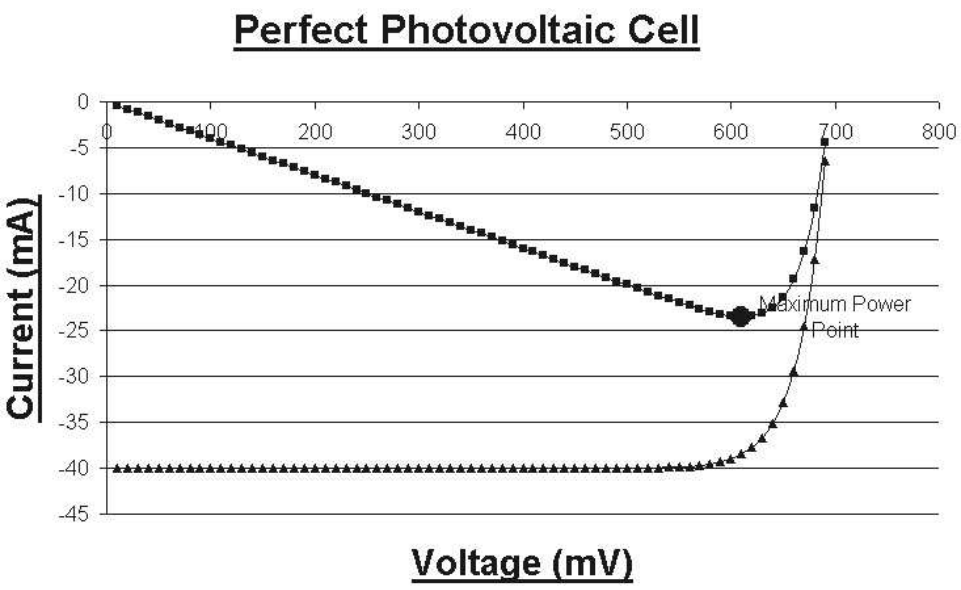


Figure 1.3: IV and power curves of a PV cell that has infinite shunt resistance and zero series resistance. Power is in units of mW.

The current generated by a PV cell can be written in terms of the series and shunt resistances as shown in Equation 1.1 [1].

$$I = I_0[exp(\frac{q(V - IR_S)}{kT}) - 1] + (\frac{V - IR_S}{R_{SH}}) - I_{sc} \tag{1.1}$$

Figure 1.3 shows two curves: the I-V curve of a solar cell (lower curve) and the power curve produced by the cell (upper curve) where power is displayed in units of mW. The maximum power point is shown near the 'knee' of the IV curve at 610 mV. This is the point where the product of the current and the voltage is the largest. Figure 1.3 was based on a theoretical cell which had the following characteristics: $R_{sh} = \infty\Omega$, $R_s = 0\Omega$, $A = 1\text{cm}^2$, I_{sc} = -40 mA and V_{oc} = 695 mV.

One means of measuring the quality of a solar cell is through its fill factor (FF). This is given in Equation 1.2.

$$FF = \frac{V_{mp} \times I_{mp}}{V_{oc} \times I_{sc}} \tag{1.2}$$

V_{mp} and I_{mp} represent the voltage and current, respectively, at which maximum power is

output. V_{oc} represents the open circuit voltage and I_{sc} represents the short circuit current. Fill factors of 70-80% are quite common for solar cells with V_{mp} and I_{mp} usually 85-90% of V_{oc} and I_{sc} respectively. Therefore, under the conditions used for Figure 1.3, the cell would have a fill factor of (-23.5 mA x 610 mV) / (695 mV x -40 mA) = 84.48%. The efficiency of a cell is defined in Equation 1.3.

$$efficiency = \frac{output\ power}{input\ sunpower} = \frac{V_{mp} \times I_{mp}}{input\ sunpower} \tag{1.3}$$

Thus the efficiency of a PV cell is directly related to its maximum power as would be expected. In typical commercial PV cells the open circuit voltages are between 500 mV and 650 mV and the short circuit currents between 30 mA and 40 mA yielding efficiencies of 15% to 20%.

In Figure 1.4 the same values of I_{sc}, V_{oc}, A, R_{sh} and R_s were assumed as in the case of the 'perfect' PV cell. However, for the cases of low shunt resistance and high series resistance, different values of R_{sh} and R_s were assumed. These were $R_{sh} = 100\ \Omega$ and $R_s = 0\ \Omega$ for the case of low shunt resistance and $R_{sh} = 10^{10}\ \Omega$ and $R_s = 10\ \Omega$ for the case of high series resistance. As can be seen from Figure 1.4, if the shunt resistance becomes smaller or the series resistance becomes too large, the maximum power of the PV cell will be reduced. Thus to maintain a high efficiency, which is directly related to the maximum power of a PV cell via its fill factor, high shunt resistances and low series resistances must be maintained. It can also be seen from Figure 1.4 that the short circuit current and open circuit voltage are relatively unaffected by these changes in series and shunt resistances.

1.2 Sliver Cells

There are alternative structures for the structure and positioning of contact to PV cells to that in Figure 1.1. Some of these have the contacts to p-type and n-type materials close to each other. This results in an increased risk of shunting currents across these areas. One particular type of cell that is susceptible to this problem is the sliver cell illustrated in Figures 1.5 and 1.6.

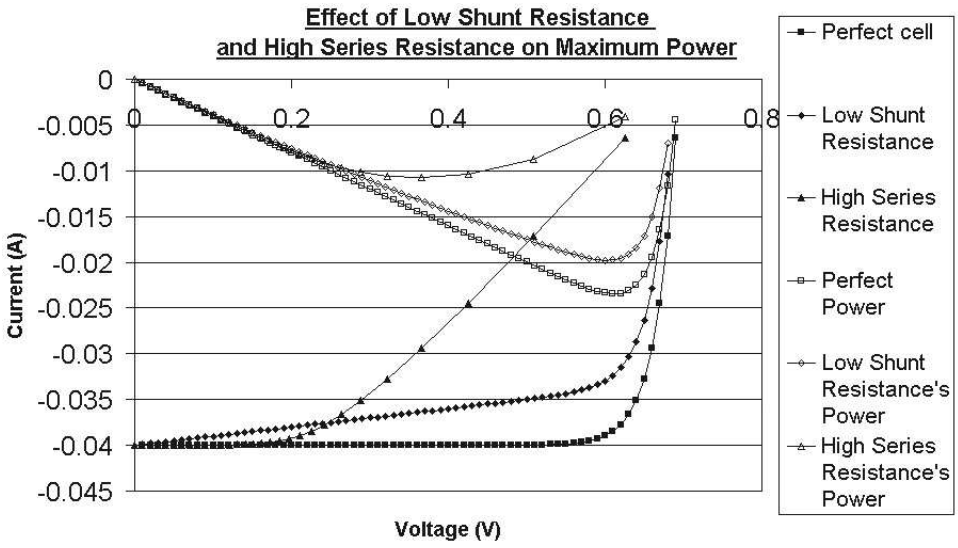


Figure 1.4: A comparison of the effect that decreasing shunt resistance or increasing series resistance has on the power output of a PV cell. Power is in units of mW.

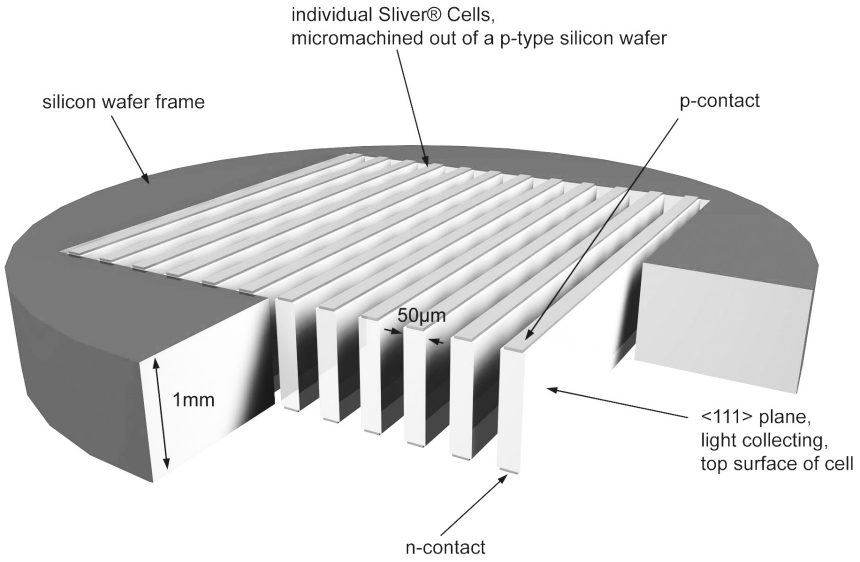


Figure 1.5: Sliver cell

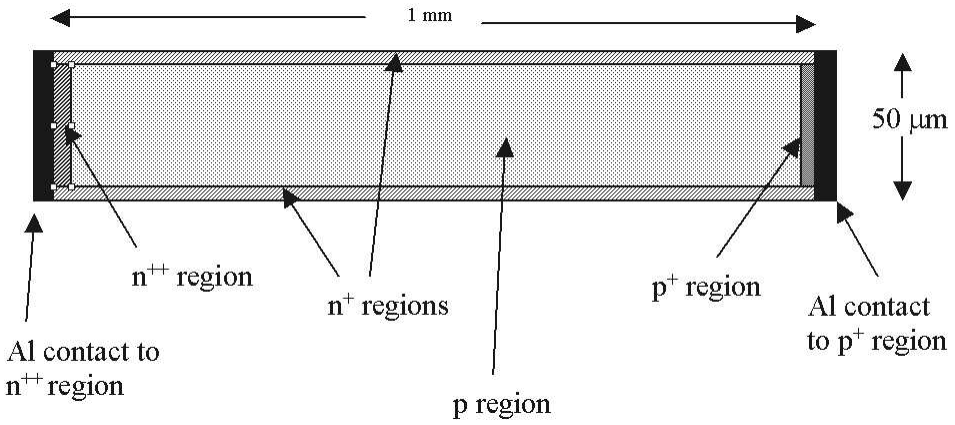


Figure 1.6: Contact to a sliver cell

Sliver cells are a type of PV cell which utilizes much less silicon for a comparable output of electrical energy as standard monocrystalline solar cells. Figure 1.5 shows the dimensions of a sliver with respect to the wafer from which the slivers are produced and Figure 1.6 shows the position of the contacts to the sliver. From this it can be seen that one of the difficulties of sliver cells is the formation of contacts to the p^+ type region, as this region is quite small and is at all places close to the neighbouring n^+ regions. From this it can be seen that there is an increased risk of smaller values for shunt resistance.

One approach to address this problem would be to search for a metal and corresponding process that result in good contact to p^+-type and poor contact to n^+-type substrate. This could be done by choosing an appropriate metal together with manipulation of the surface concentrations of the p-type and n-type dopants.

Of the metals which are available to make contacts, aluminium, which has a relatively low eutectic temperature (temperature at which a combination of two elements is first molten) with silicon (577 °C), a high silicon solubility of about 13% at 600 °C and is a p-type dopant, appears to be an ideal candidate for making low resistance ohmic contact to p-type silicon. This is indeed the case and it is widely used in IC manufacturing in contact formation. It is anticipated that, since Al is a p-type dopant, it will be possible to produce a thick p-type epitaxial layer of silicon on the n-type silicon substrate in the areas bordering the p-type substrate, thus resulting in a p-n junction, with corresponding rectifying properties, to these n-type regions.

As as a result, a rectifying contact to n-type silicon should be produced while under the same conditions forming a low resistance ohmic contact to p-type silicon. Thus, if the placement of the contact is slightly misaligned so that it overlapped both regions, the cell will not be adversely affected to a large degree and the manufacture of the cell will become simpler and result in the production of cells being more reliable.

In an attempt to produce contacts that were similar in their current and voltage characteristics to a diode, samples were prepared by performing phosphorus diffusions, using $POCl_3$ as the source of phosphorus, on Sb doped silicon wafers. 3N Al or 5N Al (99.9% Al or 99.999% Al) dots of diameter 0.7 mm and thickness of between 0.2 μm and 1.0 μm were then deposited onto quarters of these wafers. The quarters were then subsequently cleaved into 1 cm^2 pieces that were annealed at temperatures ranging from 400 °C to 650 °C for durations of time between 10 minutes and 2 hours. The speed with which the samples were cooled was also varied between 1 minute to about 30 minutes. After annealing, 3N Al or 5N Al was then deposited on the back of the samples to a thickness of approximately 1 μm to ensure a low resistivity, ohmic rear contact was formed.

Characterization of these contacts was carried out by measuring the IV characteristics of the contacts, via the two terminal-method explained in the following chapter. Characterization was also carried out by removing the Al from the front, polished side of the wafer and making observations of the surface topography under an optical microscope and a scanning electron microscope (SEM). Also, secondary ion mass spectrometry (SIMS) was used to gain the diffusion profile of Al, P, and a measure of the concentration of Sb dopant in the wafers.

The structure of this thesis is outlined as follows:

Chapter 2:*Literature Review & Theoretical Background*
A study of similarities and differences with related research and how this research will contribute new knowledge. Specifically the formation of contacts to p-type and n-type

material was researched. Fermi levels, work gaps, energy bands, epitaxial regrowth, Al spiking and eutectic phase diagrams are also discussed in detail.

Chapter 4:*Formation and Characterization Techniques*

The workings of the instrumentation used in the formation of the contacts and characterization techniques examined. These included various modes of SEM, SIMS, surface profiling and measurements of electrical properties.

Chapter 5:*Experimental Procedure*

The process by which samples were made and the characterization techniques used are explained explicitly.

Chapter 6:*Results and Discussion*

Experimental data is given and analyzed. A brief summary of the findings is then given and possibilities for future research presented.

Literature Review

2.1 Background

As detailed in the Intoduction, the fill factor (FF) of a cell is a key characteristic of the cell and a high FF is vitally important for high cell efficiencies. Significant series resistance and low shunt resistances reduce the FF, while leaving other parameters that determine photovoltaic cell efficiencies, such as V_{OC} and I_{SC}, relatively unchanged.

In Figure 2.1 it was assumed that V_{oc} was 0.7 V and I_{sc} was 4.00 x 10^{-2} A over an area of 1 cm^2. Points above the line represent values for $FF < 80\%$ and points below the line represent values of $FF > 80\%$. Thus it can be seen from Figure 2.1 that the minimum shunt resistances allowed is about 350 Ω. It can also be seen that the maximum allowable series resistances is 0.72 Ω such that the fill factor will remain at or above 80%.

It should be noted that the shunt and series resistances referred to in Figure 2.1 are those

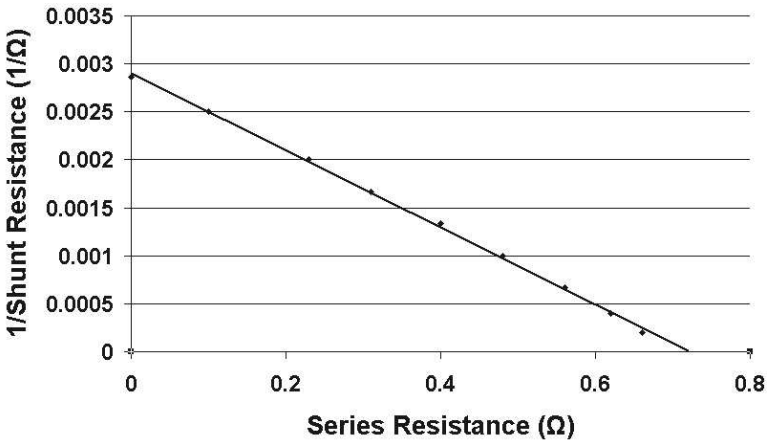


Figure 2.1: Plot of combinations of shunt and series resistances which result in fill factors of 80%

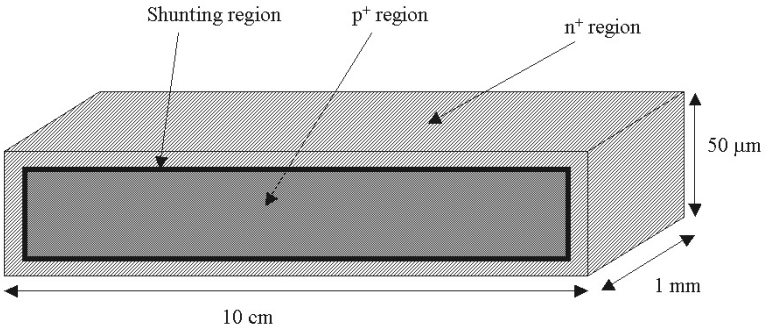


Figure 2.2: Diagram illustrating the possibility of shunting in sliver cells.

near the maximum power point, at which the cell would be operating, such that a fill factor of 80% could be maintained. In standard PV cells this is usually an operating voltage of between 0.5 V and 0.6 V.

Now the shunt resistance is related to the specific contact resistance, R_c, of the contact to the n-type material by Equation 2.1:

$$R_{sh} = R_c/A \tag{2.1}$$

where A is the area of contact to n-type material and the series resistance is related to the specific contact resistance, R_c, of the contact to the p-type material by Equation 2.2:

$$R_s = R_c/A \tag{2.2}$$

where A is the area of the contact to p-type material. This, however, is only the case if factors, other than the specific contact resistance, that contribute to the series resistance are negligible.

Figure 2.2 illustrates where shunting might occur by the thick solid line surrounding the p^+ region. The sliver cell's dimensions are about 10 cm by 1 mm by 50 μm. The contact to the p-type material is 10 cm by 50 μm and the contact to n-type material, due to misalignment, may be 10 cm by 1 μm on either side. This would result in the specific contact resistance for contact formed to n-type material needing to be greater than 10 cm x 2 x 0.0001 cm x 350 Ω = 0.7 Ω-cm^2 and that to p-type material less than

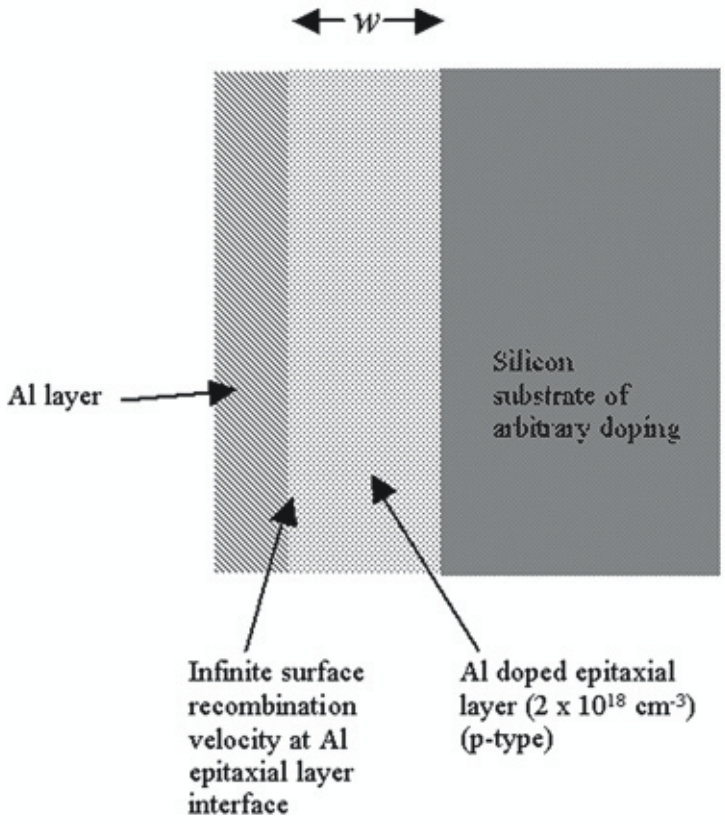


Figure 2.3: Diagram showing Al layer, epitaxial layer and Si substrate.

10 cm x 0.005 cm x 0.72 Ω = 0.0036 Ω-cm^2.

2.1.1 Estimating Dark Saturation Current Density (J_0)

Dark saturation current density is the current density through a surface when a reverse bias voltage is applied. Given a surface shown in Figure 2.3, then the J_0 contribution from this surface can be calculated as follows:

Assuming that:

- there is a negligible rate of recombination of electron/hole pairs in the epitaxial layer,
- there is a very high surface recombination velocity of about 10^7 cm s^{-1},
- and that there is negligible recombination at the epitaxial layer (epilayer)-substrate interface.

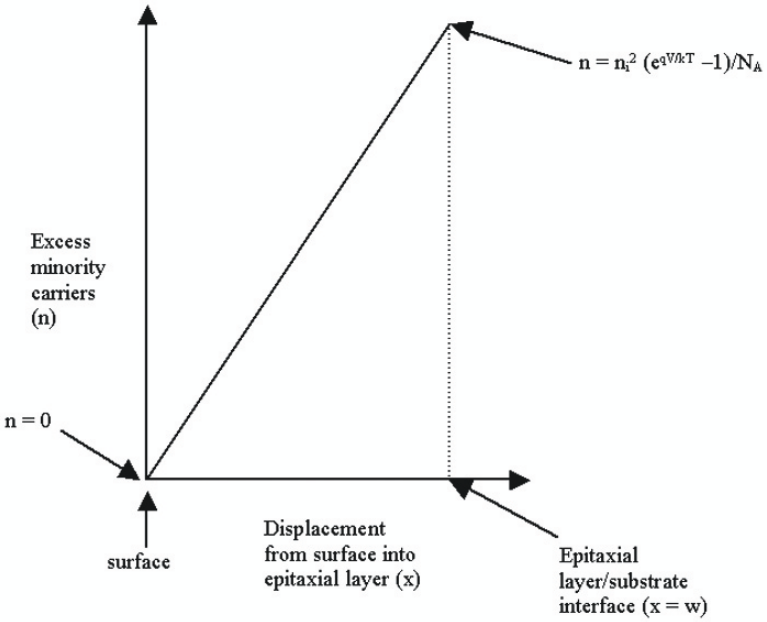


Figure 2.4: Diagram showing excess minority carrier profile in the epitaxial layer.

the excess minority carrier profile in the epitaxial layer is shown to be as in Figure 2.4 where the minority carrier concentration at the point on the right-hand side of the figure is given by Equation 2.3.

$$n = \frac{n_i^2}{N_A}(exp(\frac{qV}{kT}) - 1) \tag{2.3}$$

where n_i is the intrinsic carrier density of the doped silicon, N_A (assumed to be 2 x 10^{18} atoms cm^{-3}) is the epilayer doping level, q is the electronic charge of an electron, V is the applied voltage, k is Boltzmann's constant and T is the temperature.

Now if current flow is due in whole to diffusion then:

$$J = qD_n\frac{dn}{dx} \tag{2.4}$$

where D_n is the electron diffusivity in the epilayer (7.1 cm^2/s).

J_0 can then be calculated from the slope of the curve to give:

$$J_0 = \frac{qD_n n_i^2}{N_A w} \tag{2.5}$$

where w is the epilayer thickness.

For the calculation of n_i, bandgap narrowing must be taken into account. In intrinsic silicon at room temperature, $n_i^2 \approx 10^{20}$. For heavily doped p-type silicon, however:

$$n_i^2 = 10^{20} e^{\Delta E_c / kT} \tag{2.6}$$

where ΔE_c is the amount of bandgap narrowing.

An equation that provides a good fit to experimental data is given in Equation 2.7 [3].

$$\Delta E_c = 14 \times 10^{-3} Ln(\frac{N_A}{1.4 \times 10^{17}}) eV \tag{2.7}$$

Thus, if the doping level is $N_A = 2$ x 10^{18} dopant atoms cm^{-3} and T is room temperature (298.15 K), $n_i^2 = 4.2 \times 10^{20}$ cm^{-6} for heavily doped p-type silicon.

Using this result:

$$J_0 = \frac{1.5 \times 10^{-19} \times 7.1 \times 4.2 \times 10^{20}}{2 \times 10^{18} w} \tag{2.8}$$

$$J_0 = \frac{2.4 \times 10^{-16}}{w} A cm^{-2} \tag{2.9}$$

where w is in centimetres.

Thus if w = 0.1 μm then $J_0 = 2.4$ x $10^{-11} A cm^{-2}$.

Now if the voltage across the sample is 0.6 V and the resistance is 0.7 Ω across an area of 1 cm^2:

$$R = \frac{V}{I} = \frac{V}{J_0 \times (e^{(qV/kT)} - 1)} \tag{2.10}$$

$$0.7 = \frac{0.6}{\frac{2.4\times10^{-16}}{w} \times (e^{38.5\times0.6} - 1)} \tag{2.11}$$

Thus the epilayer thickness should be 0.3 μm.

and the dark current density would be:

$$J_0 = \frac{2.4 \times 10^{-16}}{w} = 8.0 \times 10^{-12} Acm^{-2} \tag{2.12}$$

2.2 Metal Contacts

Figure 2.5 [18] illustrates the concept of the Schottky model: the top diagrams represent the energy bands before contact and the ones below represent the energy bands after contact. E_f is the Fermi level, χ is the electron affinity of the semiconductor, ϕ_s is the semiconductor work function, ϕ_m is the metal work function, ϕ_B is the barrier height after contact, E_c is the conduction band, and E_v is the vacuum band. In (a), (b) and (c) of Figure 2.5 $\phi_s > \phi_m$, $\phi_s = \phi_m$ and $\phi_s < \phi_m$ respectively. The barrier height is given by $\phi_B = \phi_m - \chi$.

χ is defined as the potential difference between the bottom of the conduction band and the vacuum level. In the Schottky theory the barrier height depends only on the metal work function and on the semiconductor electron affinity. Thus choosing a metal with the correct work function or a semiconductor with the correct electron affinity can change the barrier height. In practice, however, the barrier height remains relatively constant even with a changing work function of different metals. This constancy of the barrier height is due to a phenomenon known as Fermi level pinning.

The barrier height is largely independent of the doping concentration, but the barrier width does depend on the doping concentration. The space-charge region (scr) width, w, is

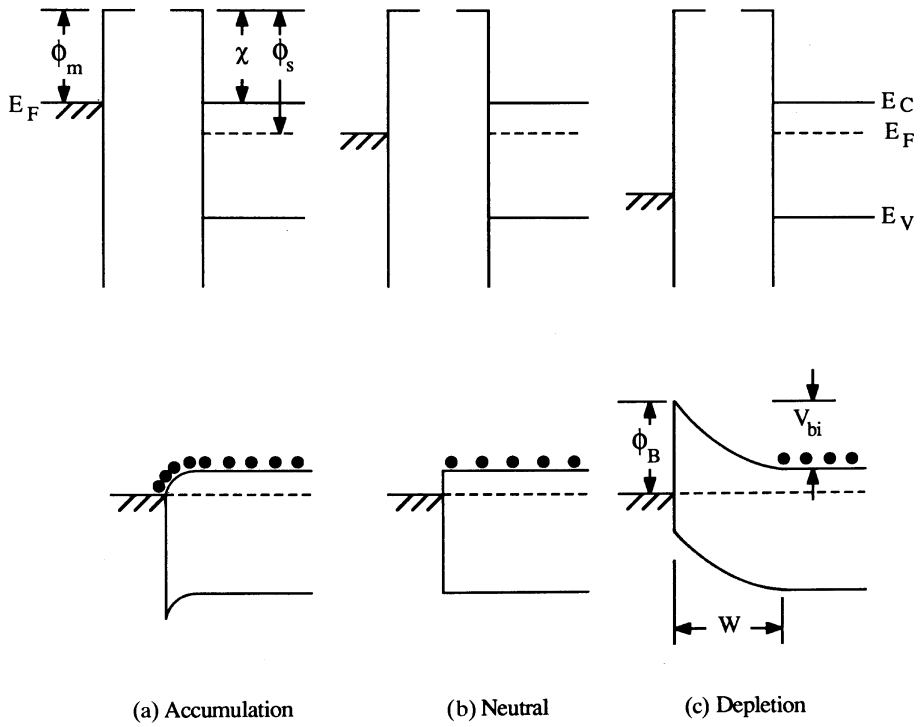


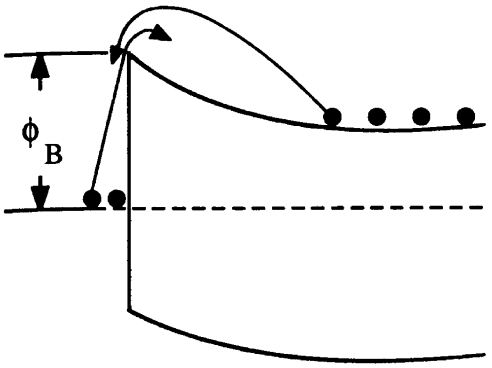
Figure 2.5: Metal-semiconductor contacts according to the simple Schottky model.

proportional to $N_D^{-1/2}$. As such highly doped semiconductors have narrower scr widths. If a metal-semiconductor contact has a narrow scr width, then electrons can tunnel from the metal to the semiconductor or vice-versa. There are three main conduction mechanisms of current flow across a metal/n-type semiconductor contact, which are illustrated in Figure 2.6 [18] where electrons are represented by black dots and their direction of motion by the arrows.

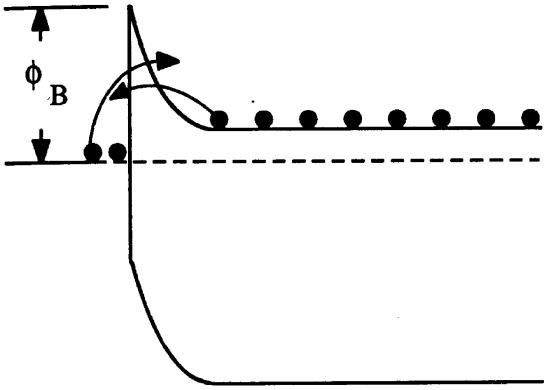
- **Thermionic Emission:** For lowly doped ($N_D \leq 10^{17}$ cm^{-3}) n-type semiconductors/metal contacts the scr width is quite large and this means that most of the current flows as a result of thermionic emission (TE) with electrons thermally excited over the wide barrier.

- **Thermionic-Field Emission:** In intermediately doped (10^{17} cm$^{-3} < N_D < 10^{19}$ cm^{-3}) n-type semiconductor/metal contacts the carriers are thermally excited to an energy where the barrier is sufficiently narrow for tunnelling to take place. This is called thermionic-field emission (TFE).

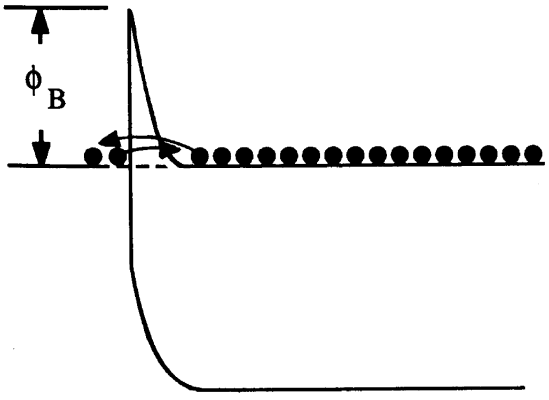
- **Field Emission:** In highly doped ($N_D > 10^{19}$ cm^{-3}) n-type semiconductor/metal



(a) Low N_D - Thermionic Emission



(b) Intermediate N_D - Thermionic/Field Emission



(c) High N_D - Field Emission

Figure 2.6: Depletion-type contacts to n-type substrates with increasing doping concentrations.

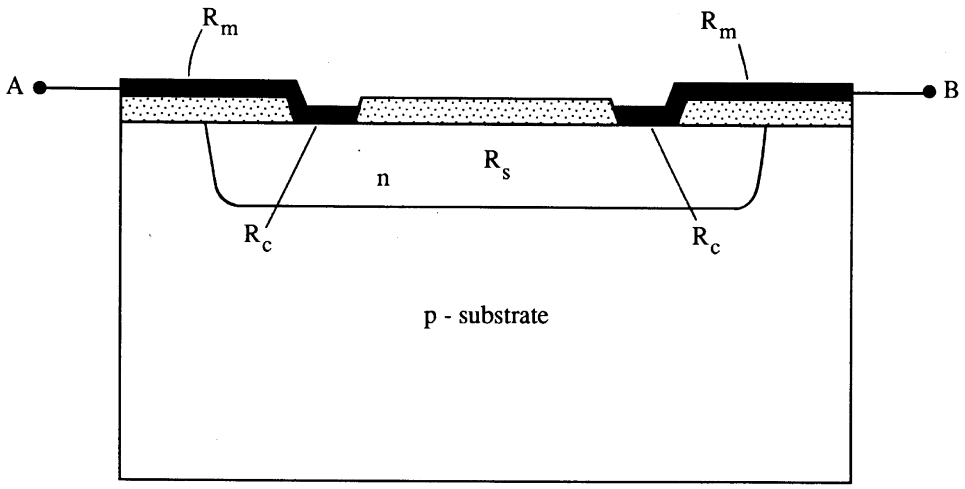


Figure 2.7: Summing the resistances to obtain the total resistance, R_T.

contacts the barrier is so narrow at or near the base of the conduction band that the electrons can tunnel directly through. This is known as field emission (FE).

2.3 Contact Resistance

The total resistance between A and B in Figure 2.7 [18], R_T, can be divided into the resistance of the metallic conductor, R_m, the contact resistance, R_c, and the semiconductor resistance R_s such that Equation 2.13 holds.

$$R_T = 2R_m + 2R_c + R_s \tag{2.13}$$

The metal resistance is the resistance due to the conductor, while the semiconductor resistance is that due to the n-doped semiconductor, which is dependant on the sheet resistance of the diffused layer. The resistance of the metal-semiconductor contact, sometimes called the specific interfacial resistance, determines the contact resistance. This is affected by the portion of the metal immediately above and below the metal-semiconductor interfaces, current-crowding effects, spreading resistance under the contact and the effect that any interfacial oxide may have.

The current density, J, of a contact depends on the applied voltage, V and the barrier height, ϕ_B, in such a way that varies for thermionic, thermionic/field and field emissions.

These variations will be examined shortly.

The contact resistance, measured in ohms, and the specific contact resistance, ρ_c, measured in Ω-cm^2, characterizes the contact resistance. This specific contact resistance, or specific interfacial resistance, is a useful term for ohmic contacts as it is independent of contact area and is thus good for comparing contacts of different sizes.

For metal-semiconductor contacts with lower doping concentrations, where thermionic-emission current dominates the current transport, Equation 2.14 holds.

$$R_c = \frac{k}{qAT} exp(\frac{q\phi_B}{kT}) \tag{2.14}$$

This assumes that the small voltage dependence of the barrier height is negligible [19]. It can then be seen from Equation 2.14 that low barrier heights should be used to obtain smaller values of contact resistance.

For contacts to highly doped silicon where the tunnelling process dominates, the contact resistance depends strongly on doping concentration and varies exponentially with the factor $(\phi_B/\sqrt{N_D})$ [19]. Thus it can be seen that to increase the contact resistance one must increase the barrier height or decrease the surface doping. Increases in barrier height are limited to approximately 0.8 eV for aluminium. While doping may take any value in theory, it is limited to about 10^{19} cm^{-3} for practical purposes in PV cells.

2.4 Barrier Height of Aluminium

When research into Al contacts to silicon was in its infancy, it was realized that the barrier height of the Al appeared to be highly variable [2]. It was found that, for Al contacts to n-type silicon, the barrier height ranged continuously from 0.45 eV to 0.80 eV as a result of post-evaporation heat treatments in the range 100 °C to 550 °C. Aluminium contacts to p-type silicon were found to have a complementary behaviour, with the work function progressively decreasing from 0.75 eV to 0.40 eV over the same temperature range. This was believed to be due to three separate and distinct mechanisms. Firstly, the metallurgical

reactions at the higher temperatures: Si is dissolved in the Al and this recrystallizes as p-type (Al-doped) Si during cooling. Secondly, the reduction of the original SiO_2 layer by the Al, and penetration, at least in certain regions, of the Al below this layer and thirdly, the motion of ionic charge within the oxide layer.

2.5 Epitaxial Growth

Liquid phase epitaxy (LPE) growth is the process by which epitaxial layers can be grown from various metals in which the semiconductor to be grown is soluble. Solid phase epitaxial (SPE) growth occurs when the semiconductor is soluble in the solid phase of the metal in question. In the case of aluminium contacts to silicon, these epitaxial regrowths occur when silicon precipitates out of the aluminium during cooling of samples.

Considering the case of a small amount of aluminium in intimate contact with silicon, one can see from the bottom left-hand corner of Figure 2.8 [16] that the solubility of Si in Al is negligible at room temperature and increases to about 1.5% at 577 °C. As Si diffuses relatively rapidly in Al even at low temperatures of 200 °C to 300 °C [11] and Al diffuses at a negligible rate in Si at these temperatures, the Al remains saturated with Si throughout this process. The eutectic temperature of aluminium and silicon, 577 °C, is the lowest temperature at which these two elements will, when combined in a specific ratio, become a molten state. When the eutectic temperature is reached the alloy melts and the solubility of silicon in aluminium increases dramatically to about 12.2% [11]. From this point the solubility again increases slowly. When the reverse happens and the sample is cooled, silicon precipitates out gradually causing LPE growth until the eutectic temperature is reached. At this point the silicon precipitates out of the aluminium quite rapidly as epitaxial silicon (doped at the solubility limit of Al in Si at that temperature at which it was deposited) and as crystals within the aluminium. As the temperature of the sample is reduced still further, deposition of silicon continues to occur as SPE growth. Due to the high diffusion coefficient of silicon in aluminium, particularly in the molten state, large amounts of silicon can be dissolved and precipitate out when samples are heated above the eutectic temperature and then cooled.

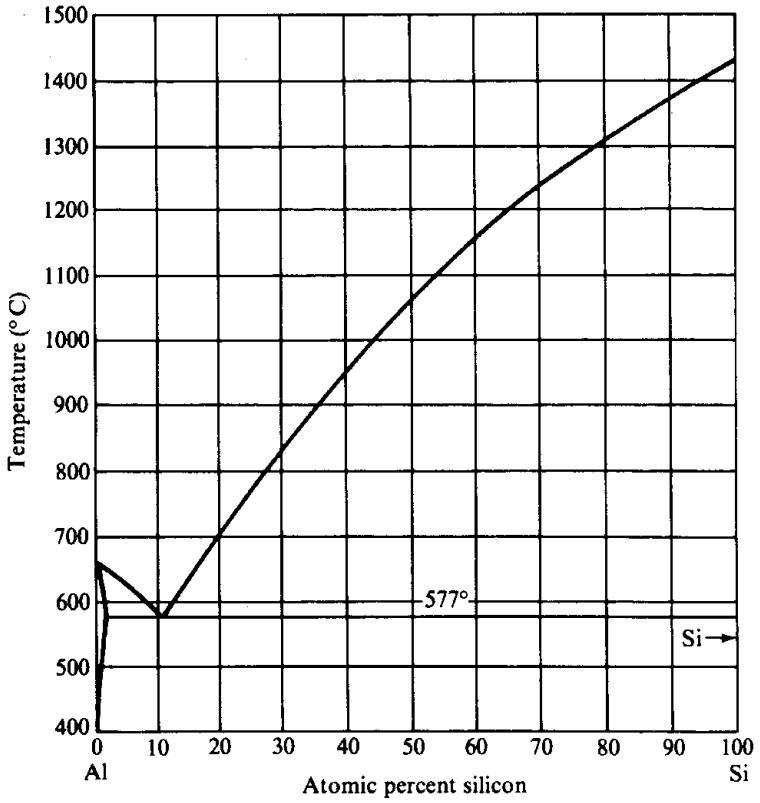


Figure 2.8: Al-Si phase diagram

One perceived negative aspect of using Al contacts is the aspect of Al spiking into the Si. When sintering occurs the native oxide layer between the silicon and aluminium is removed in specific, localized, areas first. This causes the dissolution of silicon to occur rapidly in these areas causing a 'spike' to form in the silicon. This 'spike' may be partially refilled by the epitaxial regrowth that follows during cooling. The amount of regrowth is very small and does not completely fill in the spikes, which may cause shorting or other undesirable effects on the circuitry. The progression of the formation of a spike is shown in Figures 2.9, 2.10 and 2.11.

As a result of the spiking which occurs in Al contacts to Si, the danger it has on circuitry that require good ohmic contacts, and the common use of Al contacts to Si in integrated circuits (IC) much research has been carried out with the aim of producing reliable ohmic contacts with as little pitting (spike formation) as possible.

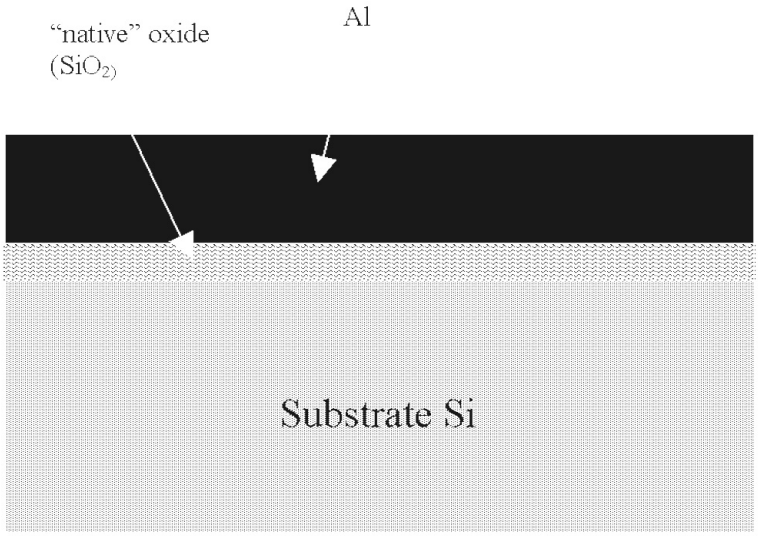


Figure 2.9: Sample prior to sintering.

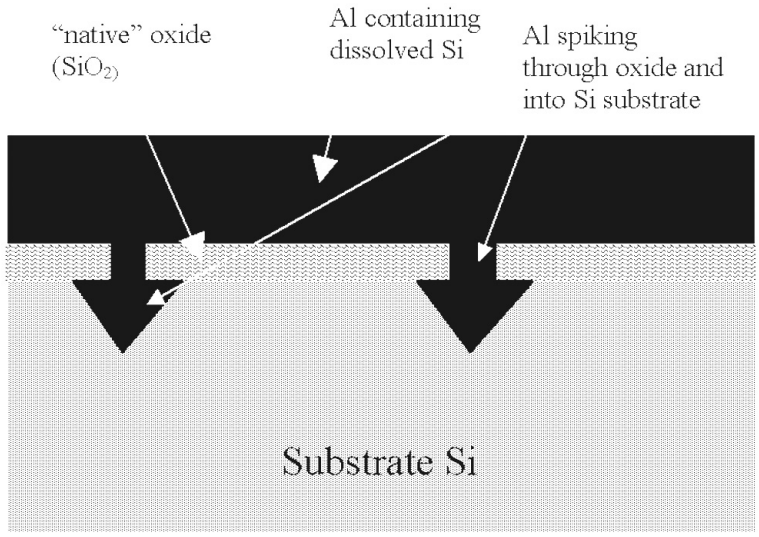


Figure 2.10: Oxide layer is removed more rapidly in certain areas causing spiking of aluminium.

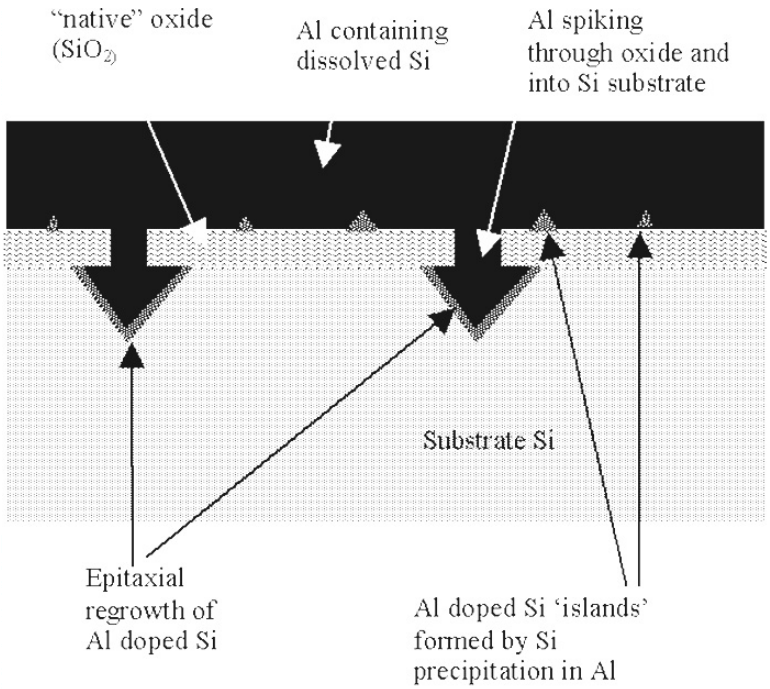


Figure 2.11: Epitaxial regrowth occurs in spikes and across whole contact.

2.5.1 Orientation Dependence of Epitaxial Regrowth on Orientation of Silicon Substrate

It has been found that there is a strong correlation between silicon surface orientation and Al-Si/Si contact resistances [13]. Onoda evaluated Al-Si/Si contact resistances to both (100) and (111) oriented silicon. It was found that for contact to (111) silicon the contact resistance remained constant, while for (100) silicon it increased rapidly under heat treatment at 400 °C for 30 minutes. This is illustrated in Figure 2.12 and these differences in results were purported to be due at least in part to silicon epitaxial growth.

Like aqueous etching, the etching of silicon by metals is crystallographic orientation dependent, and, as in aqueous etching, the slow etching planes are the (111) planes [16]. It should therefore come as no surprise that the epitaxial regrowth on (100) oriented Si was much greater than that of (111) oriented Si which may not have had sufficient time to become saturated with Si in the (111) wafers due to their slower etching rate. As the Si in the (111) plane is dissolved more slowly into the Al than from the (100) plane, the amount of Si available to be redeposited as epitaxial silicon is much less for the wafers in the (111) plane than in the (100) plane. Thus it would appear and was confirmed by Onoda that, if epitaxial growth is a desirable property, then silicon of orientation (100) should be used,

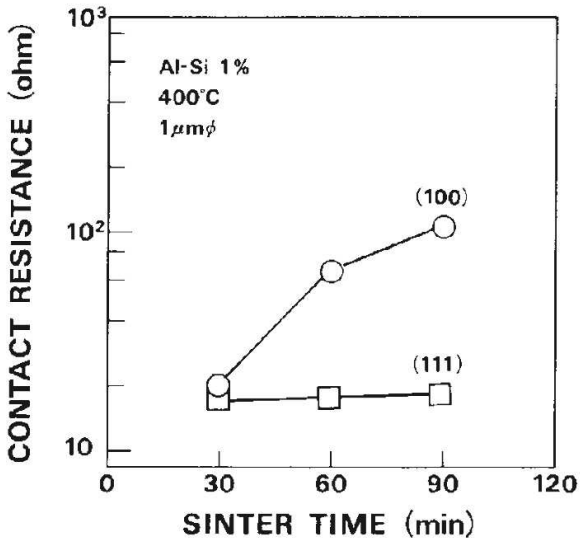


Figure 2.12: Contact resistance change on (100) and (111) substrates with 400 °C sintering time.

but if no epitaxial layer is desired (111) oriented wafers should be utilized. It should be noted, however, that if the samples were sintered for an indefinite period of time the same amount of Si would dissolve into the Al irrespective of what crystallographic orientation Si was used. This would be limited only by the solubility of Si in Al. This would then result in epitaxial layers of more equal thicknesses.

2.5.2 Speed of Diffusion of Silicon in Aluminium

Much research has been done into the diffusion of Si into Al. One method, shown in Figure 2.13 [11], measures the concentration distribution and diffusion length of Si in polycrystalline Al films. By measuring the concentration of Si as a function of distance for a fixed temperatures it is possible to fit the distribution with an error function and then to obtain a value of the diffusion coefficient. The slope of the line gives the activation energy and the diffusion coefficient of Si in Al can be written as:

$$D = D_0 e^{-E_A/kT} = 25 \times 10^{-4} e^{-0.79/kT} \tag{2.15}$$

It is the high diffusivity of Si into Al, along with the fact that the thin layer of interfacial oxide that must first be dissolved does not fail uniformly, that is responsible for the Al 'spikes'. Once the interfacial oxide layer fills in one region, enough silicon diffuses rapidly

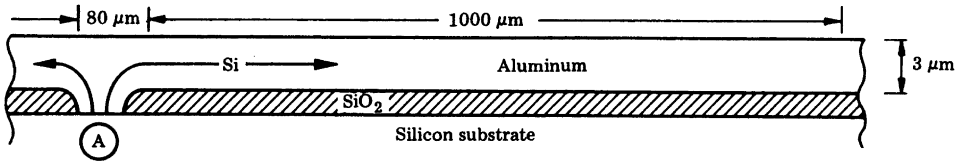


Figure 2.13: Diffusion of Si into Al.

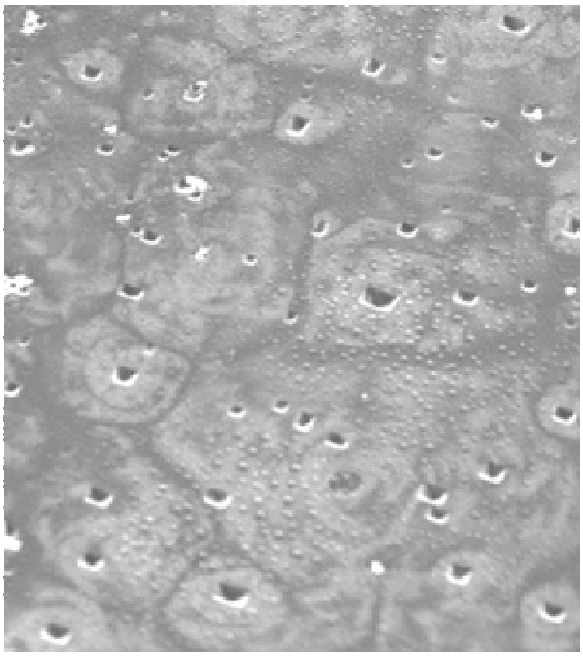


Figure 2.14: Resulting topography due to aluminium spiking. The Al has been chemically etched.

in to the aluminium bulk to saturate much of the contact and thus limit dissolution over the remainder of the contact area. This high diffusivity of Si in Al [11] allows the concentration gradient to remain quite low resulting in continued dissolution of the Si at the site of the 'spike' as long as there is an increase in the saturation limit of Si in Al (possibly by increasing temperature). Chemical etching to remove the Al layer also dissolves the regions in the Si where the Al penetrated and the spikes are then observed as pits in the Si. (See Figure 2.14)

2.5.3 Rapid Thermal Annealing (RTA) and Rapid Thermal Processing (RTP)

Many people [7, 15, 14] have researched this problem of spiking and one way that has been found of reducing the degree of Al spiking is to increase the processing temperature rapidly and sinter the contacts at high temperatures for short periods of time. This

is called rapid thermal processing (RTP) or rapid thermal annealing (RTA). The short sintering periods do not allow much diffusion/dissolution of Si into the Al and thus Al spiking is reduced. RTAs or RTPs are usually performed in a much smaller chamber than a conventional furnace's chamber and the samples are heated by halogen lamps that can be heated rapidly and are cooled, rapidly if necessary, using a nitrogen flow over them.

2.5.4 Contact Area

Pai et al [14] observed that there was a linear relationship between the contact resistance and the contact area after RTA and concluded that this indicated that the contact interface was relatively uniform. It was also noted that for short-time annealing of 1 s to 10 s in a conventional furnace at 426 °C also yielded low contact resistivity 6 x 10^{-7} Ωcm^2 and improved contact morphology. These results were attributed to the reduced Si migration into the Al layer during the short duration of the anneal.

2.5.5 Ion Mixing to Reduce Al Spiking

Pai et al [14] also studied the effect of ion mixing on the contact resistance and contact morphology of samples that underwent RTA. Ion mixing occurs when ions such as As^+ [14] or boron ions [7] are implanted through the Al into the interfacial region (between the Al and Si) to cause the native oxide layer to be broken in numerous places. The expected result of this removal of the interfacial (oxide) layer would of course be a more homogenous erosion of Si and as a result improved uniformity of the contact should occur. Pai et al [14] found that the contact resistivity increased with ion dosage.

Hara et al [7] agreed with Pai et al [14] in that the Al spikes and Si precipitates were reduced in the short time sintering. Also, they observed a decrease in contact resistance due to using RTA over a furnace and due to increased doses of B. These results are shown graphically in Figure 2.15 [7].

Al spiking can also be reduced by deposition of an Al layer containing up to 5% Si [7, 6, 12, 4]. This, however, introduces another problem in that the excess Si in the Al can precipitate during heat treatment forming crystallites of Si on the Si surface. These are

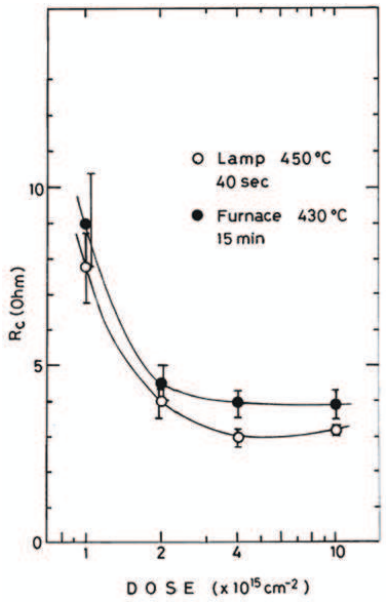


Figure 2.15: Contact resistances resulting from RTA and conventional furnace at various doses of B ion implantation.

doped with Al atoms and are thus of p-type conductivity.

Rather than having the Si contained in the Al during deposition, some researchers studied the effect of depositing a thin film of amorphous silicon or polysilicon [14, 10, 6] prior to Al deposition. When a 6 nm poly-Si layer was applied first to n^+ type Si and then 1 μm Al added, it was found by Finetti et al [6]that a high contact resistivity of the order of 10^{-1} Ω-cm^2 was measured for the metallization as deposited. This high contact resistivity was deduced to be due to the high resistivity poly-Si layer. The contact resistivity then decreased to about 10^{-2} Ω-cm^2 as sintering up to 400 °C was applied. At this stage a more rapid decrease in contact resistivity was observed such that the contact resistivity reached 3 x 10^{-4} Ω-cm^2 at a sintering temperature of 500 °C. This was higher than the resistivity value obtained for the corresponding sinter with Al/n^+Si contact, thus indicating that the dissolution of polysilicon was incomplete.

2.5.6 Removal of Interfacial Oxide Layer

The fact that the removal of the interfacial oxide layer is not uniform has been demonstrated and utilized by Ho and Wenham [9] to create buried, localized contacts for solar cells. These contacts were formed through a thick layer of oxide. Sintering was performed

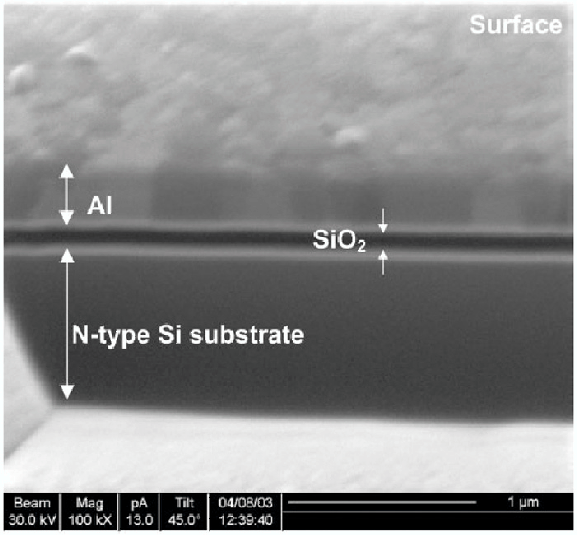


Figure 2.16: Focussed ion beam image of a cross-section of a tilted n-type Si sample with Al on 211.0 nm SiO_2 prior to sintering.

at temperatures of about 500 °C for periods of between 5 hours and 20 hours. Figures 2.16 and 2.17 illustrate the initial setup and the resulting dissolution of silicon dioxide/silion in localized areas respectively. These are clear evidence for the occurrence of localized holes being formed in oxide layers which then result in Al spiking.

2.5.7 Partially Ionized Beam (PIB) Deposition of Aluminium

Partially ionized beam deposition techniques involves depositing metal ions, usually about 1.6% [20], along with the metal to be deposited. The metal is deposited by accelerating it towards the surface of the substrate via electric fields under high vacuum. This results in the native oxide layer being removed and intimate contact being made between the metal and the substrate. Yapsir et al [20] found that utilizing PIB deposition techniques resulted in much shallower pit formation on the Si surface when compared to depositions which left the native oxide intact before sintering. This is to be expected as a lack of native oxide layer between the Al and Si would result in a more homogenous dissolution of Si into Al from across the whole contact.

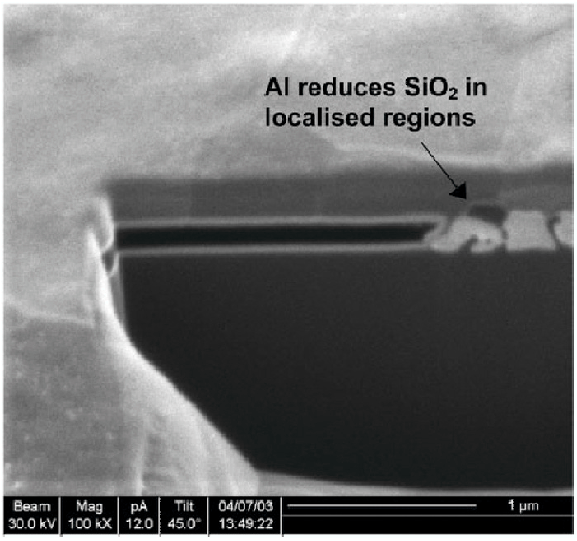


Figure 2.17: Focussed ion beam image of a cross-section of a tilted n-type Si sample with Al on 211.0 nm SiO_2 after 15 hour sinter.

2.5.8 Avoiding Formation of p-type Epitaxial Layer

Faith et al [5] examined the effect that sintering contacts of different ratios of Al:Si had on the contact resistance values for sintering temperatures ranging from 325-500 °C and contact sizes 3-5 μm. The maintenance of consistent, low-resistance ohmic contacts throughout post-alloy processing was found to depend on the silicon concentration in the aluminium being high enough to keep the aluminium supersaturated during all post-deposition temperature cycling. Once this condition of having sufficiently high Si was met the contact resistance values were independent of the Al-Si alloy composition. It was also found that silicon pitting in the contact cut was not required to achieve good ohmic contact. If all of the Si in the Al that was deposited did not become molten during the anneal then, the microcrystals of Si which remained could act as 'seeds' for the growth of Si once cooling began. This could dramatically reduce the amount of epitaxial growth on the Si surface.

2.6 Summary of Review

From these works it can be seen that most of the research has been completed with the aim of forming ohmic Al/Si contacts and to this end most annealing temperatures occurred below the eutectic temperature to avoid Al spiking and minimize the amount of

epitaxial Si regrowth. The work reported in the literature over the past four decades has shown that uniform oxide removal and/or minimization of spiking can be achieved using special techniques, such as partially ionized beam deposition techniques, particularly in conjunction with RTA, or by ensuring that there is a sufficient amount of Si in the Al to prevent dissolution of the Si substrate during the annealing process. However, no papers were found that aimed to determine the conditions under which reliable rectifying contact could be formed to n-type Si. Also, the effect of the composition of the gas under which these anneals took place and the effect of having different thicknesses of aluminium for the contacts appears not to have been examined. It was also found that some of the results obtained by different authors differed from each other. This is illustrated by that fact that Sze [19] reported a value for the contact resistance of Al to Si with a doping level of 10^{19} dopant atoms cm^{-3} of 8 x 10^{-1} Ω-cm^2, while Schroeder [18] reported it as being 5 x 10^{-3} Ω-cm^2. This is more than two orders of magnitude difference and illustrates the difficulty of obtaining consistent data on this subject that is able to be cross-referenced.

Experimental Procedure and Characterization

There are four main techniques of determining the specific contact resistance of a contact. There are two-terminal, three-terminal, four-terminal and six-terminal methods. In the two-terminal contact resistance measurement method, shown in Figure 3.1, which is the earliest and simplest method, a contact of a known radius, r, is formed on the top surface and a blanket contact deposited on the rear. For the two terminal method, the total (measured) resistance R_T is given by:

$$R_T = R_{sp} + R_c + R_0 \tag{3.1}$$

where R_{sp} is the spreading resistance under the top contact, R_c is the contact resistance of the top contact to be determined, and R_0 accounts for the resistance of the bottom contact. This bottom contact usually has a very large contact area with a concomitant small resistance. As a result, R_0 is usually neglected.

The spreading resistance accounts for the bulk sample resistance and is given by:

$$R_{sp} = \frac{\rho}{2\pi r} arctan(\frac{2T}{r}) \tag{3.2}$$

where r is the circular top contact radius and T is the sample thickness. Equation 3.2 is a reasonable approximation to the resistance of a semiconductor slab with a contact radius, r, on the top and a large contact on the bottom. With the current flowing vertically into

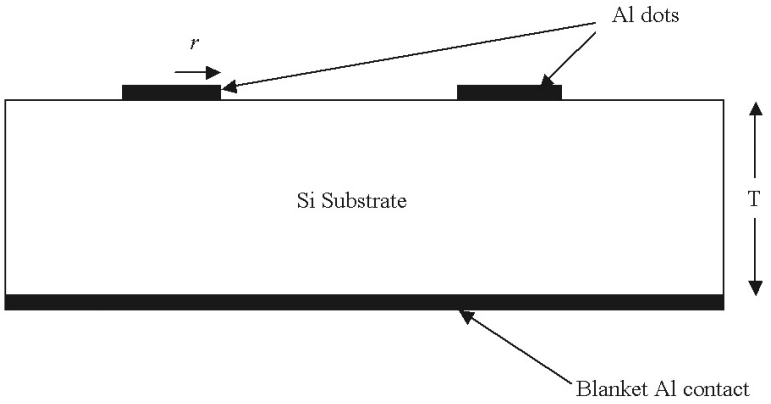


Figure 3.1: Two-terminal contact resistance method

the top contact the contact resistance can be written as:

$$R_c = \frac{\rho_c}{A_c} = \frac{\rho_c}{2\pi r^2} \tag{3.3}$$

where ρ_c is the specific contact resistance and A_c is the area through which the uniform current flows. For small R_0 it is obvious from Equation 3.1 that the contact resistance is the difference between the total resistance and the spreading resistance: the difference of two large numbers. The spreading resistance cannot be measured and it is difficult to calculate accurately. But small errors in R_{sp} can lead to large errors in R_c. Hence this method works best when $R_{sp} < R_c$. This can be approximated by using small-area contacts. For small r we find that the requirement of $R_{sp} < R_c$ leading to:

$$r < \frac{4\rho_c}{\pi\rho} \tag{3.4}$$

The three, four and six-terminal techniques often require special photolithographic steps and substantially more processing. Of the methods available the two-terminal method was the most basic and yielded reliable results for the purposes of the study at hand and thus was applied.

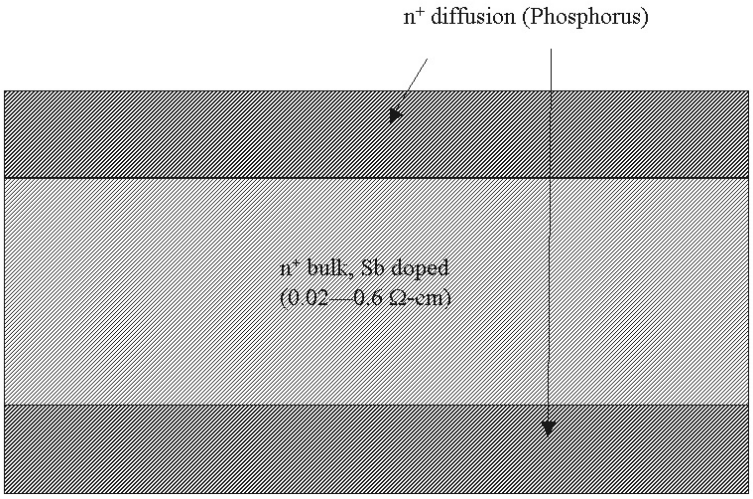


Figure 3.2: Wafers prior to Metalization

3.1 Preparation of Samples

Czochralski grown, (100) oriented, 4", n-type, Sb doped silicon wafers that were polished on one side and had resistivities in the range of 0.02 Ω-cm to 0.06 Ω-cm were utilised in the experiments performed.

Figure 3.2 illustrates the diffusions/doping of the wafers used. The wafers were made to have n^{++} doping on the rear in order to ensure that negligible contact resistance would result for the rear contact. They were also produced such that there was an n^{+} layer on the polished side in order to simulate the concentration of n doping near the p^{+} region in a typical PV cell. The whole wafer was relatively heavily doped n-type to reduce the bulk resistance of the wafer. These wafers were prepared via the following process.

Firstly the wafers were RCA cleaned. This involved a:

Phosphorus diffusions

- 10 minute dip in 5:1:1 $H_2O/NH_4OH/H_2O_2$ solution preheated to 80 °C.
- Rinse in deionised (DI) water for 1 minute.
- 10 minute dip in 5:1:1 $H_2O/HCl/H_2O_2$ solution preheated to 80 °C.
- Rinse in DI water for 1 minute.

The wafers were then dipped in HF acid ($\tilde{5}\%$) until hydrophobic. Following this a light phosphorus diffusion on both sides of the wafers was performed by:

- Loading samples into the furnace at 790 °C with O_2 flow (bubbling through $POCl_3$) of 105 standard cubic centimetres/minute (sccm) and N_2 flow (bubbling through $POCl_3$) of 75 sccm and a main flow of N_2, from which the phosphorus is utilised to make the n-type doping, at 247 L/hour.
- Maintaining this for 20 minutes.
- Switching of both bubbler flows and maintaining 10 minutes.
- Ramping furnace to 850 °C in 10 minutes.
- Maintaining this temperature for 45 minutes.
- Cooling furnace to 800 °C in 3 minutes and removing the samples.

Following this an oxidation was performed to create a thick oxide over the wafer and also to drive the phosphorus diffusion further into the wafer, thus lowering the P surface concentration to around 10^{18} atoms of P/cm^3. This was achieved as follows:

- Wafers were loaded into the furnace at less than 800 °C with a O_2 flow rate of 160 L/hour.
- The furnace was ramped up to 1100 °C in 23 minutes.
- N_2 and O_2 flows bubbling through 1, 1, 1 - trichloroethane (TCA) were set to 10 L/hour and 5 L/hour respectively and furnace temperature maintained for 100 minutes.
- N_2 and O_2 flows bubbling through TCA were switched off and furnace temperature maintained for a further 15 minutes.
- O_2 flow was switched off, N_2 flow was set to 180 L/hour and the furnace was then ramped down to 800 °C in 25 minutes.
- The wafers were finally removed and the N_2 flow switched off.

The oxide was then removed from the rear of the wafers by causing HF gas to fume on the rear of the wafers until it was hydrophobic. This took about 6 minutes. The wafers were then rinsed in DI water and a heavy phosphorus diffusion performed as follows:

- Wafers were positioned such that they were front to front and loaded at 800 °C with O_2 flow (bubbling through $POCl_3$) at 50 sccm and the main N_2 flow at 247 L/hr.
- Furnace was ramped to 860 °C in 5 minutes.
- N_2 flow (bubbling through $POCl_3$) was set to 125 sccm and wafers sintered for 30 minutes.
- Bubblers were turned off and the furnace allowed to cool to 800 °C in 5 minutes before wafers were removed.

This resulted in a heavy phosphorus diffusion on the rear sides of the wafers.

Aluminium deposition

After the phosphorus diffusions were complete and directly prior to the deposition of Al dots the oxide layer was removed by dipping the wafers/quarter wafers in 5-10% HF solution. The aluminium was then deposited onto the front in the form of dots with diameters of about 0.7 mm through the use of a screen. This removal of the oxide from the wafer directly before aluminium of deposition ensured that there was a minimal amount of 'native' oxide between the aluminium and silicon. The 'native' oxide is the oxide that is formed on the wafer when it is exposed to the atmosphere at ambient temperatures. This oxide is of the order of a monolayer thick. The formation of this oxide layer could not be avoided, but was minimized by keeping the transition time from HF dip to deposition of aluminium to a minimum (about 20 minutes). The aluminium that was used in these depositions was either of 99.9% purity (3N) or 99.999% purity (5N). The process of aluminium deposition was via a thermal evaporation as follows:

- Aluminium pellets were placed in tungsten boats until boats were at capacity. This was done for all three boat positions.

- Samples were placed in evaporation chamber with polished side facing down onto the screen with dots of 0.7 mm diameter.
- 2 glass slides were then placed on top of the sample to inhibit it vibrating out of position during deposition.
- The chamber was closed and the pressure reduced to $< 3.0 \times 10^{-6}$ Torr.
- The Inficon XMS-1 controller was set to measure the thickness of Al deposited (even in the case of 98%Al/2%Si deposition).
- Current through the tungsten boat was gradually increased to achieve a deposition rate of 0.001 to 0.005 μm/sec and the required amount of Al deposited.
- Chamber was allowed to cool for about 1 minute before being opened and samples removed.

Following the aluminium deposition, the samples were further cleaved into 1 cm^2 pieces. These were then given sintered in forming gas or N_2 gas at temperatures in the range of 400 °C to 650 °C, for periods of time ranging from 0 min to 2 hours, and were removed from the furnace under conditions varying from rapid removal and placement on a piece of metal (to allow for rapid dissipation of thermal energy) within 30 seconds to allowing the samples to cool in the furnace to below 400 ° C. The forming gas was composed of 95% ± 1% Ar and 95% ± 1% H_2 with the maximum impurities being: 200 ppm N_2, 15 ppm moisture, 10 ppm O_2, 10 ppm hydrocarbons, 5 ppm CO_2 and 2 ppm CO. The N_2 was supplied from a source of liquid nitrogen and was therefore also of extremely high quality. Some samples were annealed in the RTA for up to 15 minutes at maximum temperatures of 600 °C in forming gas composed of 95% N_2 and 5% H_2.

Following sintering, the samples were either prepared for viewing of topography or for IV measurements. The former involved the samples being placed in a solution of phosphoric acid, a solution of $10H_2O$: $1HNO_3$: 10HC, or a $1HNO_3$: 10HCl solution. Some samples were placed in the solution before, after and during the heating of these solutions, but all were allowed to continue to remain in the solution until no reaction was evidenced (by a lack of bubbles forming where the Al dots were). At this point the samples were removed and rinsed 3 times with DI water. The preparation for IV measurements involved dipping

the samples in 5-10% HF to remove oxide and followed by a deposition of aluminium as explained earlier, except that no screen and glass slides were utilized and that the rear of the sample (the unpolished side) was made to face down (toward the aluminium sources). These samples were then tested by measuring their IV characteristics. This was achieved via the two-terminal method explained earlier.

3.2 Testing Using Current/Voltage Measurements

The IV characteristics were determined by measuring the current across the sample from the front dot to the rear when voltages between -1 V and +1 V were applied. From this, resistances of the contacts at the voltages around which PV cells operate (0.5 V to 0.6 V) were then calculated.

3.3 Observation of Topography of Surfaces (SEM)

After the removal of the aluminium, the samples were then observed under an optical microscope. Some of these samples were then observed under a Cambridge S360 scanning electron microscope (SEM).

3.3.1 SEM in Secondary Electron Mode

An SEM in secondary electron mode is similar to a light microscope, with the exception that, instead of photons, electrons are used. This has two main advantages: much larger magnifications are possible since electron wavelengths are mush shorter than photon wavelengths and the depth of field can be much larger. An SEM in secondary electron mode works by scanning the sample with a focused electron beam and detecting the electrons that are subsequently emitted by the substance being viewed. The contrast in an SEM depends on a number of factors. For a flat sample that is uniform the image shows no contrast as would be expected. Contrast is affected by surface conditions and by local electric fields. However, the main contrast enhancing feature is the sample topography. Secondary electrons are emitted from the top 10 nm or so of the sample surface. When the

sample surface is tilted from normal beam incidence, the electron beam path lying within this 10 nm is increased by the factor $1/\cos\Theta$, where Θ is the angle from normal incidence. The interaction of the incident beam with the sample increases with path length and thus secondary electron emission coefficient increases.

It is this angle effect that is responsible for the striking three-dimensional nature of SEM images. These striking pictures come, not only from this angle effect, but also from the fact that the detectors attracts and collects electrons even if they leave the sample in a direction away from the detector. This does not occur in optical microscopes, where light reflected from a sample passes through a lens and is formed into an image. In an SEM no true image exists. Rather, secondary electron densities are measured and displayed.

3.3.2 SEM in Backscattering Mode

When an SEM is in backscattering mode it collects, measures, and displays densities of backscattered electrons. These are the electrons that are not absorbed by the substance being observed, but are reflected backwards. These electrons can be differentiated from those of secondary electrons by the fact that secondary electrons have a much lower energy than those of backscattered electrons. If the sample consists of materials with different atomic numbers, a contrast is observed if the signal is obtained from backscattered electrons, because the backscattering coefficient increases with atomic number, Z. The effect of angle also introduces contrast into both backscattering and secondary electron SEM images.

3.3.3 Electron Microprobe (EMP)

EMP utilizes the incident electrons of an SEM, however, an X-ray detector is added and thus it is not surprising that many SEMs have EMP capability. Two different types of detectors can be used: energy-dispersive spectrometers (EDS) and wavelength-dispersive spectrometers (WDS).

EDS utilizes an X-ray detector composed of a reverse-biased semiconductor pin or a Schottky diode. The energy of incident X-rays is determined in the detector by the number of

electron hole pairs the X-rays produce. On the other hand, WDS directs X-rays directly from the sample onto an analyzing crystal. Only those X-rays that strike the crystal at a specific angle are diffracted through a polypropylene window onto the detector, usually a gas proportional counter. An absorbed X-ray thus crates a shower of electrons and positive ions. The electrons are then attracted to the wire and produce a charge pulse. The analyzing crystals used have quite small wavelength ranges and thus a number of crystals are necessary to span an appreciable wavelength range.

EDS and WDS complement each other. The EDS are good for rapid sample analysis while WDS provides high-resolution measurements over a longer time. WDS detectors have larger collection areas and are located at longer distances from the sample, giving them lower collection efficiencies than EDS detectors. WDS has higher energy resolution since only a small range of wavelengths is detected at one time, allowing greater peak-to-background ratios and higher count rates for individual elements. This gives approximately 1 to 2 orders of magnitude better sensitivity, but makes the method slow.

3.4 Determination of Depth Profile of Samples via SIMS

Some pieces of the wafers that had received phosphorus diffusions and wafers that had been metallized utilized a Riber MIQ256 SIMS Spectrometer to determine qualitative and some quantitative properties of the depth profiles that these process result in. The SIMS uses O^{2+} and Ca^{2+} ions to bombard the sample, resulting in ions of the materials within the sample being produced. These were then collected and channelled by powerful electromagnetic fields to a mass spectrometer where it can be determined which type of molecular/atomic ion each is based on their charge and mass. P, Al, Sb and Si were the elements observed in this case. Some of these elements may be sputtered off the sample in molecules. If the number of ions produced in the atomic form are excessive so as to flood the receiver, the mass being observed can then be altered to measure the frequency of the molecular ions. All the results obtained by this means are only qualitative as, there is know way of knowing what the true scale of the concentration is. Thus, if a quantitative result is required, calibration samples must be used. This involves implanting known amounts of a substance into a sample and performing SIMS on this sample. By comparing the known

profile of the implanted sample with that of the actual samples, a quantitative result of the concentration of the dopant/metal at all the depths covered can be determined once the depth to which the profile was measured is determined. This can be determined using a surface profiler

3.5 Surface Profiling

To determine the depth scale of the SIMS, a Temcor Alpha Step 200 surface profiler was used. It worked by running a probe in a line across the surface and the hole produced by the SIMS. This was displayed on a screen along with a depth scale. Thus the depth of the hole produced can be measured and the time scale from the SIMS output could be converted to a depth scale, assuming that the sputtering rate is constant. This device was also used for checking the height of the aluminium dot deposition step that original utilised an inficon-varian measuring device.

3.6 Summary of Procedure

Some of the variables that were be altered include the temperature of the sinter, rate of heating, rate of cooling, purity of Al deposited, thickness of Al deposited and the time of sintering of the metallized samples. Through utilizing the characterization techniques mentioned and varying the sintering conditions and the form of the contact it was anticipated that an improved process for producing rectifying contacts to n-type silicon could be produced.

Results & Discussion

All SEM images shown were taken at 45° unless otherwise stated. This provided a good depth of view to the images.

4.1 Verification of Validity of IV Measurement Technique

Czochralski grown, (100) oriented, 4", n-type, Sb doped silicon wafers that were polished on one side and had resistivities in the range of 0.02 Ω-cm to 0.06 Ω-cm were treated with a heavy phosphorus diffusion on both the front and rear. This resulted in a wafer shown diagrammatically in Figure 4.1. This wafer was then dipped in a HF solution until hydrophobic to remove the layer of oxide that had formed during the phosphorus diffusion. Following this, 20 nm Cr, 20 nm Pd and 260 nm Ag were deposited in 0.7 mm diameter dots on the front (polished) surface. This combination of Cr, Pd and Ag is known to result in excellent ohmic contact to silicon. 320 nm Al was then deposited on the rear of the sample. When this standard was tested, via the two-terminal method, a characteristic ohmic contact was observed as illustrated in Figure 4.2. The data that is level, on the left and right hand side of Figure 4.2, indicate that the current measuring device was saturated. The resistance measured was 0.35 Ω. Thus the contact resistivity was 0.35 x A = 0.35 x πr^2 = 1.3 mΩ-cm^2. This resistivity is due to the bulk resistivity as the contact resistance to the front and rear of the sample are assumed to be negligible. This bulk resistivity is also called the spreading resistivity of the sample, R_{sp}. The theoretical value of the resistance of the contact can be calculated using:

$$R_{sp} = \frac{\rho}{2\pi r} arctan(\frac{2T}{r}) \tag{4.1}$$

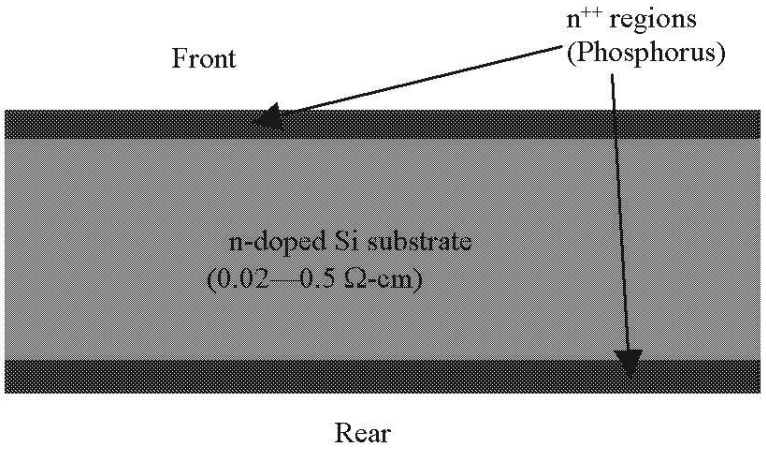


Figure 4.1: Diagram illustrating diffusions in Silicon used for finding bulk resistance.

where T is the thickness of the wafer (0.5 mm) and r is the radius of the dot (0.35 mm). This yields 0.33 Ω. This is very close to the resistance that was measured (0.35 Ω). The bulk resistance is the minimum resistance that will be able to be measured for all of the samples that were made as all the samples utilised wafers of the same bulk resistivity.

4.2 Conventional Furnace Sintering Below the Eutectic Temperature

Samples were prepared with dots of 3N Al on the front of diameter approximately 0.7 mm, sintered at temperatures ranging from 400 °C to 500 °C and subsequently cooled to room temperature in times ranging from 30 seconds to 40 minutes. As evidenced by the black areas in Figure 4.3, significant spiking occurred when the sample with 1.0 μm was sintered at 500 °C for 30 minutes and cooled rapidly. Figure 4.3 also shows crystals of silicon on the surface (as the lighter parts).

Figure 4.4 illustrates the general current and voltage current characteristics of these samples. This particular data was collected from a sample which had 0.3 μm 3N Al dots sintered at 500 °C for 30 minutes and cooled slowly. As was explained earlier, PV cells are designed to operate at their maximum power that usually occurs at a voltage of between 0.5 V and 0.6 V. Thus to measure the effective shunt resistance of a cell that was operating, the resistances of samples in this region were determined. It can be seen from Figures 4.6 that the resistances at voltages of between 0.53 V and 0.56 V of these samples

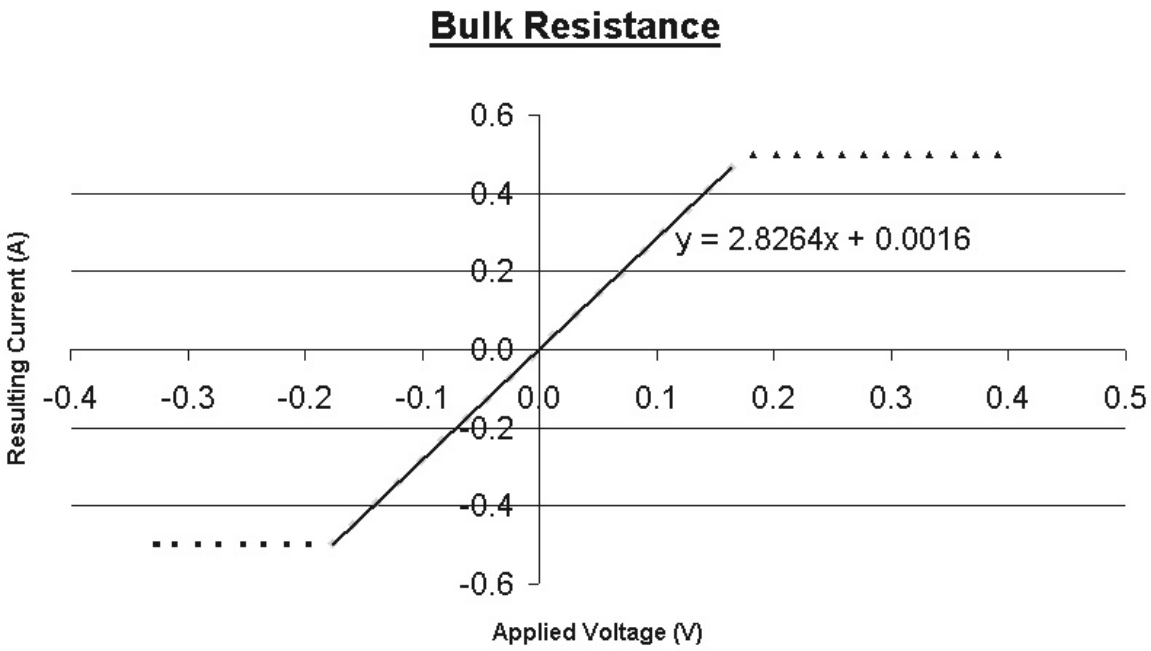


Figure 4.2: Bulk resistance of wafers used.

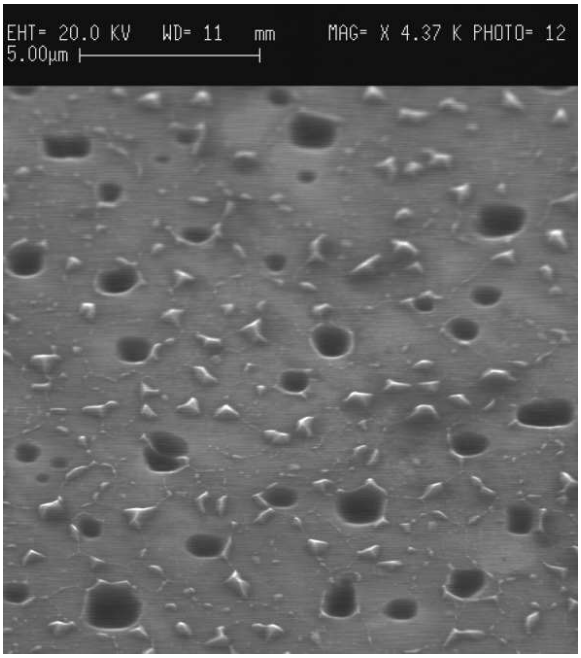


Figure 4.3: SEM image (in secondary electron mode) of Al spiking and crystal growth in a sample with 1.0 μm Al sintered at 500 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed.

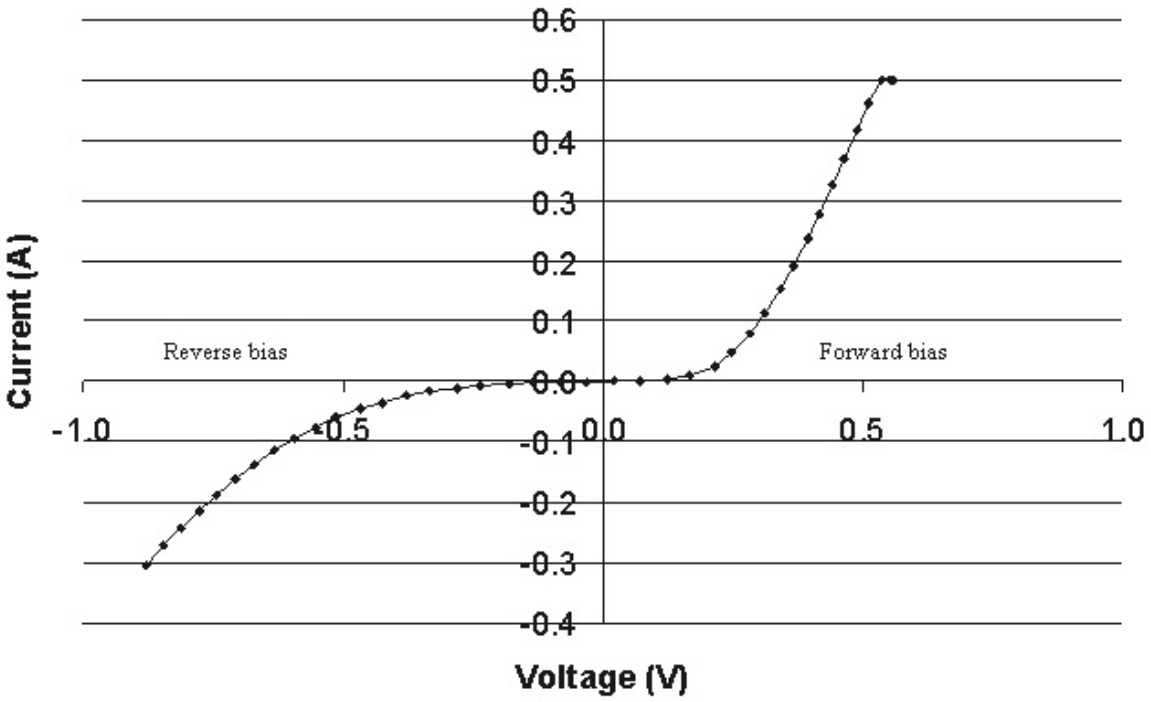


Figure 4.4: Typical IV curve for samples sintered below the eutectic temperature in a conventional furnace.

are very low (well under 100 Ω). It should be noted that there is one data point that shows a resistance of approximately 130 Ω. This data point came from a sample that had 1.0 μm 3N Al dots, was sintered for 30 minutes at 500 °C and was cooled over about 30 minutes to room temperature.

4.2.1 Effect of Al Thickness

Samples were prepared with 3N Al dots of thickness 0.3 μm and 1.0 μm. Figure 4.5 when compared to Figure 4.3 illustrates the differences in topography observed due to thickness of Al deposited. It can be seen that the sample with 0.3 μm Al resulted in a smoother surface around the spikes than that with 1.0 μm Al. The resulting differences in the metal contacts were also evidenced by differences in the IV characteristics of the samples. These are illustrated in Figure 4.6. From this it can be seen that the resistances of the samples that had 1.0 μm of 3N Al dots were more widely spread than those of 0.3 μm indicating that the smoothness of the samples was indicative of the quality of the contact.

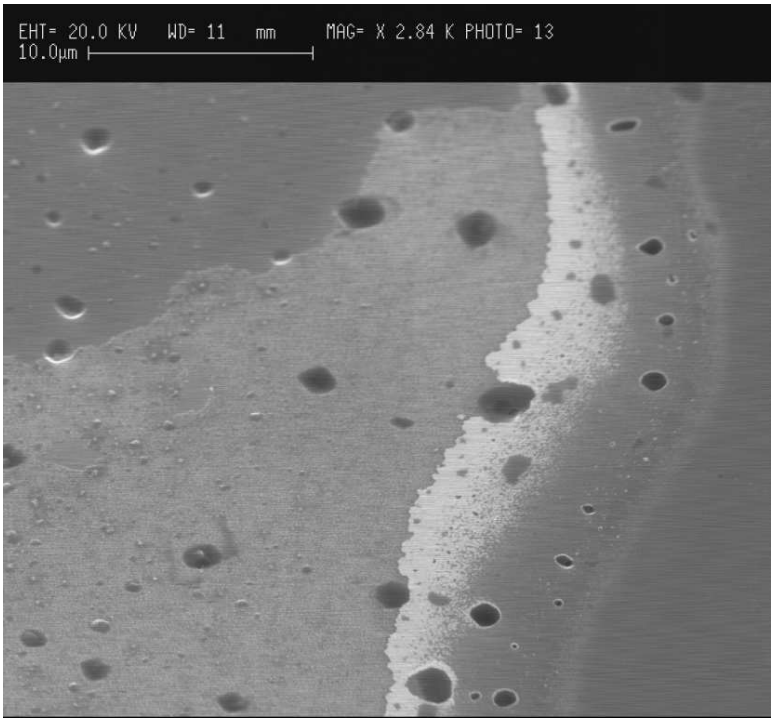


Figure 4.5: SEM image (in secondary electron mode) of Al spiking and epitaxial growth on a sample with 0.3 μm Al dots sintered at 500 °C for 30 minutes and cooled to room temperature within 30 seconds.The Al has been removed.

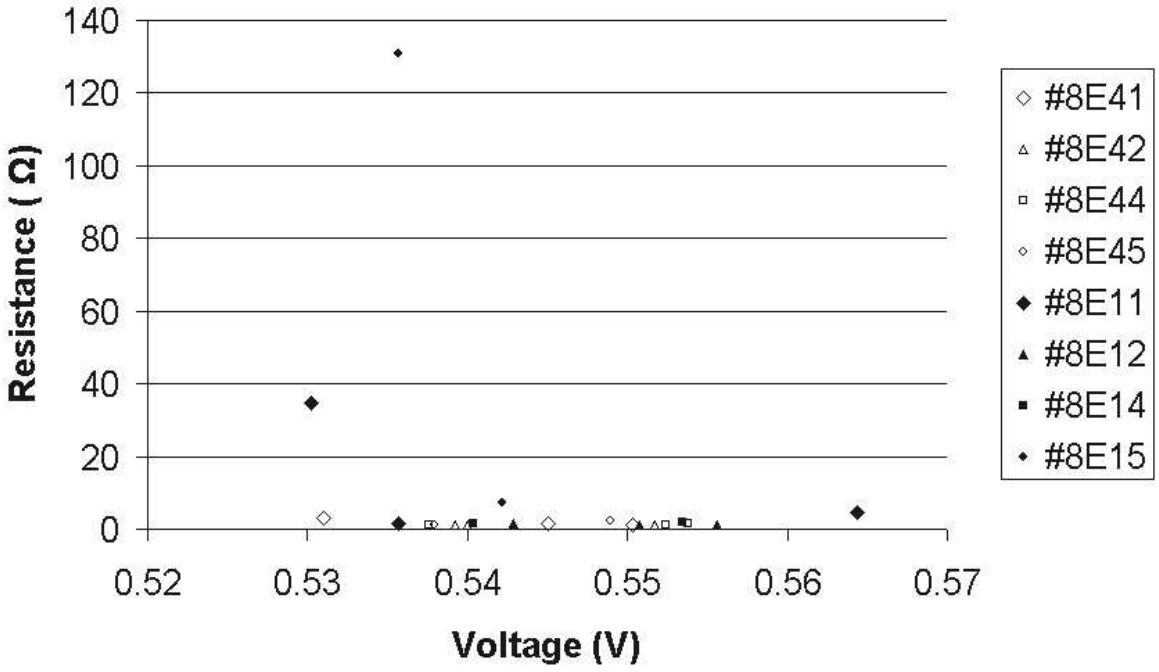


Figure 4.6: Effective resistances of these samples that were heated to below the eutectic temperature in a conventional furnace.

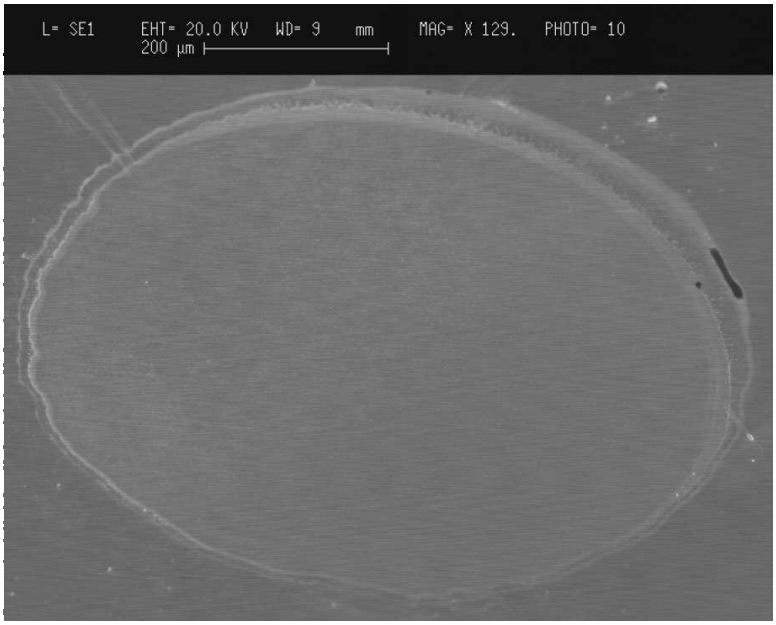


Figure 4.7: SEM image (in secondary electron mode) of a single Al dot which was 0.3 μm Al thick sintered at 400 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed.

4.2.2 Effect of Cooling Rate

Some samples were taken from the furnace immediately after sintering and placed on a metal block to cause rapid cooling while others were allowed to cool to below 400 °C in the furnace before being removed and allowed to cool on the sample holder (which was also in the furnace during sintering).

The rate of cooling of the sample after sintering at these temperatures appeared to have minimal effect on the surface topography with both samples appearing similar to Figure 4.7 and having spikes of cross section approximately 1 μm as illustrated in Figure 4.8. This minimal effect of cooling rate on contact was also confirmed by IV measurements illustrated in Figure 4.6. Samples ending in a '1' or '2' were cooled in about 30 seconds, while sample ending in a '3' or '4' were cooled in the furnace for about 30 minutes before being removed.

In conclusion, these results indicate that when samples were sintered below the eutectic temperature of Al and Si a rectifying contact were not produced. This would appear to be due to the fact that an uniform epitaxial layer was not produced as evidenced by Figure 4.3. Even if this epitaxial layer had been uniform, the extent of dissolution of Si in Al appears to have been insufficient to allow for production of a sufficiently thick epitaxial

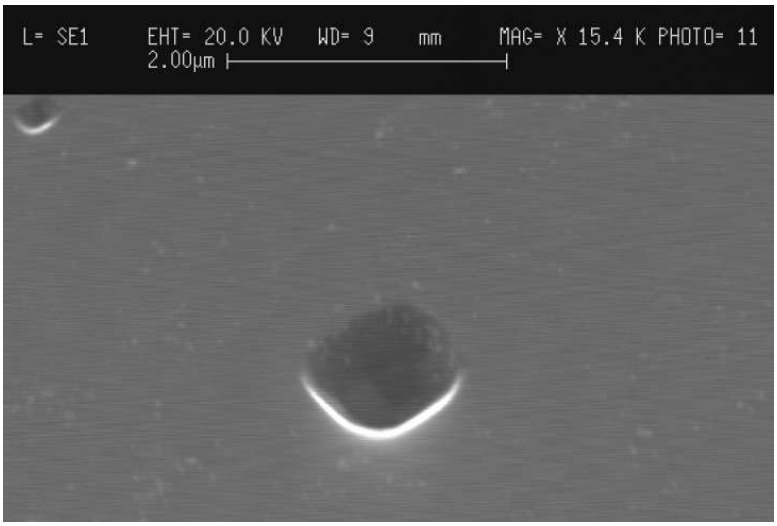


Figure 4.8: Close up SEM image (in secondary electron mode) of a Al spike/pit on a sample with 0.3 μm Al dots sintered at 400 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed.

layer.

4.3 Conventional Furnace Sintering Above the Eutectic Temperature

4.3.1 Effect of Aluminium Thickness on 3N Aluminium

Samples with 3N Al thicknesses of 0.3 μm and 1.0 μm were sintered at 600 °C for 30 minutes. Figure 4.9 shows the resulting SEM image obtained in secondary electron mode for the sample which had 0.3 μm Al on it. This was in stark contrast to the SEM image obtained for a sample which had 1.0 μm thick Al dots deposited on it(Figure 4.10).

1.0 μm thick Al dots

Figure 4.10 illustrates, via an SEM image in electron backscattering mode, the extensive pitting that occurred for samples with 1.0 μm. Figures 4.11 and 4.12 show the aluminium and silicon profiles through the same central horizontal strips from Figure 4.10. In the images that are profiles of Al and Si the element that is being profiled shows up as a lighter colour in the wds mode. Thus it can be seen that the pits contained a large amount of Al and less Si, while the surrounding areas contained less Al and more Si. This is indicative

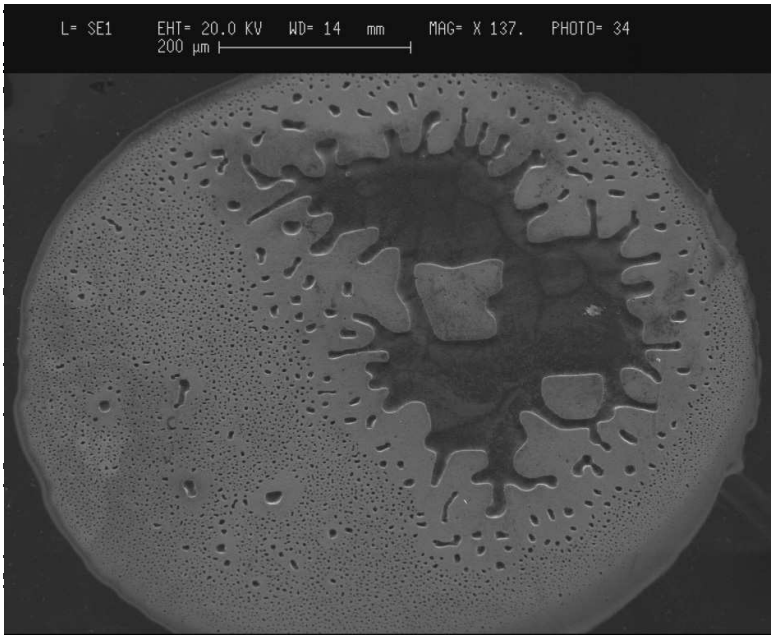


Figure 4.9: SEM image (in secondary electron mode) of a single Al dot on a sample with 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed.

of epitaxial regrowth within the spikes, with very limited or no epitaxial regrowth outside of these pits/spikes.

Figure 4.13 illustrates the effective resistances obtained for samples sintered above the eutectic temperature. Data points represented by solid points are those that were taken from samples which had 1.0 μm Al dots. These are also indicated by a '1' following the 'E' in the label. It can be seen that most of these gave resistances of less than 200 Ω. The sample which gave resistances of 700 Ω to 1000 Ω (#8E18) was sintered at 650 °C for 30 minutes after being brought to 650 °C from room temperature in 14 minutes, was cooled to room temperature in 60 seconds. This higher temperature may have been the reason why the resistance was so large for this sample when compared to the other samples which had 1.0 μm Al on them. However, #8E17, which was also sintered under the same conditions with the only difference being that it was cooled for about 2 hours to room temperature, shows resistances of less than 200 Ω. Thus the high resistance obtained by #8E18 may have been due to the combination of the high temperature sinter and the rapid cooling of the sample. The importance of the higher temperature agrees with the theory in that more Si could dissolve in the Al and thus a thicker epitaxial layer could grow with resulting higher resistances.

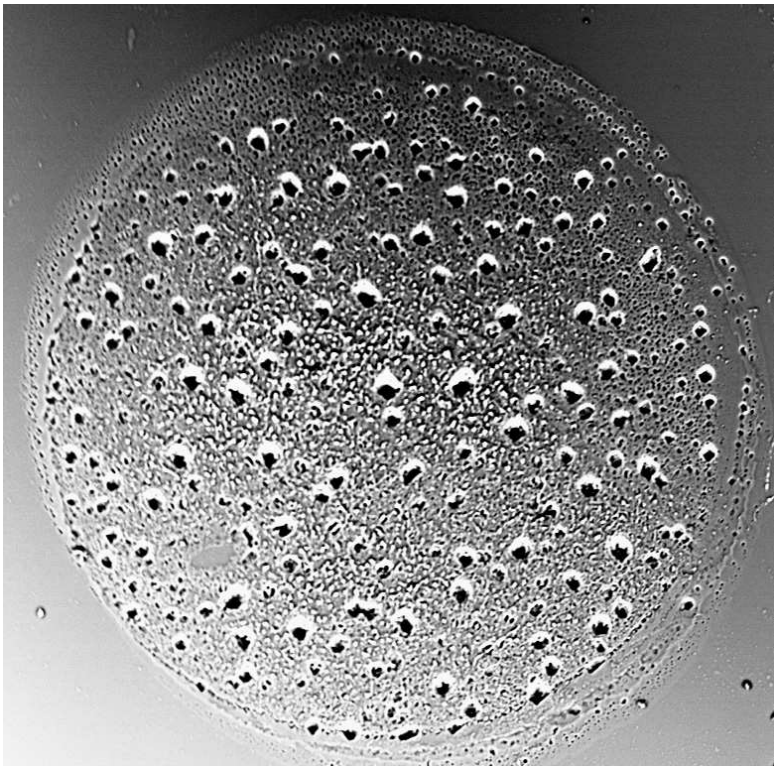


Figure 4.10: SEM image (in electron backscattering mode) of a sample which had 1.0 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

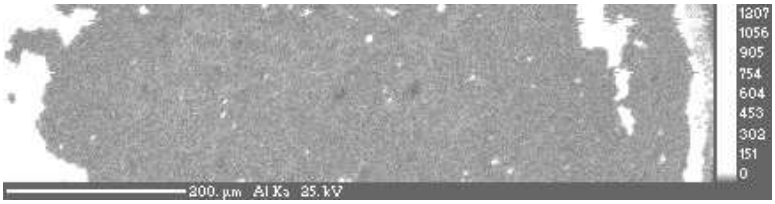


Figure 4.11: SEM cross section profile (in wds mode) of Al in a sample which had 1.0 μm 3N Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

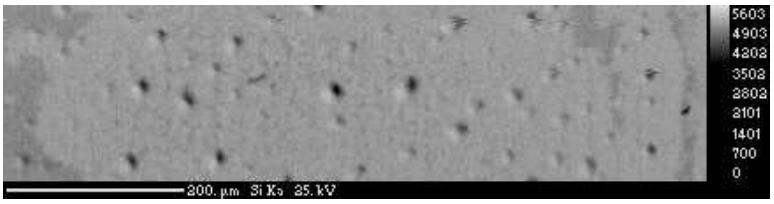


Figure 4.12: SEM cross section profile (in wds mode) of Si in a sample which had 1.0 μm 3N Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

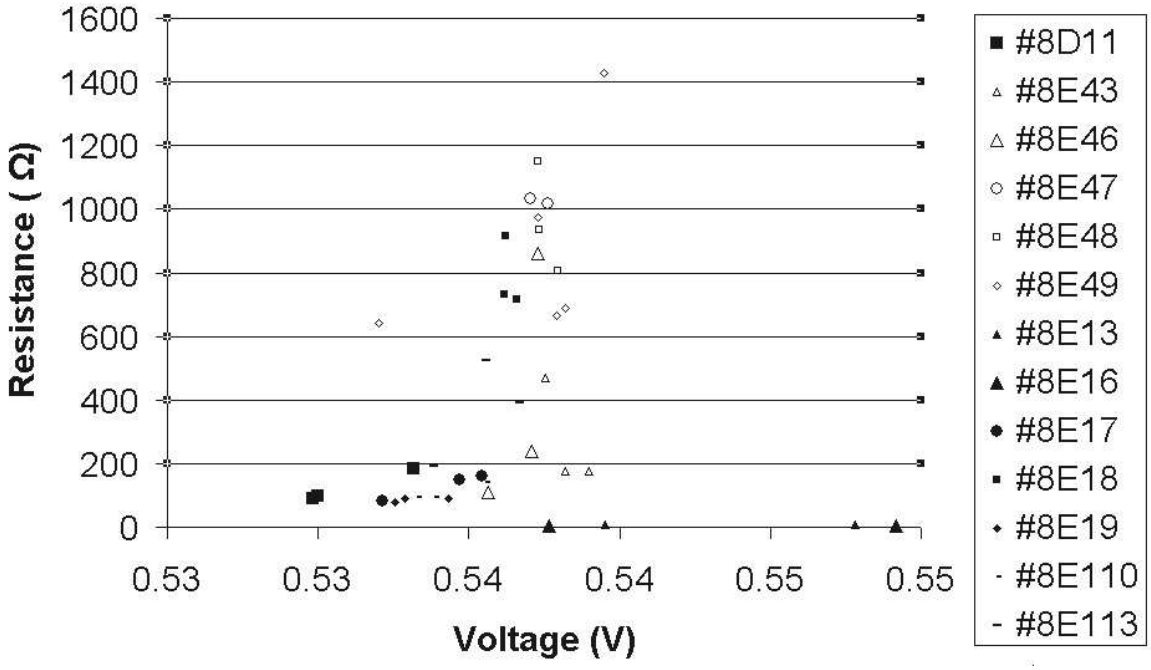


Figure 4.13: Samples sintered above the eutectic temperature in a conventional furnace. Hollow points represent samples which had 0.3 μm Al dots while the rest had 1.0 μm Al dots.

0.3 μm thick Al dots

Figure 4.9 shows what appears to be a dark pool in the top right quarter of the dot. Figures 4.14 and 4.15 show close up views of this pooling effect. All of these SEMs were taken from a sample which was heated at 600 °C for 30 minutes and cooled rapidly. From Figure 4.14, and the fact that it was taken at 60°, the depth of this pool/hole can be calculated to be 1.5 μm deep. Figure 4.15 illustrates the smoothness of the surface in the pool. Figure 4.16 shows an SEM image taken in electron backscattering mode which illustrates that the pooled substance was indeed Al. This can be clearly seen in that the area which is not pooled is nearly the same as the areas in the picture that are clearly not part of the dot (plain Si).

Figure 4.17 illustrates what the edge of the pooled areas looked like before the Al was removed. From this figure it appears that the Al was about the same height as the surrounding Si after the sample was cooled.

As was confirmed by the Temcor Alpha Step 200 surface profiler, the dots which were measured to be 0.3 μm thick by the Inficon XMS-1 controller were indeed that thickness.

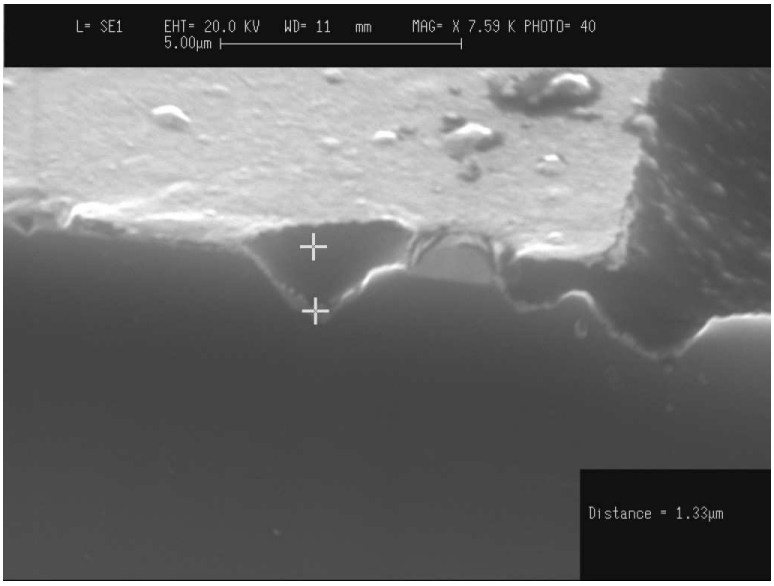


Figure 4.14: SEM image (in secondary electron mode) of a sample that had 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 60°.

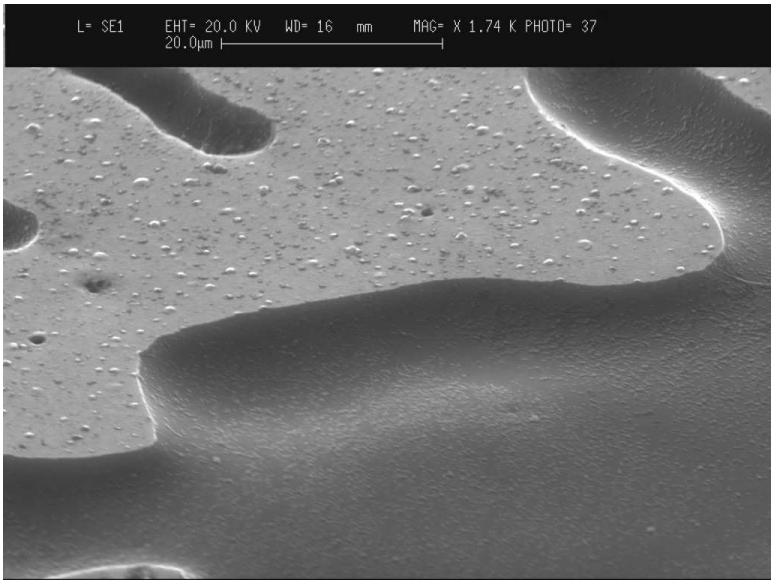


Figure 4.15: SEM image (in secondary electron mode) at the edge of a pool in a sample which had 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed.

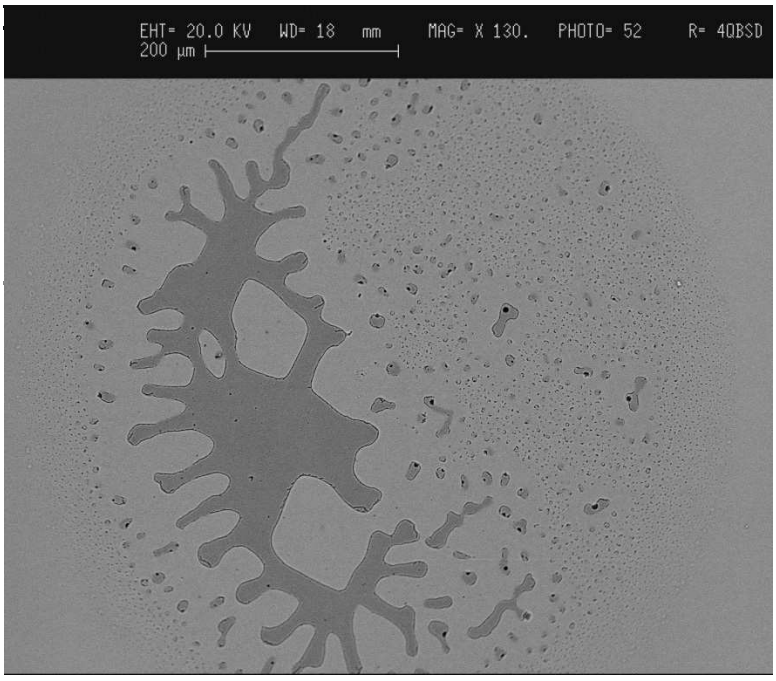


Figure 4.16: SEM image (in electron backscattering mode) of a sample which has 1.0 μm 3N Al dots sintered in a conventional furnace. Sintered for 30 minutes at 600 °C and cooled in about 40 minutes. The Al has been removed. This image was taken at an angle of 0°.

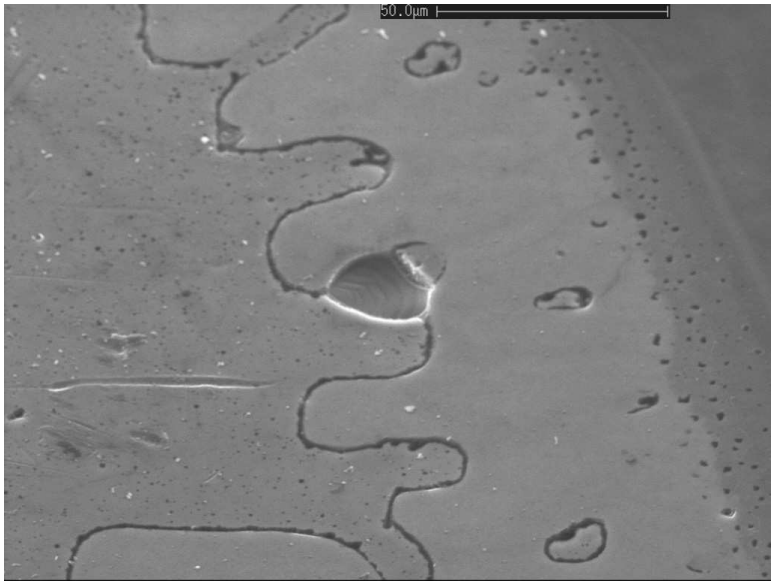


Figure 4.17: SEM image (in secondary electron mode) of a sample which has 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The aluminium is still on the sample.

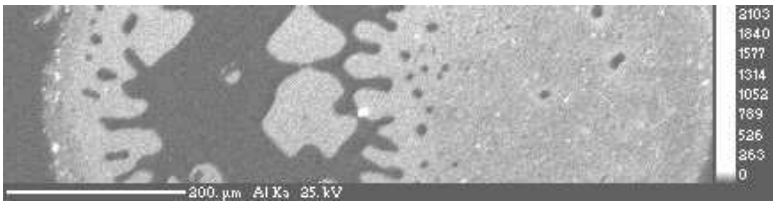


Figure 4.18: SEM cross section profile (in wds mode) of Al in a sample which had 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

The surface profiler was also used to measure the surface profile of a sample that had been sintered at 600 °C for 30 minutes and cooled rapidly from which the Al had subsequently been removed on it. This resulted in a profile that showed the dot as being approximately 0.1 μm high in the non-pooled areas and 0.3 μm high in the pooled areas. On the inside edge of the pool the depth fell of very quickly and on the outside edge of the pool rose to about 1.4 μm. The depth at the edge of the pool could not be measured accurately as it appeared to be a very narrow canyon-like feature. All of this suggests that the Al, which was originally covering the entire dot in a uniform layer, was saturated with Si from the 'pooled' areas. This implies that the 'native' oxide was partially or completely removed in the pooled regions, but that it probably remained in the non-pooled regions. The surface profile in combination with the SEMs in Figures 4.18, 4.19 and 4.20 also suggest that the epilayer outside of the pooled areas was approximately 0.1 μm thick while inside the pooled areas it was about 0.3 μm thick.

Figure 4.18 shows the Al profile of a dot from the sample, while Figure 4.19 shows the same region profiled for Si and Figure 4.20 shows an SEM image in backscattering mode of the whole dot from which the previous two images were taken. Figures 4.18 and 4.19 show areas containing higher percentages of the profiled substance as lighter and indicate that, indeed, the pooled areas appear to be nearly 100% Si while the non-pooled areas had higher concentrations of Al: indicative of Al doped Si due to epitaxial regrowth.

From this it would appear that there was a dynamic process operating during the sinter that resulted in these pools. The Al may not merely have dissolved the Si until it was saturated, and then regrown the Si in an epitaxial layer when cooled. Rather, Si appears to have been dissolved, throughout the 600 ° sinter, from the pooled areas and redeposited in the non-pooled areas starting at the periphery of the dots. This mechanism of dissolution

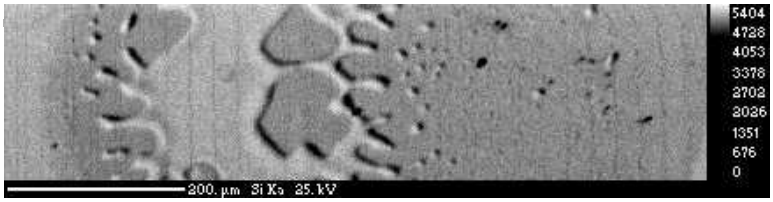


Figure 4.19: SEM cross section profile (in wds mode) of Si in a sample which had 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

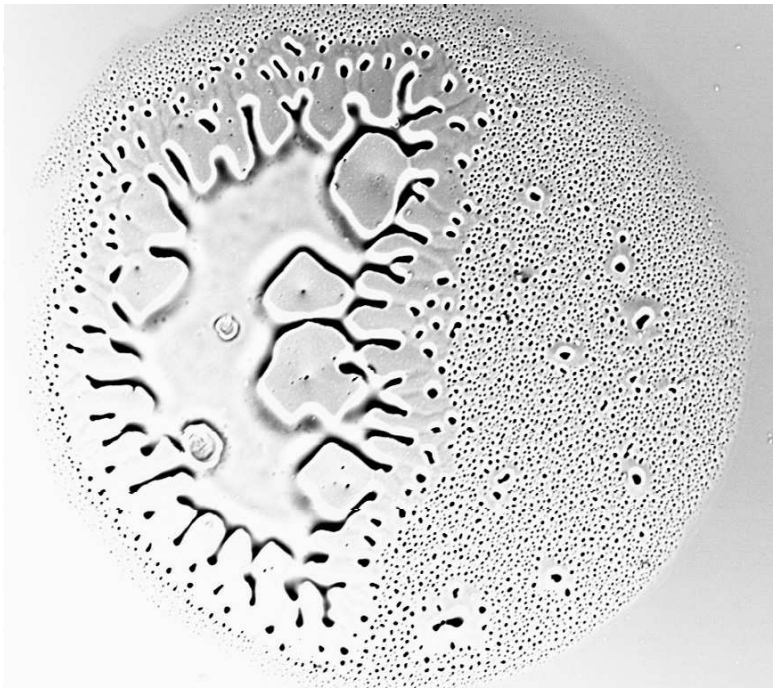


Figure 4.20: SEM image (in backscattered electron mode) of a sample which had 0.3 μm Al dots sintered at 600 °C for 30 minutes and cooled to room temperature within 30 seconds. The Al has been removed. This image was taken at an angle of 0°.

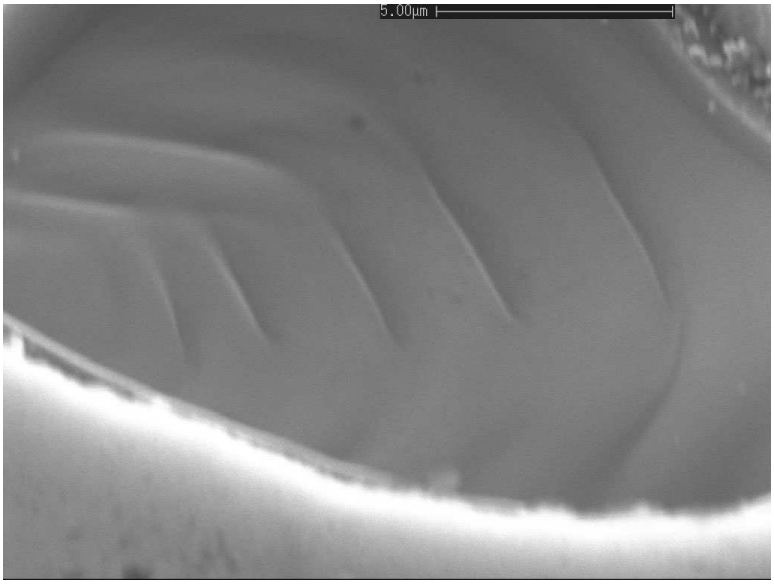


Figure 4.21: Expanded view of Figure 4.17.

in one place while there is simultaneous growth in other regions would require a driving force. The most obvious driving force would be a temperature gradient arising within the sample. The areas where Al is dissolved (in the pooled areas) may have been hotter than the areas around the dot periphery. Thus the hotter regions of Al would have a higher Si solubility, resulting in a Si concentration gradient within the Al. This would have resulted in the continuous diffusion of Si away from the etched areas towards the cooler areas at the periphery where the Si would crystallize out. Due to the very high diffusivity of Si in Al, even a modest temperature gradient could have been sufficient to result in the observed topography of the sample. A possible reason for the temperature gradient is that it was due to differences in the blackbody characteristics of the Si and Al, leading to the Al dots being hotter than the surrounding Si and thus the regions near the edge of the Al dot would be cooler than those near the centre. This agrees with the observation that most of the Al pools were never located at the edge of a dot, but always had a bounding region completely around them.

As can be seen in the centre of Figure 4.21 and more graphically in Figure 4.22, there appeared to have been holes through the Al after the sinter. These will be discussed in the section dealing with the effect of thickness on samples that used 5N Al.

Therefore, one possible explanation for the pooling observed and the smooth epitaxial growth is that:

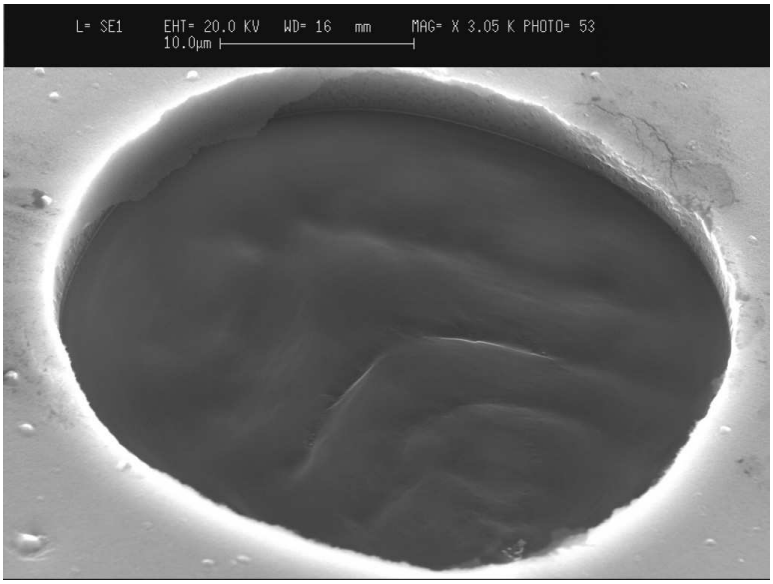


Figure 4.22: SEM image (in secondary electron mode) of a sample which has 0.3 μm Al dots sintered at 600 °C for 5 minutes and cooled to room temperature within 30 seconds. The Al has been not been removed.

- The sample was first heated to 600 °C in 15 minutes with minimal activity due to the lower temperature state and shortness of the time.
- Following this, oxide in the central regions of the dot was removed more quickly than at the periphery.
- Si started to dissolve in these central regions where there was no oxide and saturation of the Al with Si occurred wholly from these regions.
- Once saturation was achieved, Si began to precipitate out of the Al at the edges of the dot in regions where the oxide has also been removed (albeit maybe only pinholes through the oxide) to initiate the growth of an epitaxial layer of Si.
- The epitaxial layer may then have grown laterally from the periphery of the Al dot. This would have allowed smooth epitaxial growth even if the interfacial oxide had not been removed in these areas. As the epitaxial layer was growing laterally, the Al would be pushed back, gradually retreating into the pooled areas depositing epitaxial Si as it retreated.
- The process would stop or slow dramatically when the Al became confined into the final pooled areas of the dot as the Al had hemmed itself in by epitaxial silicon and thus had nowhere to retreat to. This would explain why the surface profiler indicated

a high region around the pool. This high region could have been due to the slowing retreat of the Al and thus the thicker deposition of laterally grown epitaxial silicon.

This hypothesis explains most of the observed features well, including the relative smoothness of the epitaxial layer. Such smooth epitaxial layers are difficult to obtain unless the interfacial oxide has been completely removed. However, in the case of epitaxial lateral overgrowth, such complete oxide removal is not necessary for smooth epitaxial growth.

Figure 4.13 shows indications that the effective resistances of the samples that were sintered above the eutectic temperature and had 0.3 μm thick dots of 3N Al were higher than those which had 1.0 μm. Indeed, most of the effective resistances were in the range of 800 Ω to 1100 Ω compared to those with 1.0 μm which were in the range of 50 Ω to 200 Ω. If the area of the contact of a pooled sample is assumed to be one quarter of the total area of the original dot then the resistivity of a sample which measured 1000 Ω would be 1000 x πr^2 / 4 = 0.96 Ω-cm^2. Assuming the voltage across the sample was 0.54 V, this would be the result of (using Equation 2.10) a current density, J_0, of 5.26 x 10^{-10} A cm^{-2}. This current density would be due to a uniform epitaxial layer thickness of 4.57 nm according to Equation 2.9. Figure 4.23 shows the effective resistances of the dots of a sample that had 0.3 μm thick dots of 3N Al sintered at 600 °C for 30 minutes and cooled to room temperature in 30 seconds. This indicates that most of the resistances obtained, even for this sample which exhibited pooling, were in the range of 100 Ω to 500 Ω rather than 1000 Ω as the epitaxial layer thickness was calculated for earlier. Thus the necessary theoretical epitaxial thickness required to get these results would actually be in the range of 0.5 nm to 2.2 nm (assuming that the area which actually made contact was one quarter of the dots area).

Figure 4.24 shows a typical IV curve of a dot from a sample that had 0.3 μm thick 3N Al dots that were sintered at 600 °C for 30 minutes and cooled to room temperature in 30 seconds. As can be seen this particular sample appeared to show good rectifying properties with small currents flowing until a voltage of about 0.6 V is reached at which stage the current begins to increase more rapidly. It can also be seen that the slope of the line, toward the right hand side of the figure, where the current flow is high is quite high. This bodes well for forming good ohmic contacts to the p^+ type substrate as the

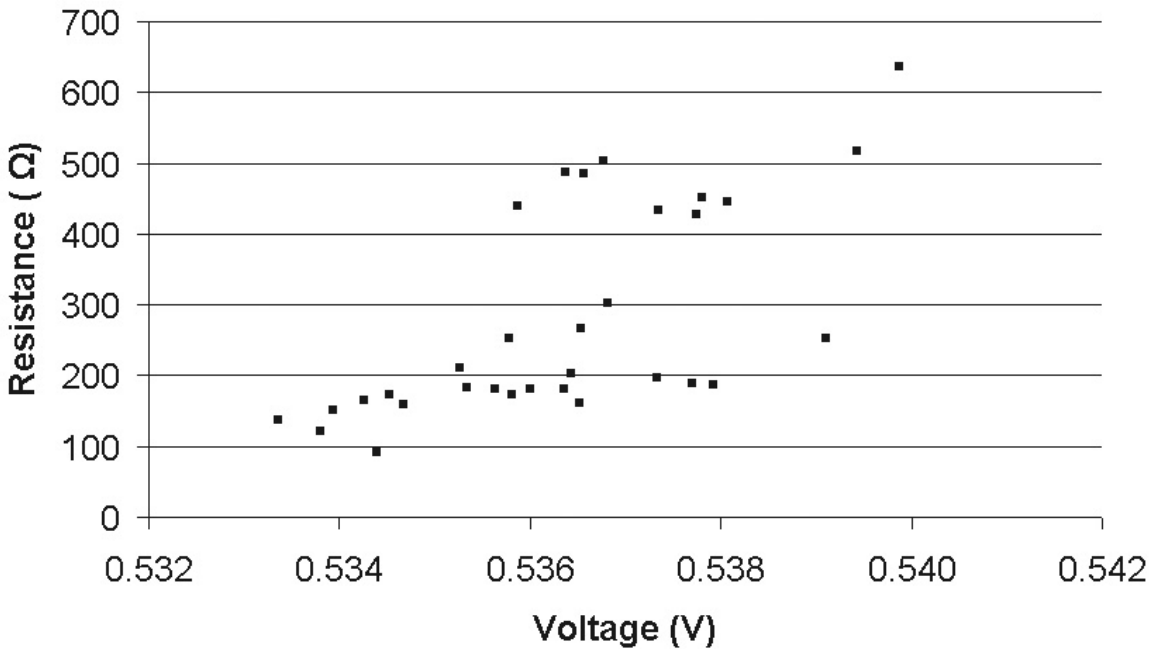


Figure 4.23: Resistances of a sample that had 0.3 μm 3N Al deposited and was sintered at 600 °C for 30 minutes and cooled within 30 seconds.

high slope of this line indicates that the series resistance that would result from such a contact would be quite low.

Figures 4.18, 4.19 and 4.20 show three images of the same sample that was sintered at 600 °C for 30 minutes and cooled to room temperature in 30 seconds. The first one is a profile of Al, the second of Si and the third is an SEM image taken in backscattering mode at 0°. It can be seen from these images that:

- The pooling of the Al occurred over areas that, in the end had very little epitaxial silicon on them. This is indicated by the darkness of Figure 4.18 in the pooled region.
- The areas in which the Al was not pooled showed higher concentrations of Al. This is indicative of strong epitaxial regrowth in these areas.
- Figure 4.19 confirms this explanation as it shows that the profile of the Si was inversely related to the Al throughout.

It should be noted that the WDS signal from the areas where Al was detected was quite small, and the Al detected was quite close to the sensitivity limit of the device. Thus, a possible explanation of these results is that a much thinner epitaxial layer, grown during

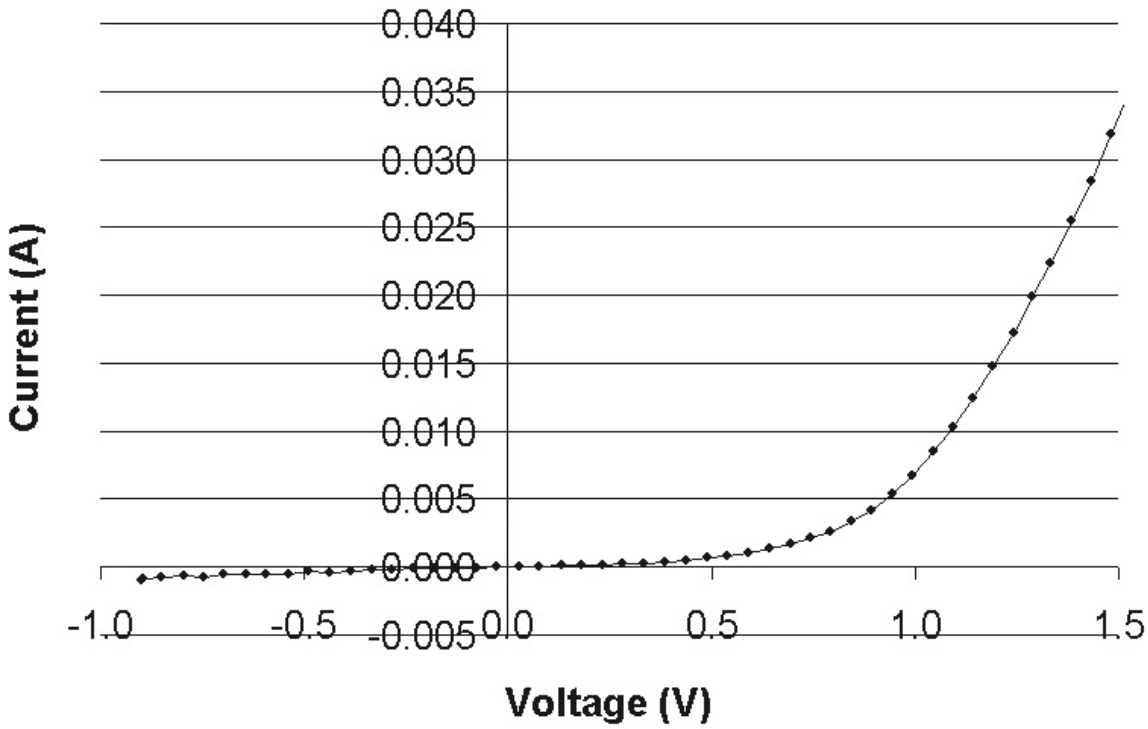


Figure 4.24: Typical current/voltage characteristics of a dots from a sample that had 0.3 μm thick 3N Al dots that were sintered at 600 °C for 30 minutes and cooled to room temperature in 30 seconds.

the cooling of the sample, did in fact exist in the etched areas, but that this layer was too thin to be detected. Since it is the thickness of the epitaxial layer between the Al and the Si that determines the IV characteristics, it would have been this very thin epitaxial layer that was the reason for the resulting diode-like IV curves. As calculated from theory earlier, this epitaxial layer would have needed to be between 0.5 nm and 2.2 nm thick. This thickness of Al doped Si would have been very difficult, if not impossible, to observe using WDS.

It should be noted that while the formation of the pool the Al would have dissolved large amounts of Si, it would also have dissolved the other dopants in the Si. These include Sb and P. However, it is unlikely that these impurities would have had a significant impact on the contact, as their concentrations in the Al would have been well below the concentrations of Al and Si, and the concentrations of these impurities that would have been incorporated back into the epilayer are likely to have been at least 2 orders of magnitude lower than those of the Al.

4.3.2 Effect of Aluminium Thickness on 5N Aluminium

In order to observe the effect of thickness on the contacts which utilized 5N Al, samples with 0.2 μm, 0.3 μm and 0.5 μm thick dots of 5N Al were formed and the samples sintered at 600 °C for 0 minutes, 5 minutes and 30 minutes and cooled rapidly. Figure 4.25 is indicative of what these samples looked like after sintering but before the Al was etched. It can be seen that the Al appeared to be evenly spread over the whole dot with some smaller black dots contained within it. These black dots were then examined further as shown in Figure 4.26, 4.27, and 4.28. Figure 4.26 illustrates one of these black dots that appears somewhat like a volcano. It can also be seen that there appears to be a tear around most of the base of this 'volcano'. This could have been caused by a gas, presumably H_2 or Ar, trapped under the aluminium oxide on the surface of the Al during cooling of the samples. It is known [17] that aluminium oxide is relatively impervious to H_2 and thus it would be reasonable to assume that it was H_2 gas that was trapped under the aluminium oxide layer. Aluminium is also known to dissolve hydrogen in only very small quantities, about 1 PPM at atmospheric pressure near the melting point [8]. It could be assumed that this quantity would increase when the Al melts and thus the molten Al could absorb hydrogen during the sinter during which the oxide layer would not exist (at least in a rigid state since the Al/Si alloy is molten) and, upon cooling, the gas would then gather under the oxide layer, which would form quite rapidly during cooling, and cause these 'volcanoes'. Figure 4.28 illustrates the oxide layer, seen on the left hand side, the hole/bubble and some spikes within the hole.

As can be seen, the SEM images of samples that had 5N Al dots are quite different from the samples that had 3N Al dots. This difference would appear to have been due to one or more of the impurities contained in the 3N Al that was not contained (at least in the same magnitude) in the 5N Al. The manual that provided the specifications for the impurities of the Al did not provide specifications for 3N Al. However, it did state Ca was the dominant impurity in 5N Al at up to 65 ppm. Therefore, it could be concluded that in 3N Al it is likely that the Ca level was significantly higher than this and once again the largest factor in the impurities. Ca is a well known reducing agent and thus would increase the speed with which a 'native' oxide would be reduced and thus result in a smoother interface

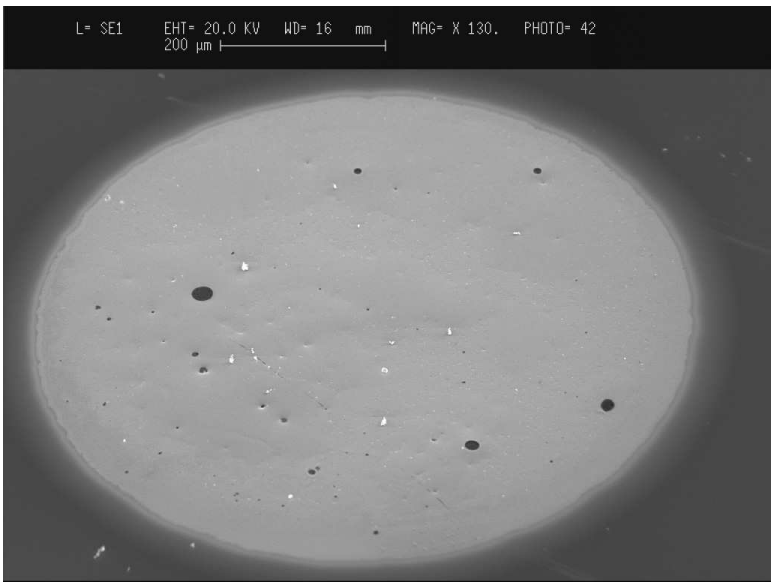


Figure 4.25: SEM image (in secondary electron mode) of a sample which has 0.3 μm 5N Al dots sintered using RTA. 3 second ramp to 600 °C , 60 second at 600 °C and cooled rapidly. The Al has not been removed.

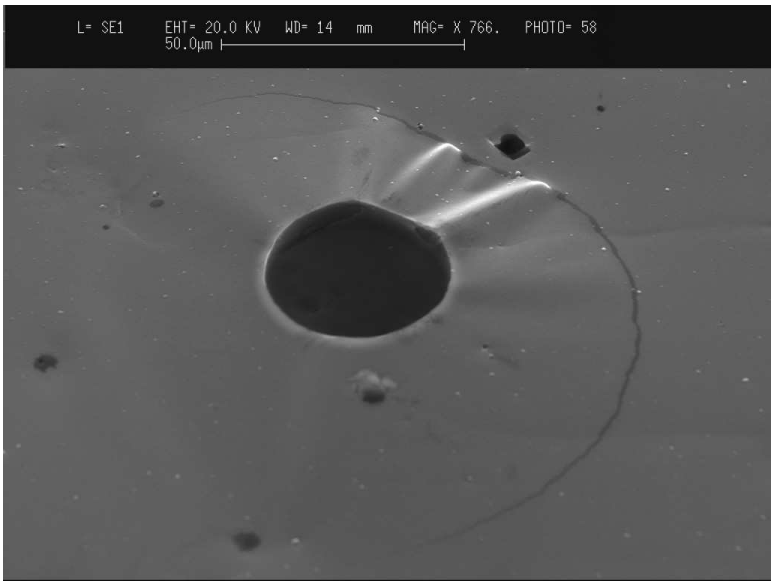


Figure 4.26: SEM image (in secondary electron mode) of a sample which has 0.3 μm 5N Al dots sintered in a conventional furnace. Sintered for 5 minutes at 600 °C with 15 minutes ramp up and cooled in 30 seconds. The Al has not been removed.

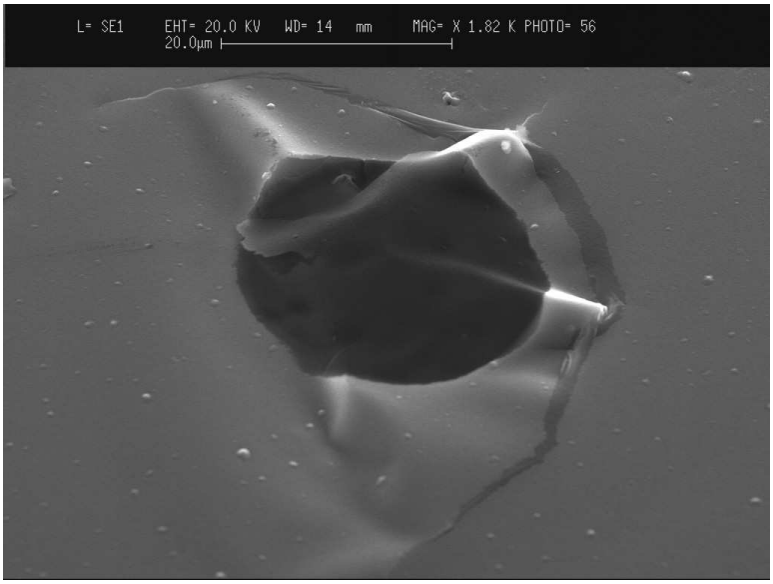


Figure 4.27: SEM image (in secondary electron mode) of a sample which has 0.3 μm 5N Al dots sintered in a conventional furnace. Sintered for 5 minutes at 600 °C with 15 minutes ramp up and cooled in 30 seconds. The Al has not been removed.

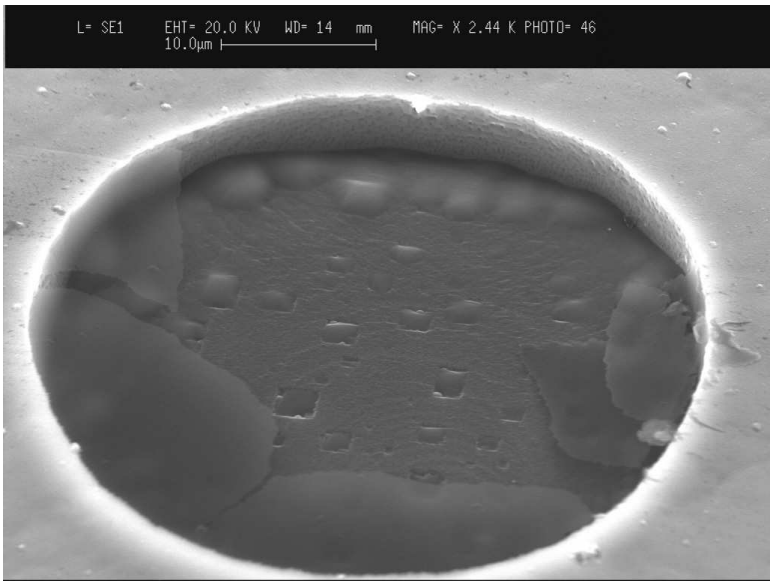


Figure 4.28: SEM image (in secondary electron mode) of a sample which has 0.3 μm 3N Al dots sintered in a conventional furnace. Sintered for 0 minutes at 600 °C with 12 minutes ramp up and cooled in 30 seconds. The Al has not been removed.

between the Al and Si.

It was found that there was usually one 'volcano' per Al pool and that there was a direct relationship between the size of a hole and the size of the pool surrounding it (in the samples with 3N Al). This agrees with the above explanation in that, if the Al pooled more greatly, the gas that gathered in these 'volcanoes' would have had less distance to travel and thus a greater probability gathering into one large 'volcano' rather than more smaller ones.

Figure 4.13 shows the one sample with 1.0 μm 5N Al dots whose IV characteristics were tested (#8D11). It can be seen that its operating resistance would be less than 200 Ω.

4.3.3 Effect of Cooling Rate

The rate at which the samples were cooled appeared to have little affect on the topography of the contact. Figure 4.16 shows that pooling occurred even when the sample was cooled slowly (Compare this to Figure 4.9). It should be noted that Figure 4.16 was taken at an angle of 0° under electron backscattering mode, while Figure 4.9 was taken at an angle of 45° in secondary electron mode.

The IV characteristics of these curves were, however, different. Those of the samples which were cooled rapidly after sintering above the eutectic temperature of Al and Si appeared similar to Figure 4.13. However the voltage at which the current began to increase more rapidly was about 0.5 V rather than the 0.6 V displayed in this figure. The samples which were cooled rapidly after sintering above the eutectic temperature of Al and Si appeared similar to Figure 4.13 in all respects. Indeed, this figure is derived from one of those samples. One possible explanation of these different IV characteristics is that while there is substantial dissolution of Si, the Si surface remains free of aluminium oxide. However, when dissolution of Si ceases an aluminium oxide layer forms at the interface of the Al and Si. In the case of the rapidly cooled samples, the opportunity for oxide growth before the sample had cooled and the Si recrystallized (either as epitaxial silicon or crystallites within the Al) was minimized, whereas in the case of the slow cooled sample, a partial oxide may have regrown, resulting in a loss of uniformity of the epitaxial layer produced.

4.3.4 Effect of the Ambient Gas

In order to examine the effect, if any, of the ambient gas in the sinter furnace on the topography of the samples, the gas which was originally forming gas (95% Ar, 5% H_2) flowing at 160 L/hour was changed to 100% N_2 flowing at 160 L/hour. The sinter was performed at 600 °C for 30 minutes and the resulting SEMs were different to those resulting from sinters performed under forming gas. Unlike the sinter performed under forming gas, sintering under nitrogen flow resulted in extensive spiking and extremely limited pooling. This indicates that the ambient gas has an effect on the resulting contact topography. It is possible that the H_2 in the forming gas, which is an excellent reducing agent, diffuses through the molten Al, dissolving any remaining native oxide, thus reducing the amount of spiking evident on these samples. Ar and N_2 are largely inert gases and would not be expected to have much effect on the samples during the sintering. From this it can be inferred that the gas under which the sinter takes place is of vital importance to the outcome of the electrical properties of the contacts being formed.

4.4 Effect of Heating Rate in Rapid Thermal Anneals

Attempts were made to reproduce the results obtained from the sinter furnace in Rapid Thermal Anneals (RTAs) using an ADDAX AET RX Series RTA. There were however limitations on the RTA that did not allow for complete replication of conditions. These included that the forming gas used contained N_2 instead of Ar and that the total time allowed for any one sinter was limited to 15 minutes. Reasons for utilizing RTA were that:

- It allowed the samples to be loaded into the furnace at room temperature (rather than about 400° for the conventional furnace).
- The furnace could be flushed thoroughly with an inert gas (N_2) prior to heating. This may help to minimize sample oxidation, which, for the standard furnace treatment, could be particularly pronounced because, as the sample was loaded, some air will inevitably be introduced into the furnace.
- RTA allows investigation of the effect of different heating/cooling regimes. This may

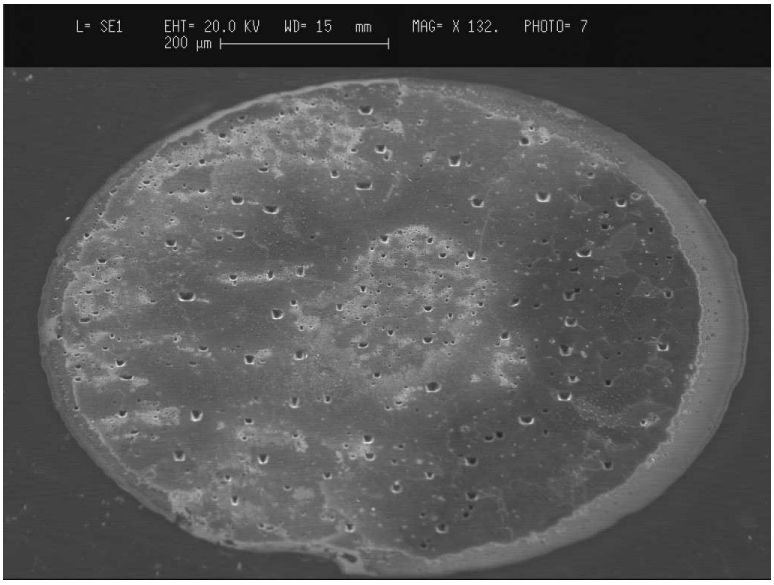


Figure 4.29: SEM image (in secondary electron mode) of a sample which has 0.3 μm 5N Al dots sintered in RTA. Sintered for 5 minutes at 600 °C after ramping to 550 °C in 6 seconds followed by ramp to 600 °C in 600 seconds and then cooled rapidly. The Al has been removed.

have allowed more information about the process of pooling to be gained.

The effect of the rate at which the temperature was increased over the eutectic temperature was observed using RTAs. Samples rapidly heated to 550 °C. They were then heated from 550 °C to 600 °C over times ranging from 5 seconds to 15 minutes. However, due to the limitations of the machine mentioned above, samples could not be left to sinter for 30 minutes after each ramp up as the total time was limited to 15 minutes.

Effect on 5N Al

Figure 4.29 shows what generally happened over all these sinters for samples which used aluminium of purity 5N. As was the case for the conventional samples this did not exhibit any significant pooling.

Effect on 3N Al

Figure 4.30 shows a dot from a sample that was ramped from room temperature to 550 °C in 6 seconds followed by a ramp to 600 °C in 300 seconds followed by a 600 second anneal at this temperature. The sample was then cooled rapidly. It can be seen from this figure

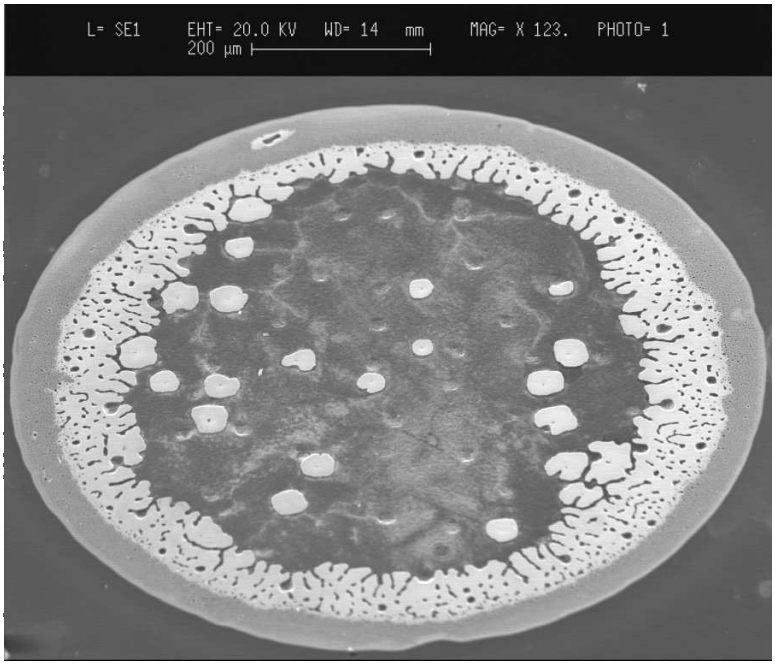


Figure 4.30: SEM image (in secondary electron mode) of a sample which has 0.3 μm 3N Al dots sintered in RTA. Sintered for 600 seconds at 600 °C after ramping to 550 °C in 120 seconds followed by ramp to 600 °C in 300 seconds and then cooled rapidly after sintering. The Al has been removed.

that pooling of samples with 3N Al did occur although not to the same extent as in the conventional furnace. It also shows that the pool tends to form from the edge of the dot. This would indicate that, as explained earlier, silicon is dissolved from the centre and deposited at the edge of the aluminium during the sinter. The samples containing 3N Al that were ramped up from 550 °C to 600 °C over periods of time longer than 300 seconds (at least up to 15 minutes) appeared similar to that in Figure 4.29. This may have been due to the fact that the sample spent insufficient time at temperatures above the eutectic temperature to allow sufficient lateral epitaxial growth to occur.

Figure 4.31 indicates that spiking did occur in this sample even within the pool. However, the degree of spiking appears to be small. It can be seen that the holes within the pool have what appear to be little miniature spikes around the edge of the holes. It is uncertain as to what affect these miniature spikes have, if any, on the formation of these holes or vice-versa, and on the smoothness of the pooled area.

In conclusion, minimal pooling was observed in both 3N and 5N samples, with the pooling in 3N samples occurring when the sample was sintered above the eutectic temperature for

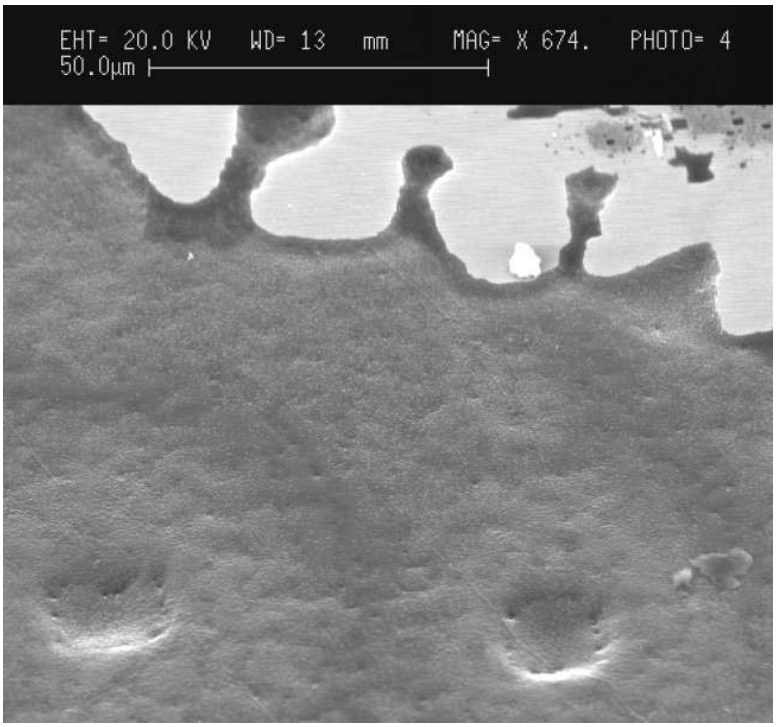


Figure 4.31: SEM image (in secondary electron mode) of a sample which has 0.3 μm 3N Al dots sintered in RTA. Sintered for 600 seconds at 600 °C after ramping to 550 °C in 120 seconds followed by ramp to 600 °C in 300 seconds and then cooled rapidly after sintering. The Al has been removed.

longer times (and having correspondingly shorter ramp up times) and the pooling in the 5N samples occurring, to a lesser degree, when the samples were ramped up more slowly to temperatures above the eutectic temperature (and having correspondingly shorter sinter times). IV measurements on these samples were not carried out. It would be expected, however, that those samples exhibiting smoother surfaces would have more rectifying properties than those which did not.

4.5 Conclusions and Suggestions for Further Research

Throughout this project it was found that most research that had been done in Al contacts to Si was for the purpose of creating ohmic contacts. In this respect the research carried out was original in that the aim was to form a rectifying contact to n-type Si while still forming a good quality ohmic contact with p^+ doped Si. It was found that good rectifying contacts could be produced by deposition of 0.3 μm of 3N Al in dots of diameter 0.7 mm, sintering these at 600 °C for 30 minutes and cooling them rapidly (within 30 seconds) to

room temperature. It was found that this resulted in the pooling of Al and the formation of a smooth surface within the pool with a very thin Al-doped epitaxial layer and a thick Al-doped epitaxial layer outside the pooled areas. Although contact resistances of these contact was not performed when they were made to p^+ type Si, the IV curves of the samples that had contacts to Al indicated that the contact to p^+ type Si would be a low resistivity ohmic contact.

While good rectifying contacts were found, there were problems with reliability and repeatability of the data as indicated by the large spreads in figures displaying the effective resistances. Also, dissolution of large amounts of Si is undesirable in contact formation to PV cells as it dissolves not only the Si, but also the dopants in the underlying diffusion. This can result in the destruction of the p^+ region and the PV cell no longer having the correct diffusion profiles to produce electron/hole pairs to any large, worthwhile extent.

More research needs to be done to understand completely the formation of these pools and how it results in a rectifying contact being produced. This could involve sintering samples, which are the same as those that resulted in pooling, under the same sintering conditions except for the period of time spent sintering. This would hopefully give insight into the progression of the formation of these pools. Formation of Al contacts containing higher quantities of Ca, either within the Al or as a separate layer, could also be performed to observe if the Ca level was a determining factor in the differences observed between the 3N Al contacts and the 5N Al contact.

An alternative to forming good rectifying, uniform contacts could be to deliberately form only localized contacts through the interfacial oxide. This would result in the familiar 'spikes' in the silicon substrate during the annealing. If it were possible to determine a set of processing conditions under which these spikes were almost completely refilled with p-type, Al doped, epitaxial silicon, then, at least in principle, excellent rectifying contacts should be able to be obtained. Utilizing this technique would allow the sintering temperatures to be kept below the Al-Si eutectic temperature as the area over which the Si would be dissolved and deposited would be quite small in comparison to the contact as a whole (as compared to the sum of the localized contact areas). The area of the localized contacts could be controlled by varying the interfacial oxide thickness as well as

the annealing temperatures and times.

Bibliography

[1] Andrew Blakers, Andres Cuevas, and Klaus Weber. *Solar Cells - Physics, Technology and Characterization*, chapter 4-38. Australian National University, July 2003.

[2] H. C. Card. Thermally-induced changes in barrier heights of aluminium contacts to p-type and n-type silicon. *Solid State Communications*, 16(1):87–89, September 1975.

[3] UNSW Centre for Photovoltaic Engineering˙ Pc1d. http://www.pv.unsw.edu.au/Links/pc1d.asp.

[4] S. S. Cohen, G. Gildenblat, M. Ghezzo, and D. M. Brown. Al-0.9%Si/Si ohmic contacts to shallow junctions. *Journal of the Electrochemical Society: SOLID-STATE SCIENCE AND TECHNOLOGY*, 129(6):1335–1338, June 1982.

[5] T. J. Faith, R. S. Irven, S. K. Plante, and Jr. J. J. O'Neill. Contact resistance: Al and Al-Si to diffused N^+ and P^+ silicon. *J. Vac. Sci Technology*, 1(2):443–448, April-June 1983.

[6] M. Finetti, P. Ostoja, S. Solmi, and G. Soncini. Aluminum-silicon ohmic contact on "shallow" n^+/p junction. *Solid-State Electronics*, 23:255–262, 1980.

[7] Tohru Hara, Hidenori Suzuki, Masakazu Furukawa, and Kimio Amemiya. Contact resistance of Al/Si ohmic electrodes formed by rapid lamp sintering. *Japanese Journal of Applied Physics*, 22(6):L340–L342, June 1983.

[8] E. Hashimoto and T. Kino. Hydrogen diffusion in aluminium at high temperatures. *J. Phys. F: Met. Phys.*, 13:1157–1165, January 1983. Published by The Institute of Physics.

[9] Anita Wing Yi Ho and Stuart R. Wenham. Buried contact solar cells with innovative rear localised contacts. *Progress in Photovoltaics: Research & Applications*, 12(4):297–308, June 2004.

[10] Minoru Kaneiwa and Katsuhiko Nomoto. Manufacturing technology for terrestrial PV systems: High efficiency crystalline Si through amorphous Si. *PROGRESS IN PHOTOVOLTAICS: RESEARCH AND APPLICATIONS*, 10:77–84, January 2002.

[11] James W. Mayer and S. S. Lau. *Electronic Materials Science: For Integrated Circuits in Si and GaAs.* Macmillan Publishing Company, 866 Third Avenue New York New York, 1990. P. 281, 282.

[12] Masamichi Mori. Resistance increase in small-area Si-doped Al-n-Si contacts. *IEEE TRANSACTIONS ON ELECTRON DEVICES*, 30(2):81–86, February 1983.

[13] Hiroshi Onoda. Dependence of Al-Si/Si contact resistance on substrate surface orientation. *IEEE Electron Device Letters*, 9(11):613–615, November 1988.

[14] C. S. Pai, E. Cabreros, S. S. Lau, T. E. Seidel, and I. Suni. Rapid thermal annealing of Al-Si contacts. *Applied Physics Letters*, 46(7):652–654, April 1985.

[15] D. Ratakonda, R. Singh, L. Vedula, A. Rohatgi, J. Mejia, and S. Narayanan. Rapid thermal processing of screen printed ohmic contacts. *Journal of the Electrochemical Society*, 144(9):3237–3242, September 1997.

[16] W. R. Runyan and K. E. Bean. *Semiconductor Integrated Circuit Procesing Technology.* Addison-Wesley Publishing Company, Inc, United States of America, July 1990. P.662, 353, 532, 530.

[17] H-J. Schluter, H. Zuchner, R. Braun, and H. Buhl. Diffusion of hydrogen in aluminium. *Zeitschrift fur Physikalische Chemie*, 181:103–109, 1993. pt.1-2.

[18] Dieter K. Schroeder. *Semiconductor material and device characterization.* Wiley-Interscience, United States of America, 1990. P.100, 103, 105, 108.

[19] S. M. Sze. *Physics of Semiconductor Devices.* John Wiley Sons Inc, 605 Third Avenue New York New York, 2nd edition, May 1981. P.304–305.

[20] A. S. Yapsir, P. Bai, and T-M. Lu. Formation of low-temperature Al/n-type Si Schottky contacts using a partially ionized beam deposition technique. *Applied Physics Letters*, 53(10):905–907, September 1988.