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Electrical characterization of impurity-free disordering-induced defects in *n*-GaAs using native oxide layers

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ABSTRACT Defects created in rapid thermally annealed *n*-GaAs epilayers capped with native oxide layers have been investigated using deep-level transient spectroscopy (DLTS). The native oxide layers were formed at room temperature using pulsed anodic oxidation. A hole trap H0, due to either interface states or injection of interstitials, is observed around the detection limit of DLTS in oxidized samples. Rapid thermal annealing introduces three additional minority-carrier traps H1 ($E_V + 0.44$ eV), H2 ($E_V + 0.73$ eV), and H3 ($E_V + 0.76$ eV). These hole traps are introduced in conjunction with electron traps S1 ($E_C - 0.23$ eV) and S2 ($E_C - 0.45$ eV), which are observed in the same epilayers following disordering using SiO_2 capping layers. We also provide evidence that a hole trap whose DLTS peak overlaps with that of EL2 is present in the disordered *n*-GaAs layers. The mechanisms through which these hole traps are created are discussed. Capacitance–voltage measurements reveal that impurity-free disordering using native oxides of GaAs produced higher free-carrier compensation compared to SiO_2 capping layers.

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Impurity-free disordering (IFD) of III–V semiconductor structures has been actively researched over the past two decades for the monolithic integration of optoelectronic and photonic devices with different functionalities [1, 2]. IFD is often achieved using dielectric capping layers, such as SiO_2 [1–5] or the native oxides of the compound semiconductors [1, 6–8], followed by annealing. However, as pointed out in a recent review of point defects and diffusion in thin films of GaAs, the technological viability of IFD has been limited by reproducibility and controllability issues [9]. These issues can be related to the current poor understanding of two critical success factors, namely (i) the influence of dielectric layer quality on IFD and (ii) the defect engineering underlying the disordering process. Although the first factor has received some attention in the past few years [3–5, 10–12], the second has remained mostly untouched. Previous studies have provided evidence that IFD proceeds via the diffusion of point defects on the group-III sublattice, namely the gallium vacancy (V_{Ga}) in GaAs-based systems [8, 9, 13–15]. The use of defect engineering to tailor the properties of semiconductors requires knowledge of the structure and energy levels in the forbidden gap, as well of as the diffusion mechanism of defects and the influence of processing parameters on their introduction rates.

In this communication, we report on the electrical properties of defects created in *n*-GaAs epilayers by rapid thermal annealing (RTA) of native oxide layers. Pulsed anodic oxidation is used to form thin native oxide layers on the surface of GaAs at room temperature. A comparison is also made with defects created in the same epilayers using SiO_2 capping layers.

Epitaxial *n*-type GaAs layers of (100) orientation and doped with $\sim 1.1 \times 10^{16}$ Si/cm^3 were grown by metalorganic chemical vapor deposition (MOCVD). Pulsed anodic oxidation was used to form ~ 25- or ~ 50-nm thick layers of native oxides on samples (samples AO1 and AO2, respectively) using the setup and conditions described in [7]. The native oxides on one sample were etched away using diluted HCl, and this sample, thereafter referred to as AO0, did not undergo annealing. Another set of samples was capped with 200-nm SiO_2 by plasma-enhanced chemical vapor deposition (sample SO). RTA was performed on samples AO1, AO2, and SO at 900 °C for 30 s under Ar flow in order to initiate the disordering process. Gold Schottky-barrier diodes of 200-nm thickness and 0.77-mm diameter were fabricated on the chemically cleaned samples. Deep-level transient spectroscopy (DLTS) was used to study the IFD-induced defects, and high-frequency (1 MHz) capacitance–voltage (*C*–*V*) measurements were used to determine the doping concentration, N_D, in the samples.

Figure 1 shows the depth profiles of free carriers, N_D, in as-grown (open triangles) and IFD *n*-GaAs samples (solid circles, open circles, and open diamonds corresponding to samples SO, AO1, and AO2, respectively). It is evident that the extent of free-carrier compensation, ΔN_D, is more significant in epilayers disordered using the native oxide layers compared to using a SiO_2 capping layer. The presence of one electron trap with surface concentration, N_{T0}, and characteristic decay length, λ, can be used

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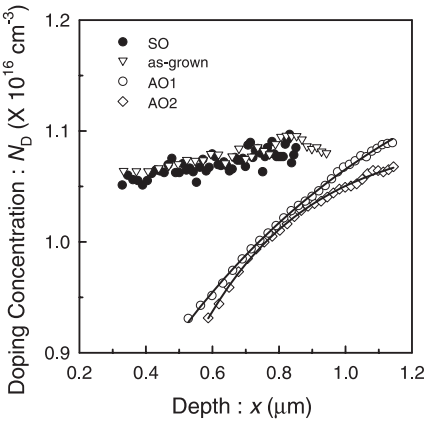

FIGURE 1 Free-carrier profiles of as-grown (*open triangles*) and impurity-free disordered (*solid circles*, *open circles*, and *open diamonds* correspond to samples SO, AO1, and AO2, respectively) *n*-GaAs epitaxial layers. The *solid lines through data points* for samples AO1 and AO2 are fits to (1)

to adequately account for ΔN_D. The spatial variation of the free-carrier concentration, $N_D(x)$, can, therefore, be expressed as

$$N_D(x) = N_D(\infty) - N_{T0}\exp(-x/\lambda), \quad (1)$$

where $N_D(\infty) \approx 1.1 \times 10^{16}\,cm^{-3}$ is the uncompensated free-carrier concentration. The solid lines through the data points for samples AO1 and AO2 are fittings to (1). The values of the fitting parameters are ($N_{T0} \approx 6 \times 10^{15}\,cm^{-3}$, $\lambda \approx 0.78\,\mu m$) for AO1 and ($N_{T0} \approx 1 \times 10^{16}\,cm^{-3}$, $\lambda \approx 0.32\,\mu m$) for AO2, which suggest that defects with different diffusion lengths dominate in the two samples.

We now turn to the electrically active defects introduced by IFD in the *n*-GaAs epitaxial layers. DLTS spectra (a) in Fig. 2 were taken from as-grown epilayers (dotted line) and sample AO2 (solid line) prior to annealing. Only EL2 ($\sim E_C - 0.79\,eV$), which is commonly observed in MOCVD-grown *n*-type GaAs epilayers, is detected in our as-grown epilayers with concentration $\sim 10^{13}\,cm^{-3}$. A hole trap H0 is observed in samples following anodic oxidation, but no distinctive change in the concentration of EL2 is apparent. It is pointed out that the DLTS spectrum measured from sample AO0 is identical to the one shown by a solid line in Fig. 2a. IFD introduces additional hole traps H1, H2 ($\sim E_V + 0.73\,eV$), and H3 ($\sim E_V + 0.76\,eV$), as shown by the DLTS spectra

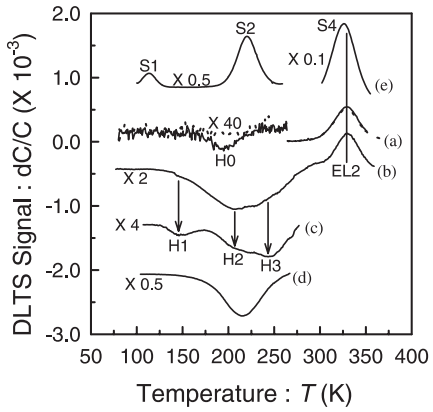

FIGURE 2 DLTS spectra taken from (a) as-grown *n*-GaAs layers (*dotted line*) and pulsed anodically oxidized sample AO2 (*solid line*) using $V_r = -2\,V$ and $V_p = 2\,V$. Spectra (b), (c), and (d) are taken from impurity-free disordered epilayers AO2 using $V_r = -4\,V$ and $V_p = 2\,V$, $V_r = -2\,V$ and $V_p = 1.5\,V$, and $V_r = -2\,V$ and $V_p = 2.4\,V$, respectively. Spectrum (e) is from rapid thermally annealed SiO_2-capped *n*-GaAs samples using $V_r = -2\,V$ and $V_p = 2\,V$. All spectra were measured using a filling pulse width of 50 ms and a rate window of $(2.56\,s)^{-1}$

(b) and (c) in Fig. 2. Spectra (b), (c), and (d) were taken from annealed sample AO2 using different quiescent biases, V_r, and filling pulses, V_p ($V_r = -4\,V$; $V_p = 2\,V$, $V_r = -2\,V$; $V_p = 1.5\,V$, and $V_r = -2\,V$, $V_p = 2.4\,V$, respectively). Hence, the differences between these three spectra relate to the different depth distributions of H1, H2, and H3. The apparently single-defect peak at $\sim 216\,K$ in spectrum (d) is due to the superposition of the defect peaks of H2 and H3, and being broad it masks the smaller defect peak of H1. A comparison of spectra (b), (c), and (d) also reveals that EL2 could be observed in the annealed anodically oxidized GaAs epilayers only by probing a region far from the native oxide/GaAs interface. Issues related to the detection of EL2 in our samples will be treated later. It is worth noting here that it is generally assumed that the occupation of traps in a Schottky-barrier diode is everywhere determined by the electron quasi-Fermi level (i.e. only majority carrier traps can be detected). However, as explained in [20], hole traps may also be detected using Schottky diodes, especially in a region close to the metal. We will demonstrate later that electron traps are also introduced in samples disordered using native oxide layers.

The electronic signatures (i.e. activation energy, E_a, and apparent capture cross section, σ_a) of defects were extracted from the Arrhenius-like plots of $\ln(T^2/e_n)$ versus $1000/T$ depicted in Fig. 3 (T is the measurement temperature and e_n is the emission rate). The signature of a hole trap was extracted from the slope of a least-squares fit (solid line) through the data points (open symbols) in Fig. 3. The defect signatures are: H1 [$E_a \sim (E_V + 0.44) \pm 0.04\,eV$, $\sigma_a \sim 10^{-13}\,cm^2$], H2 [$E_a \sim (E_V + 0.73) \pm 0.08\,eV$, $\sigma_a \sim 10^{-9}\,cm^2$], and H3 [$E_a \sim (E_V + 0.76) \pm 0.08\,eV$, $\sigma_a \sim 10^{-10}\,cm^2$]. The Arrhenius plots for H2 and H3 deviate from linearity because of their overlapping peaks, and also because they overlap with an electron trap S2 as will be shown later. Consequently, a fairly large error ($\pm 0.08\,eV$) is associated with the values of E_a for H2 and H3. There are two further points worth noting concerning the signatures of the defects. Firstly, small deviations from linearity of Arrhenius plots may result in large variations in σ_a, which is determined by extrapolating the least-squares fit through data points to $T \to \infty$. This could well explain the unusually large values of σ_a determined for H2 and H3. Secondly, the value of E_a obtained from Fig. 3 also includes an energy component for minority-carrier capture, which we have not measured.

The origin of traps in IFD *n*-GaAs is now discussed. Although we have not been able to determine the electronic signature of H0, we can speculate on the possible causes for its creation. Anodic oxidation of GaAs has previously been shown to create interface states, which

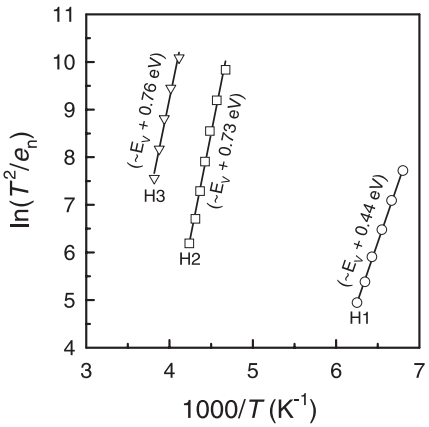

FIGURE 3 Arrhenius plots of $\ln(T^2/e_n)$ versus $1000/T$ from which the activation energy, E_a, and the apparent capture cross section, σ_a, of defects are extracted

have discrete energy levels in the band gap [16–18]. Those investigations have shown that the electronic properties of interface states were specific to the surface-oxidation process, and their creation was not understood. Alternatively, defects could be created during the oxidation of GaAs analogous to the injection of silicon interstitials during the thermal oxidation of silicon, as has recently been proposed by Yuan et al. [6]. No levels related to the isolated interstitials of gallium (Ga_i) or arsenic (As_i) can be observed in GaAs [19]. However, defect reactions involving excess Ga_i or As_i can produce both electron and hole traps in GaAs. For instance, excess Ga_i may produce the double-acceptor gallium antisite, Ga_{As}, with hole traps at $E_V + 0.07$ eV $(0/-)$ and $E_V + 0.23$ eV $(-/=)$, in the presence of arsenic vacancies, V_{As} (i.e. $Ga_i + V_{As} \rightarrow Ga_{As}$). However, Ga_{As} has a relatively high energy of formation, which is predicted to be ~ 10 eV [19], and its formation should be inhibited during simultaneous injection of As_i (since $As_i + V_{As} \rightarrow 0$). Since no study has yet reported the formation of defects resulting from the injection of intrinsic defects during electrochemical oxidation of GaAs, further investigation of defects, such as H0, is required.

The disordering-induced defects created using native oxide layers arise during metallurgical reactions between GaAs and the native oxides of Ga and As [8]. Although the exact interfacial reactions are not known, we have recently proposed that chemical reactions could involve the oxidation of Ga atoms in the near-surface region of GaAs epilayers by (a) reaction with moisture in the anodic oxide layer and (b) reduction of the thermodynamically unstable oxides of As [7]. Two scenarios can be envisaged here, namely (1) oxidation of out-diffusing Ga atoms into the anodic oxide layer resulting in the generation of excess V_{Ga} and/or (2) oxidation of Ga at the anodic oxide/GaAs interface, which creates an increase in the ratio of Ga:As, and hence, hole traps resulting from defect reactions involving Ga_i and Ga_{As} as discussed above. The oxidation of As may occur simultaneously but As_2O_5 being thermodynamically unstable at 900 °C is either reduced by Ga atoms or is decomposed. The low thermal stability of oxides of arsenic may also produce a porous layer of gallium oxide through which As from the near-surface layer of GaAs may desorb. This loss of As will also increase the ratio of Ga:As in the near-surface region of GaAs. At this point in time, the exact origin and structure of traps H1–H3 remain unknown. Nevertheless, it can be concluded that IFD using native oxides of Ga and As, and SiO_2 capping, are significantly different. Spectrum (e) in Fig. 2 illustrates the three dominant electron traps S1 $[E_a \sim (E_C - 0.23) \pm 0.02$ eV, $\sigma_a \sim 7 \times 10^{-15}$ cm^2], S2 $[E_a \sim (E_C - 0.45) \pm 0.02$ eV, $\sigma_a \sim 5 \times 10^{-15}$ cm^2], and S4 $[E_a \sim (E_C - 0.74) \pm 0.03$ eV, $\sigma_a \sim 4 \times 10^{-14}$ cm^2] that are created in rapid thermally annealed n-GaAs epilayers capped with a SiO_2 layer. We have previously reported that these defects are related to V_{Ga}, As_i, As_{Ga}, or complexes thereof [14].

We now demonstrate that electron traps are also introduced in n-GaAs samples disordered using native oxide layers. Figure 4 illustrates DLTS profiles measured from IFD sample AO2 using different bias conditions. Spectrum (a) shows that hole traps H2 and H3 are dominant when the diode is placed under forward bias (i.e. in a region near the metal), as is the case in sample AO2 (Fig. 2c, d). However, when sample AO1 is probed further away from the metal contact (Fig. 4b), hole traps H2 and H3 are not resolved. A broad defect peak is instead detected over the temperature range marked by the double-ended arrow in Fig. 4b (i.e. ~ 170 K $< T <\sim 240$ K), which arises from the superposition of an electron trap with H2 and H3. This electron trap could be S2. Figure 4a shows that electron traps S1 and S3 are also detected in IFD samples using native oxide layers. The defect peak of S1 is asymmetric because of the presence of the hole traps at the higher temperatures. S1 and S2 are dominant defects in IFD n-GaAs samples using SiO_2 capping layers as discussed above. We have previously shown that S3 is produced in rapid thermally annealed uncapped n-GaAs epilayers [14], and proposed that it resulted under conditions giving rise to an increase in the ratio Ga:As in the epilayers. Based on these results, we may conclude that the presence of traps S1 and S2 in the sample AO2 is masked by a high concentration of hole traps shown in spectra (b), (c), and (d) in Fig. 2. Figures 2 and 4 reveal that the relative importance of the two scenarios proposed above for defect creation in impurity-free disordered GaAs depends on the thickness of the native oxide layer. It is worth noting here that we have recently observed both hole and electron traps in rapid thermally annealed Si_3N_4/n-GaAs structures [15].

We now explain why EL2 could not be measured in the near-surface region of samples AO1 and AO2 after RTA as illustrated by Fig. 2c, d and Fig. 4a. Figure 5 shows the variation of the peak

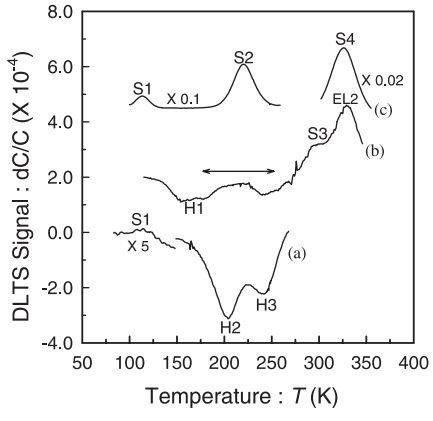

FIGURE 4 DLTS spectra taken from IFD sample AO1 using (a) $V_r = -2$ V and $V_p = 2.4$ V and (b) $V_r = -2$ V and $V_p = 1.5$ V. Spectrum (c) is similar to spectrum (e) in Fig. 2. The broad DLTS peak in the temperature range marked by the double-ended arrow in spectrum (b) suggests the creation of both hole traps H2 and H3, and the electron trap S2 in sample AO1. The electron traps S1 and S3 are also observed in this sample

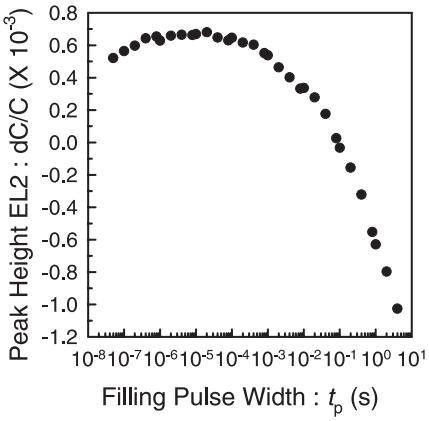

FIGURE 5 Dependence of the peak intensity of EL2 on the filling pulse width, t_p. A quiescent bias, $V_r = -4$ V, and a filling pulse, $V_p = 4.4$ V, were used. The decrease in peak height for the larger pulse widths is characteristic of the capture and emission from a hole trap

intensity of EL2 as a function of filling pulse width, t_p, for $V_r = -4$ V and $V_p = 4.4$ V. The initial increase of peak intensity for $t_p \leq 1\,\mu$s is followed by a saturation level for $1\,\mu s \leq t_p \leq 20\,\mu$s. Any further increase in t_p results in a monotonic decrease in peak intensity, which is characteristic of the filling of a hole trap with a capture cross section much smaller than that of EL2. EL2 has $\sigma_a \sim 10^{-13}$ cm^2 and is easily filled using sub-μs filling pulse widths.

In summary, we have investigated the electrical properties of defects introduced in rapid thermally annealed n-GaAs epitaxial layers capped with native oxide layers grown by pulsed anodic oxidation. A hole trap H0, which could be due to either interface states or the injection of interstitials of Ga or As during oxidation, is observed in the oxidized epilayers. Additional hole traps H1 ($E_V + 0.44$ eV), H2 ($E_V + 0.73$ eV), and H3 ($E_V + 0.76$ eV) are introduced in the annealed samples. We demonstrated that electron traps S1 ($E_C - 0.23$ eV) and S2 ($E_C - 0.45$ eV) are also observed in the same epilayers, but are masked by the larger concentration of hole traps, especially close to the surface. The possible mechanisms responsible for the creation of defects in the disordered epilayers using native oxide layers have been discussed. Disordering using native oxide layers produced more carrier compensation than a SiO_2 capping layer.

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