EVIDENCE OF IMPURITY GETTERING BY INDUSTRIAL PHOSPHORUS DIFFUSION

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ABSTRACT

The possible benefits of phosphorus gettering as applied to production multicrystalline silicon wafers have been evaluated. After optimization of an open tube POCl_3 process, relatively low temperatures and short times have been found to significantly improve the minority carrier lifetime of most wafers. The possible gettering action stemming from the industrial process of phosphorus diffusion has also been investigated and found to be similarly effective. Average lifetimes of $45\mu\text{s}$ (diffusion length of $360\mu\text{m}$) were obtained, with some wafers reaching maximum values up to $130\mu\text{s}$. Lifetime monitoring of a commercial cell fabrication line has also enabled characterization of the voltage limits imposed by the standard emitter and aluminum back-surface-field. The results indicate that the bulk, as improved by emitter gettering, is generally not the limiting factor on cell performance.

INTRODUCTION

The possibility of improving the electronic quality of silicon wafers by extracting impurities from them via a phosphorus diffusion is well known [1,2,3]. The diffusion technique normally used for impurity gettering is based on a liquid POCl_3 source for the dopant. This source has the added advantage of releasing chlorine in the process furnace, which is known to help to avoid contamination of the wafers during high temperature steps.

In this paper we study the possible benefits of phosphorus gettering as applied to multicrystalline silicon grown by BP Solar. After careful optimization of an open tube POCl_3 gettering process, the possible gettering action stemming from the industrial emitter diffusion has been investigated.

In order to put the post-gettering bulk lifetime results in perspective, we have determined the limit imposed on the effective lifetime by both the standard emitter and aluminum back-surface-field (BSF) formation steps used at BP Solar. The results suggest that in most cases, the in-situ gettered bulk lifetime is considerably higher than

the effective lifetime limit imposed by recombination in the emitter, and higher than or comparable to that arising from the aluminum BSF.

EXPERIMENTAL DETAILS

The effect of a phosphorus gettering treatment on the lifetime of a large number of mc-Si wafers from various regions along two different ingots has been investigated using the quasi-steady-state technique [4]. The effectiveness of the gettering treatment is given by the change of the minority carrier lifetime, measured at the same carrier density, before and after gettering. Surface passivation is essential to evaluate the true bulk minority carrier lifetime, and it has been achieved by means of a very light, low temperature phosphorus diffusion at 840°C followed by a short oxidation at the same temperature and a forming gas anneal at 400°C . This process minimizes recombination at both surfaces of the wafer while having a minimal gettering effect. After the intentional gettering diffusion, the wafers were etched $5\text{--}10\mu\text{m}$ per side to remove the heavy diffusion and then passivated again by the 840°C diffusion and thermal oxidation process.

The $11.2 \times 11.2\text{cm}^2$ mc-Si wafers were cut into four smaller sections to facilitate laboratory processing. The lifetime was measured in the center of every section, with the sensing coil extending over a diameter of 2cm ; this gives an average lifetime for the 3cm^2 tested area. We have found significant differences in electronic quality among the four different sections. One particular section of ingot 113C and also of ingot 94G is clearly inferior to the other three sections. In fact, the differences in lifetime found among the different sections is sometimes greater than the differences produced by the gettering treatments. It is important therefore to compare identical sections of the wafers when comparing different gettering treatments, but, even if this is done, a degree of variability between the wafers cannot be excluded.

To minimize wafer to wafer variability we have carefully used wafers from adjacent positions as much as possible. Sister wafers were processed at BP Solar. The results presented are averaged over the four smaller

sections to give values more representative of the entire wafers.

RESULTS AND DISCUSSION

We have previously found that high temperature processing can result in a degradation of some mc-Si materials [5]. Because of this, we have tried to minimize the temperature of the gettering treatment, while maintaining a reasonable level of phosphorus incorporation into the wafer. The main driving factors for phosphorus incorporation at a given temperature are the percentage of POCl_3 in the furnace and the oxygen/ POCl_3 ratio. We have used a low O_2 concentration of 1.1% and a relatively standard 0.2% POCl_3 . With these diffusion conditions we obtained a sheet resistance of about $70\Omega/\text{sq}$ at 870°C for 30 minutes and also at 850°C for 60 minutes. Both gettering temperatures resulted in almost identical improvement of the electronic quality, indicating that the conditions of the treatment are not very critical. The effectiveness of the gettering at 870°C for 30 minutes is shown in Figs. 1 and 2 by a general increase of the lifetime for most regions of the two ingots investigated.

Fig. 1. Bulk lifetimes of mc-Si wafers prior to gettering, and after POCl_3 and industrial diffusion gettering, as a function of wafer number: ingot 113C (1.0 $\Omega\cdot\text{cm}$).

The improvement is particularly important for the regions that showed a low lifetime before gettering (top of the ingot), bringing their quality up to essentially the same level as the other regions. Such a homogenization of the electronic quality has very desirable implications from the mass production point of view. The exception is the very bottom of ingot 94G (see Fig. 2), which is normally cut off and recycled. Despite the fact that we have not observed a particularly high density of dislocations in this region, it is possible that a high density of other micro-defects

dominates the lifetime and/or prevents an effective gettering of the impurities. Lifetimes in excess of $100\mu\text{s}$ were measured for some individual wafers.

The fact that effective impurity gettering can be achieved at relatively low temperatures, as low as the typical phosphorus diffusion conditions used to create the emitter region of the solar cells both in the laboratory and in the industrial environments, raised the hope that the current industrial diffusion process itself may be appropriate as a gettering treatment. We have verified that this is indeed the case. BP Solar's process consists of coating one side of the wafers with a phosphorus source and feeding the wafers onto a conveyor belt that takes them through a large quartz furnace. The typical diffusion time is 12-15 minutes and the temperature $860\text{--}870^\circ\text{C}$. The resulting sheet resistance of the diffused layer is approximately $45\text{--}70\Omega/\text{sq}$.

Fig. 2. Bulk lifetimes of mc-Si wafers prior to gettering, and after POCl_3 and industrial diffusion gettering, as a function of wafer number: ingot 94G (1.5 $\Omega\cdot\text{cm}$).

To assess the impact of the industrial phosphorus diffusion step on the mc-Si wafers themselves, the heavy phosphorus diffused layer was stripped in a silicon etch and a high quality surface passivation was applied to both surfaces. The lifetimes increased substantially, from an average value of approximately $25\mu\text{s}$ before gettering to $45\mu\text{s}$ (ingot 94G, excluding the bottom region) and $60\mu\text{s}$ (ingot 113C, which does not include the bottom). Note that a lifetime of $45\mu\text{s}$ represents a minority carrier diffusion length of $360\mu\text{m}$, significantly greater than the wafer thickness. The improvement is quite general, with the exception of wafers from the very bottom of the ingots, as can be seen in Figs. 1 and 2. The gettering effectiveness of the industrial phosphorus diffusion process is similar to that achieved with the POCl_3 process. This indicates that the gettering action is related

to the incorporation of phosphorus atoms into the silicon rather than to the presence of chlorinated compounds in the furnace. This is not surprising, since the very first evidence of phosphorus gettering was given in 1960 by Goetzberger and Shockley using P_2O_5 [1]. The typical industrial diffusion and also, the typical gettering diffusion from $POCl_3$, result in a surface layer where the chemical concentration of phosphorus atoms is greater than the electrically active solid solubility of about $3 \times 10^{20} \text{cm}^{-3}$. The gettering action seems to come from the excess phosphorus concentration in what has been called in the solar cell community the “dead layer”.

LIMITATIONS DUE TO EMITTER AND BSF

The relatively low sheet resistance of the industrial diffusion, which is necessary to allow ohmic contact of the screen-printed metal fingers, has the coincidental advantage of being a good gettering layer. However, it also has the disadvantage of being a source for additional recombination in the finished cells. In order to quantify this recombination, and to compare it with that represented by the measured bulk lifetimes, single-crystal $1.0\Omega\cdot\text{cm}$ float-zone (FZ) wafers were subjected to the standard emitter formation step. The resulting lifetime was measured to be $26\mu\text{s}$. A high quality passivation treatment had been applied to the rear surface beforehand, which, combined with the knowledge that the bulk wafer lifetime (as measured after diffusion removal and re-passivation) was verified to be $200\text{--}300\mu\text{s}$, indicates that the phosphorus diffused emitter region limits the effective lifetime to $26\mu\text{s}$. This is equivalent to a limit on the achievable open circuit voltage of 626mV .

The emitter contribution to the dark saturation current density J_{0e} was determined from the injection level dependence of the effective lifetime of high resistivity (greater than $50\Omega\cdot\text{cm}$) FZ wafers. A dark saturation current density of $J_{0e} = 8.2 \times 10^{-13} \text{Acm}^{-2}$ was measured at 25°C . This value places a limit on the achievable open-circuit voltage of 625mV , for a $1.0\Omega\cdot\text{cm}$ wafer of thickness $250\mu\text{m}$ and reflectance of 15% , in good agreement with the separate experiment described above. It is interesting to note that these high resistivity wafers exhibited lifetimes above 1ms at carrier densities near the dopant density (around $3 \times 10^{14} \text{cm}^{-3}$), indicating that the industrial diffusion process does not introduce significant contamination into the bulk of the wafers.

The relatively long diffusion lengths measured in the mc-Si wafers, as arising from the in-situ gettering, makes them sensitive to the rear surface, where additional recombination can occur. While Al BSF formation provides a lower surface recombination velocity than plain metal on silicon, the passivation may still be poor enough to impact on performance. The BSF is formed by alloying aluminum which is deposited by screen-printing. After etching the excess aluminum in hot HCl to make the use of the photoconductance tester possible, the measured lifetime on single crystal $1.0\Omega\cdot\text{cm}$ FZ wafers with a high

quality front surface passivation was $46\mu\text{s}$, which is equivalent to an implied voltage of 641mV .

We also used an alternative method based on probing the voltage between the n-type diffusion and p-type Al-doped layer as a function of light intensity [6]. This measurement does not require full contacts to the cell, since no current is drawn from it. The measured $V_{oc} = 640\text{mV}$, corrected for reflectance, is in excellent agreement with the lifetime evaluation. The quality of the BSF layer can also be expressed in terms of a saturation current density of $J_{0(\text{BSF})} = 5 \times 10^{-13} \text{Acm}^{-2}$, or alternatively as a surface recombination velocity of around 500cm/s . The aluminum BSF is, therefore, less restrictive than the phosphorus diffusion.

As a final verification of these results, a further experiment was performed. Rather than using a high-quality front surface passivation, the $1.0\Omega\cdot\text{cm}$ FZ wafers were subjected to both the standard front industrial phosphorus diffusion and rear BSF process steps. After etching the excess aluminum at the rear, we measured a lifetime of $17\mu\text{s}$, which is equivalent to an implied voltage of 615mV . This was corroborated by probing the open-circuit voltage before etching the metal, which resulted in a measurement of 611mV . By adding the inverse lifetimes of the individual emitter and BSF limits (the inverse bulk lifetime is negligible in these FZ wafers), we would expect the results to be $17\mu\text{s}$ and 615mV , in good agreement with these measurements.

Fig. 3. Effective lifetime and voltage caps imposed by the bulk (average values), emitter and BSF regions, and various combinations. The voltage caps are calculated for $1.0\Omega\cdot\text{cm}$ material of thickness $250\mu\text{m}$ and total reflectance of 15% .

These results are summarized graphically in Fig. 3. It depicts the voltage and lifetime caps imposed separately by the emitter, the BSF, bulk lifetimes of 45 and $60\mu\text{s}$ (representing average measured values), as

well as various combinations of the three recombination mechanisms. The combination of emitter, BSF and a bulk lifetime of $60\mu\text{s}$ results in a voltage cap of 608mV , in reasonable agreement with those observed in the completed $1.0\Omega\cdot\text{cm}$ mc-Si cells of up to 602mV (ingot 113C). The lower voltages in the finished cells are due, at least partly, to mild shunting, and also to the presence of silver-contact strips on the rear of the cells, where no passivating BSF is present.

While the results indicate that the bulk is generally not the most limiting factor on cell performance, it still has some impact on the final voltages. Note that for wafers from the bottom region of ingot 94G the bulk is still very important, as it may also be for the entire length of poorer quality mc-Si ingots.

Fig. 4 shows the measured open-circuit voltages as a function of ingot position for finished cells from ingot 94G. The general trend follows that of the lifetime measurements in Fig. 2, confirming the general correlation between the two quantities. The correlation between these two sets of data is not exact however, due to the relatively localized nature of the lifetime measurement technique.

Fig. 4. Open-circuit voltage versus ingot position before and after ARC coating for ingot 94G ($1.5\Omega\cdot\text{cm}$).

CONCLUSIONS

For this particular multicrystalline silicon material, the optimum POCl_3 phosphorus gettering temperature and time are similar to those typically used to form the emitter region of solar cells, albeit with a different mix of gasses in the furnace characterized by a high POCl_3/O_2 ratio, which results in a super-saturation of phosphorus in the wafers. We have subsequently verified that a similarly

effective gettering is provided by the standard industrial phosphorus diffusion process. At present, cell performance is largely limited by other factors, hence there is no need for an extra impurity gettering step. However, the fast gettering treatment verified here may be useful in conjunction with more advanced cell processes. The minority carrier lifetime of the mc-Si wafers after phosphorus diffusion is of the order of $45\mu\text{s}$, which represents a minority carrier diffusion length of $360\mu\text{m}$, significantly greater than the wafer thickness.

Such diffusion lengths indicate that the rear surface of the wafers can play an important role in the performance of industrial cells. Characterization of the standard emitter and BSF formation steps revealed, however, that recombination in the unpassivated emitter places the strictest cap on the achievable voltage, followed by the BSF and then the bulk (after in-situ gettering). Hence, the wafer quality itself does not appear to be the most severe limitation to present solar cell efficiency, which offers significant scope for its enhancement via advanced device design.

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