ABSTRACT: The PERC cell design offers the possibility of significantly improved performance over conventional commercial cell designs with only a small increase in process complexity. Optimisation of the PERC structure to date has been aimed at high efficiency cells. This paper reports the results of comprehensive modelling to determine what advantage the PERC structure with dot or stripe contacts has over conventional screen printed rear cells for lower quality substrate wafers. The efficiency trade-offs of contact spacing and contact area are investigated as a function of wafer resistivity, diffusion length and wafer thickness, taking into account recombination elsewhere in the device. The efficiency for a PERC cell and a cell with a silver screen printed rear are compared for different wafer resistivities.

Keywords: Modelling - 1: c-Si - 2: Multi-crystalline - 3

1. INTRODUCTION

The PERC (passivated emitter and rear cell) structure was developed by one of the authors in 1988 [1] and produced record efficiency silicon cells for that time. It has a lightly doped emitter with heavier diffusions under the front contacts, a SiO$_2$ passivating layer and antireflection coating, and inverted pyramids on the top surface (figure 1). Rear contact is made directly to the substrate via contact holes through the rear oxide, without the use of a boron diffusion. The spacing of the holes is large compared to the cell thickness in order to minimise contact recombination. The substrate of the record efficiency cell was reasonably heavily doped (0.2–0.5Ωcm) in order to reduce series resistance due to the widely spaced contacts and to allow low resistance contact to be made with aluminium to the substrate.

The PERC cell design offers the possibility of significantly improved performance over conventional commercial cell designs with only a small increase in process complexity. For example, a high quality bifacial commercial multicrystalline cell could be made simply by phosphorus diffusing the top surface, depositing silicon nitride on both surfaces, screen printing aluminium on the rear and silver on the front and firing through the nitride. For a monofacial cell, stripes could be cut in the silicon nitride with a laser or dicing saw, followed by plasma-spraying aluminium through a shadow mask. A dot contact cell could be made by cutting dots in the silicon nitride with a laser before plasma-spraying, or by locally damaging the nitride with a set of “pins”. The stripe structure has the advantage of a potentially simpler manufacturing process and the possibility of bifacial illumination. These processes avoids all high temperature steps post-diffusion, which allows the large getterted lifetimes to be preserved. Oxidations and boron diffusions after the gettering step tend to degrade the minority carrier lifetime.

The small metallisation fraction of the PERC cell means that recombination at the rear is significantly reduced compared to a cell with 100% rear metallisation. The current increase that goes along with a $V_{oc}$ increase means that overall cell efficiency improvement can be substantial, provided that the diffusion length is larger than the wafer thickness, even neglecting the benefits of the bifacial design.

Spreading resistance losses for majority carriers in the base are proportional to wafer resistivity. High efficiency PERC cells have small contact areas (1%) and large contact spacings (around 2mm) to minimise recombination. This requires relatively low wafer
resistivities (0.2–0.52Ωcm) to keep spreading resistance losses low. The modelling shows that high efficiencies can also be achieved with 10Ωcm material. This allows advantage to be taken of the higher lifetimes achievable with 10Ωcm silicon, which is important for industrial quality multicrystalline material. A broad optimum in the efficiency with back contact fraction and back contact spacing gives flexibility in cell design and manufacturing processes.

2. OTHER STUDIES OF PERC CELLS

Optimisations of the PERC structure have been previously reported in the literature. These papers are aimed at high efficiency cells, and so only consider a narrow range of wafer resistivities and material qualities. Aberle et al. [2] solve the fully coupled set of semiconductor differential equations in two (cartesian) dimensions. Aberle et al. analysed one resistivity (0.52Ωcm), one wafer thickness (280µm), a fixed rear metallisation fraction of 1.5% and only large diffusion lengths. Spacings were restricted to less than 1.4mm because the main emphasis of the modelling was on cells with locally diffused rear contacts.

Sterk et al. [3] used a 3D simplified model which requires the use of assumptions in the calculation of the fill factor. One wafer thickness (200µm), one resistivity (0.52Ωcm) and one diffusion length (500µm) were modelled. Rear metallisation fractions of 0.5% and 4% and contact spacings from 0.02mm to 6mm were used.

Schöffthaler et al. [4] use a 3D model based on Fourier decomposition of the minority carrier diffusion equation. This model also requires extra assumptions for the calculation of the fill factor and again only one wafer thickness, diffusion length and wafer resistivity were modelled. Metallisation fractions of 0.4–16% and contact spacings of 100µm to 10mm were used.

3. MODELLING OF PERC CELLS

The aim of the modelling is to optimise the cell design for stripe and dot back contact structures and determine what advantage the PERC structure has over conventional screen printed rear cells. The modelling package Dessis [5] is used which solves the fully coupled set of semiconductor differential equations. The efficiency trade-offs of contact spacing and contact area are investigated as a function of wafer resistivity, diffusion length and wafer thickness, taking into account recombination elsewhere in the device.

The stripe structure was modelled in two dimensions using cartesian coordinates. The dot structure was modelled using cylindrical coordinates. For dots in a hexagonal pattern, the PERC structure can be modelled with a hexagonal prism as the unit cell. This was replaced with a cylinder to allow the use of cylindrical coordinates. The error introduced by this assumption is expected to be small. Dessis can also be used to solve the semiconductor equations in three dimensions without the need for the assumption of cylindrical symmetry, but such an approach is very computationally intensive, especially for large contact spacings.

A perfectly passivated emitter with negligible sheet resistance was used in order to focus attention on the bulk and rear surface. This was modelled with a 100% front contact and a very heavily doped emitter (2ΩΩ/cm) to make the minority carrier diffusion length in the emitter so low that recombination at the front contact is negligible. Band gap narrowing was turned off to avoid lowering the open circuit voltage through Auger recombination in the emitter. The light was made to appear close to the junction in order to avoid the loss of short wavelength light in the heavily doped emitter. This results in a structure with essentially no recombination at the front surface.

The light intensity was adjusted to give short circuit currents in agreement with the one-dimensional modelling package PCID [6] when diffusions at the rear contacts were added to reduce recombination. Monofacial illumination was used and excellent light trapping was assumed. Shading by metal fingers was not taken into account.

Wafer resistivities of 0.23Ωcm and 1Ωcm were used, with the corresponding contact resistivities for aluminium of 4 × 10⁻⁴Ωcm² and 1 × 10⁻³Ωcm² respectively [7]. Surface recombination velocities of 10cm/s for 1Ωcm material and 100cm/s for 0.23Ωcm material were used. These values have been achieved in the laboratory with silicon nitride on p-type silicon and it is expected that this will soon be repeated in an industrial setting. Back contact spacings were varied from 100µm to 7000µm and back contact fractions from 0.2% to 100%. The wafer thickness was varied in the range 100–400µm. Two bulk minority carrier lifetimes were used for each wafer resistivity, corresponding to industrial quality and state-of-the-art multicrystalline wafers. For 1Ωcm silicon these were 50µs and 400µs, and for 0.23Ωcm they were 5µs and 25µs.

4. RESULTS

There is a broad optimum for back contact spacings and back contact fraction. This optimum broadens further for low wafer resistivities and higher contact fractions. For the dot structure with high quality 1Ωcm material there is less than 0.2% (absolute) difference in efficiency in the back contact spacing range 800–2400µm for a back contact fractions of 1%, as shown in figure 2. For a dot structure with high quality 0.23Ωcm material with a contact fraction of 10% the range for constant efficiency is 1600–8000µm.

The stripe structure shows a broader optimum for back contact spacings than the dot structure. For 0.23Ωcm material with a stripe structure and a back contact fraction of 1% there is less than 0.2% (absolute) difference in efficiency in the range 1200–7200µm whereas for a dot structure with the same contact fraction the range is 800–3600µm. This is due to the lower
The broad optimum in the back contact fraction for both the dot and stripe structures is due to a decrease in recombination offset by an increase in spreading resistance as the contact fraction is decreased. This means it is not necessary to use small dots or thin stripes to achieve high efficiencies. Contacts can also be very widely spaced without significant loss in efficiency.

The difference in efficiency between the stripe structure and the dot structure is small for optimised back contact spacings, as shown in figure 3. It was found that for both 0.20cm and 1Ωcm material with contact fractions of 1% and 10%, the efficiency of the stripe contact structure and the dot structure was the same within the uncertainty of the modelling (0.1% absolute). The optimised back contact spacings for the stripe structure were 3.2mm for a 1% contact fraction and 4.8mm for a 10% contact fraction. For the dot structure the optimised back contact spacings were 1.2mm for a 1% contact fraction and 3.6mm for a 10% contact fraction. The choice of dot or stripe structure will therefore be decided by manufacturability issues. A 1% dot contact with a spacing of 1.2mm corresponds to a dot diameter of 120µm, while a 1% stripe contact with a spacing of 3.2mm will be 32µm wide. Such narrow contacts could present manufacturing difficulties. A larger contact fraction is likely to be tolerable because of the broad optimum in efficiency with contact fraction. The stripe structure may be favoured because it could be formed with a dicing saw rather than requiring a laser and because it lends itself well to a bifacial design.

The results for both dot and stripe contacts show a broad maximum in efficiency as the ratio of diffusion length to wafer thickness ($L/W$) is varied, provided that $L/W > 1$. For high quality 0.20cm and 1Ωcm wafers, and industrial quality 10Ωcm wafers, wafer thickness has little effect on cell performance in the range 100–400µm because $L/W$ is always greater than 1 in this range. For industrial quality 0.20cm material $L/W$ varies from about 0.3 to 0.9 as the wafer thickness is decreased from 400µm to 100µm. The best results with this material using a PERC structure can be obtained with thin (around 100µm) wafers e.g. multicrystalline wafers manufactured by ribbon processes. In this case the use of a thin wafer can increase achievable efficiencies by about 1% absolute as shown in figure 4. The reason for this increase in efficiency is the reduction in bulk recombination as the wafer is made thinner. This is offset to some extent by the increase in recombination rate at the rear contacts as $L/W$ increases and more carriers “see” the contacts.

The efficiency improvement achievable through the use of a PERC structure rather than a 100% back contact is significant, as shown in figure 5. The efficiency difference is 3% absolute for 400µs 1Ωcm silicon, from 18.5% to 21.5%. For 125µs 10Ωcm silicon the improvement is 1.5% absolute from 18.5% to
The efficiency for PERC, PERL and 100% back contact cells as a function of wafer thickness, for a contact fraction of 1% and a back contact spacing of 1600 μm for the PERC and PERL cells. From top to bottom the curves are: 0.2Ωcm PERL (dotted), 0.2Ωcm PERC (solid), 1Ωcm PERL (dash-dot), 1Ωcm PERC (dashes), 0.2Ωcm 100% contact (x), 1Ωcm 100% contact (+).

As expected the influence of the back surface is smaller for lower bulk lifetimes. Significant front surface recombination will also reduce the advantage if the back surface contact is small for a contact fraction of 1%.

**5. CONTACT RESISTANCE IN PERC CELLS**

Contact resistance and spreading resistance in the PERC structure were compared. Contact resistance is given by \( R_c = \rho_b / A \) where \( \rho_b \) is the contact resistivity and \( A \) is the area of the contact. The largest value of contact resistivity between metal and p-type silicon where the contact remains ohmic is about \( 10^{-5} \Omega \text{cm}^2 \) for evaporated contacts [7]. The spreading resistance between a circular contact of radius \( a \) and a plane contact at a distance \( W \) is given by \( R_s = \rho_b/(4a) \), where \( \rho_b \) is the bulk resistivity of the material, with the requirement that \( a << W \). This expression provides a lower bound for the spreading resistance due to the back contacts of a PERC structure. (There is also a lateral resistance component due to the transport of carriers to the neighbourhood of the rear contact. The expression given above is for a plane contact in which the carriers travel through the plane contact with no loss.)

The above expressions are for a single dot contact. To account for dots with a contact spacing \( s \) the resistances must be multiplied by the number of dots per square centimetre which for a hexagonal contact pattern is \( \sqrt{3}/2 \times s^2 \).

In general, contact resistance is much smaller than spreading resistance for contact spacings typically used with the PERC structure. This is illustrated in figure 6 for a 1% contact fraction. Since the optimum efficiency occurs at spacings greater than 800μm, \( R_c \) is less than \( R_{sp} \) for all cases of interest. Therefore the exact value of the contact resistance does not need to be known, although the contact must be ohmic.

**6. CONCLUSIONS**

The PERC structure has significant efficiency advantages for industrial multicrystalline cells over the 100% back contact structure. There is little difference between a stripe structure and a dot structure of the same contact fraction provided the back contact spacing is optimised. Contact resistance is negligible in PERC cells compared to spreading resistance for optimised back contact spacings.

**References**