OXIDE / LPCVD NITRIDE STACKS ON SILICON: THE EFFECTS OF HIGH TEMPERATURE TREATMENTS ON BULK LIFETIME AND ON SURFACE PASSIVATION.

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ABSTRACT: Silicon dioxide / silicon nitride stacks are potentially useful for solar cell applications due to many favourable properties of the silicon nitride. If the thickness of the oxide and nitride is chosen correctly, an oxide / nitride stack behaves as a near ideal antireflection coating. Nitride layers allow significantly increased process flexibility and hence the realisation of novel cell structures. We used LPCVD deposition and in this paper, show that the effective lifetime of an oxide / LPCVD nitride wafer drops after a high temperature anneal in an inert gas ambient. This loss is due almost entirely to a loss of hydrogen from the silicon / oxide interface and a subsequent loss of surface passivation. Damage of the wafer, due to thermal expansion mismatch between nitride and silicon was minimal for all the stack parameters we used, the most extreme being a 25nm oxide under a 94nm nitride. The loss of surface passivation has been characterised as a function of oxide thickness, nitride thickness, anneal temperature and anneal time. Hydrogen can be reintroduced to the interface in a number of ways. We have shown complete repassivation of the interface using a high temperature forming gas anneal.
Keywords: Silicon nitride – 1: LPCVD – 2: Hydrogen passivation - 3

1. INTRODUCTION

Silicon dioxide / silicon nitride stacks can be very useful for solar cell fabrication due to many favourable properties of the silicon nitride. Nitride layers deposited at high temperatures are very hard and therefore scratch resistant; nitride is etched much more slowly than oxide in solutions containing HF; nitride can be used to mask against the oxidation of silicon and a deposited nitride will correct for naturally occurring pinholes in a grown oxide. Further, if oxide and nitride thickness are chosen correctly, an oxide / nitride stack behaves as a near ideal antireflection coating. These attributes allow significantly increased process flexibility and hence the realisation of novel cell structures.

LPCVD was chosen for nitride deposition as it is a reliable, mature technique that can be scaled to cope with large batches and allows conformal coating of all surfaces. It is well known that nitride deposited at low temperatures by PECVD results in excellent surface passivation. For LPCVD nitride, excellent surface passivation is retained if a thin oxide is present under the nitride. However, for both deposition methods, surface passivation is lost once the wafer is heated in an inert gas ambient, for example, if the nitride is used as an oxidation or diffusion mask. In order to take advantage of the physical and chemical properties of silicon nitride, it is useful to deposit the nitride prior to high temperature steps. This paper looks at the effect of these high temperature steps on the effective lifetime and how LPCVD silicon nitride can be used for solar cell production despite of the loss of surface passivation.

2. EXPERIMENTAL DETAILS

Float zone, p-type 1000Ωcm wafers were used as the starting material. Both sides of the wafer were passivated with a light phosphorous diffusion (830°C for 30 minutes $R_{\square}$ ~800-1000Ω/□), a thermally grown oxide (900°C or 1100°C for varying times) and a forming gas anneal (30 minutes at 400ºC in 5% H_2 in Argon). Silicon nitride was then deposited on both sides of the wafer using LPCVD at 750ºC and ~900mtorr. The flow ratio of DCS:NH_3 was between 1:3 and 1:4. Nitride thickness was controlled by varying the deposition time. The wafers were subjected to high temperature steps in a nitrogen ambient at varying temperatures and for varying times. The effective lifetime was determined using quasi-steady state photoconductivity decay (QSS PCD) measurements and from this, the emitter saturation current, J_0, was determined [1].

3. BULK VERSES SURFACE EFFECTS

For all combinations of oxide and nitride thickness trialed in this work, a long, high temperature anneal caused a drop in effective lifetimes (bulk and surface combined) for all injection levels in the range 10^{13}-10^{17}/cm^3. The thermal coefficients of expansion for silicon nitride and silicon are very different (3ppm/K for silicon nitride compared with 2.3ppm/K for silicon). An initial suspicion was that at least some of this drop was caused by the generation of defects in the bulk as a result of stress due to this thermal expansion mismatch.

In an experiment to determine if the drop in lifetime seen after a high temperature anneal of an oxide / nitride stack was caused by damage to the bulk material, the oxide and nitride was stripped from a number of annealed samples. The oxide was then re-grown and passivated with a standard forming gas anneal. The nitride thickness was 37nm in each case and three wafers were used with initial oxide thickness of 100, 225 and 300nm. These wafers had a 900°C anneal for 1 hour and a 1000°C anneal for 1 hour before they were stripped and the oxide was re-grown. The second oxide was 150nm for all samples (grown at 1100ºC). The results for the case of the 100nm oxide are shown in figure 1. In all cases, the final and initial lifetimes curves are essentially identical and we can conclude that the high temperature anneal with nitride has not caused irreversible damage to the wafer bulk in these cases. Also shown in figure 1 is the case of the wafer with no initial protective oxide. Since the effective lifetime of this wafer is much lower than that of a similar wafer which had the same processing except for the presence of an oxide, we can conclude that in the absence of a protective oxide, the high temperature anneal

of the nitride layer has caused irreversible damage to the bulk.

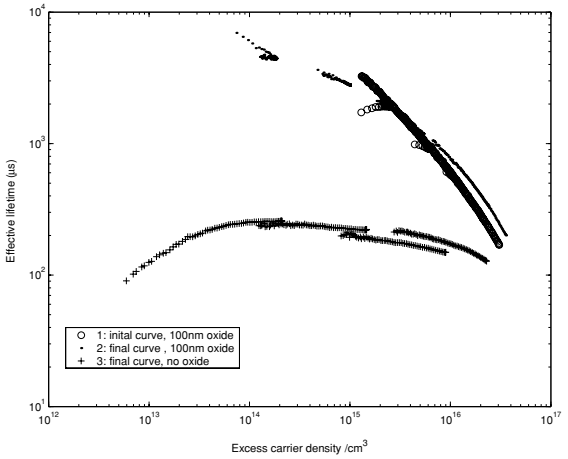

Figure 1 Curves (1) and (2) are for the same wafer shown initially after oxide passivation (1) and finally after oxide / nitride stack formation, high temperature anneal, stack removal and re-passivation (2). The wafers shown in curve (3) had similar treatment to that shown in curve (2) except it did not have an oxide layer. We conclude that the oxide layer provides protection against irreversible damage to the bulk.

For the case of a relatively thin oxide under a thicker nitride, the thermal expansion mismatch between the silicon and the silicon nitride is more likely to cause some damage in the wafer bulk. The case of a 25nm oxide underneath a 94nm nitride is shown in figure 2. After nitride deposition, these wafers also spent 1 hour at 900°C and 1 hour at 1000°C in a nitrogen ambient. The second oxide was also about 25nm thick.

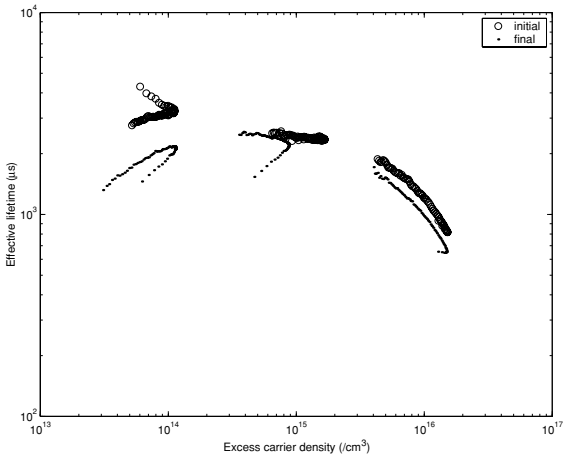

Figure 2 Effective lifetime curves for a wafer passivated with a 25nm oxide (initial), compared with the same wafer after nitride deposition, high temperature anneal in nitrogen, removal of the stack and re-passivation (final). The small decrease in the "final" curve compared with the "initial" curve may be attributable to damage caused by thermal expansion mismatch.

Even with a very thin oxide and a relatively thick nitride, the damage to the material bulk caused by a thermal expansion mismatch is minimal. For this reason, we believe that the drop in lifetime curves seen as a result of long, high temperature anneals is due to a loss of surface passivation.

4. CHARACTERISING THE DROP IN SURFACE PASSIVATION

We believe the drop in surface passivation after an oxide / nitride stack is subjected to a high temperature anneal in nitrogen is due to hydrogen loss at the silicon / oxide interface, which occurs during the high temperature anneals. This is the case whether the wafer has a nitride layer or not. In the case of oxide passivation, an anneal in froming gas at 400°C restores hydrogen passivation. However, hydrogen is unable to diffuse through nitride under the conditions of a standard foming gas anneal (400°C for 30 minutes), and so the loss of hydrogen becomes noticeable in the case of a nitride capped wafer. Hydrogen loss also occurs from the nitride, and this affects the hydrogen content at the silicon / oxide interface. The loss in surface passivation has been characterised in terms of the effect of anneal temperature, anneal time, thickness of the overlaying oxide and the nitride thickness.

4.1. Anneal Temperature

In order to measure the effect of the temperature of the nitrogen anneal on surface passivation loss, wafers were subjected to anneals at a variety of temperatures. The wafers had a light phosphorous diffusion (~930Ω/□), an oxidation (100-310nm) and nitride deposition (two batches; 14 and 24nm). The nitrogen anneals were done for 60 minutes with a flow rate of 120l/hour at temperatures of 750°C to 1000°C, in 50ºC increments. The same wafers were used for each temperature step. Emitter saturation current, J_0, was measured before and after nitride deposition and following each nitrogen anneal. The results are shown in figure 3. For each wafer, J_0 became increasingly worse as the temperature was increased above 750°C. For the thinner oxides the degradation saturated at about 900°C.

These findings can be understood within the context of a hydrogen loss model. Hydrogen is stable within the wafer stack at low temperatures, or for very short times at high temperatures [2]. However, as the temperature is increased, hydrogen bonds at the silicon / oxide interface and within the silicon nitride are broken and hydrogen diffuses from both regions in both directions. The temperature at which hydrogen bonds are broken within the nitride is dependent on the deposition conditions. As hydrogen diffuses away from the silicon / oxide interface, the surface passivation decreases. As long as hydrogen is still present in the nitride, some of this hydrogen will diffuse to the interface and re-passivate the surface to some extent.

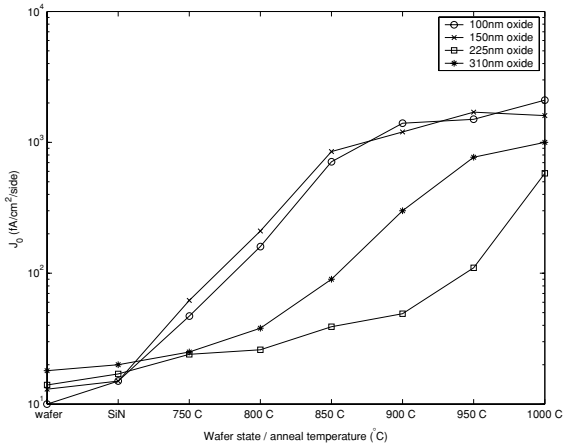

Figure 3 The effect of temperature on J_0 for stacks with 24nm of nitride, varying oxide thickness.

4.2. Anneal Time

The effect of anneal time was investigated using four wafers. These were given a light phosphorous diffusion, oxidation, forming gas anneal and LPCVD nitride deposition. They were then loaded into a 900ºC nitrogen furnace for varying times, after which J_0 was measured. The longer time spent in a high temperature ambient, the more the surface passivation was lost. For a 900°C anneal and a stack with 150nm of oxide, 33nm of nitride, this effect saturated after 45-60 minutes. These results imply that surface passivation may not be lost during a rapid thermal anneal of a wafer with an oxide / nitride stack.

The wafer which had a 15 minute anneal was given another three 15 minute anneals, bringing the total time at 900°C in nitrogen to 1 hour. At this point, J_0 values were similar, ~1600fA/cm^2/side for the wafer with four 15 minute anneals and ~2600fA/cm^2/side for the wafer with one 60 minute anneal. These results imply that it is the total time spent at any one temperature that dictates the drop in surface passivation. Consequently, a series of short anneals could not be used in preference to a longer anneal.

These results fit with a hydrogen loss model in that as hydrogen is removed from the system and surface passivation is consequently lost, further high temperature steps will only serve to remove more hydrogen.

4.3. Oxide Thickness

In order to check if the drop in surface passivation was affected by the oxide thickness, a number of wafers were made with varying oxide thickness. A noticeable trend, that can be seen in figure 3, was that a thicker oxide provided some protection against degradation of J_0 and that this was true for anneals at all temperatures. The fact that a thicker oxide results in a smaller degradation of surface passivation implies that with a thicker oxide a supply of hydrogen is available to passivate the interface following the anneal. A possible explanation is that as the wafer cools, hydrogen in the oxide (originally from both the silicon / oxide interface and the nitride) travels to and passivates the interface. With a thicker oxide, more hydrogen is available at the conclusion of the nitrogen anneal. This indicates that hydrogen readily diffuses through the oxide and is not trapped within the oxide. This conclusion has also been reported by Habraken [4].

4.4. Nitride Thickness

Wafers with a range of deposited nitride thickness and a relatively thin underlying oxide were prepared and the J_0 values after a nitrogen anneal at 900°C and at 1000°C were measured.

After a 900°C anneal, we found a strong correlation between effective lifetime and nitride thickness. A thicker nitride provided some protection against degradation in J_0. However, after a 1 hour anneal at 1000°C in nitrogen, the thicker nitride no longer provided any protection against degradation in surface passivation and J_0 values were equal for all samples. These results are shown in figure 4.

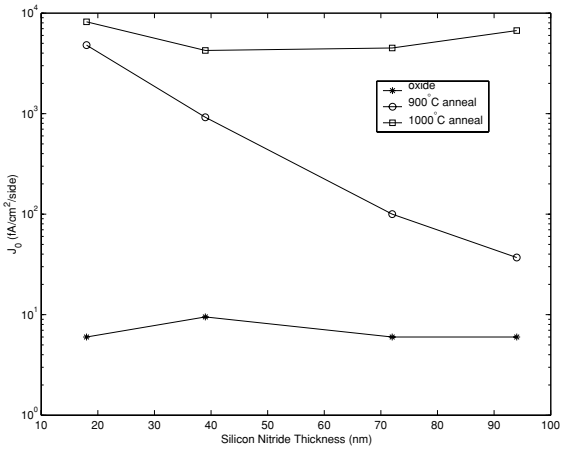

Figure 4 The effect of a 900ºC and 1000ºC anneal in nitrogen on wafers with a relatively thin oxide (20nm) and a much thicker nitride.

These results imply that hydrogen from the nitride diffuses towards the silicon bulk (and at the interface it is available for passivation) as well as out into the gas ambient. The idea that a small percentage of the hydrogen in the nitride would diffuse towards the silicon bulk is reported in the literature [3, 5, 6]. A thicker nitride contains more hydrogen atoms and so the time taken for all of these atoms to diffuse out of the nitride is greater. A small percentage of the hydrogen atoms diffuse towards the silicon bulk and are available to re-passivate the interface. If the wafer is removed from the high temperature nitrogen ambient before hydrogen has been depleted from the nitride, some passivation of the interface will be retained. Arnoldbik et al. [3] have estimated that at any one time, the amount of hydrogen diffusing towards the silicon is only a few percent of the hydrogen which is exiting the wafer into the ambient.

5. RE-INTRODUCTION OF HYDROGEN

The essence of our hydrogen loss model is that at high temperatures in an inert gas ambient, hydrogen diffuses out of all regions of a wafer with an oxide / nitride stack and that this is noticeable primarily because hydrogen can not be reintroduced during a standard 400°C forming gas anneal. It should be therefore be possible, under more extreme conditions, to reintroduce hydrogen to the interface and so re-attain effective lifetime values

close to the initial state.. This has been done using a forming gas anneal at 840ºC for 30 minutes. The results are shown in figure 5 for a wafer that had 100nm of oxide, 33nm of nitride and a nitrogen anneal at 900°C for 60 minutes. As expected, the effective lifetime for the original wafer was high. After the wafer had a nitride deposition and was annealled in nitrogen, the effective lifetime dropped as we have seen before. However, after an anneal in forming gas at 840°C, the lifetime curve was almost indistinguishable from that of the intial wafer, implying that successful reintroduction of hydrogen had occurred and validating the claim that the loss in surface passivation after the high temperature anneal in nitrogen was due to a loss of hydrogen from the silicon / oxide interface.

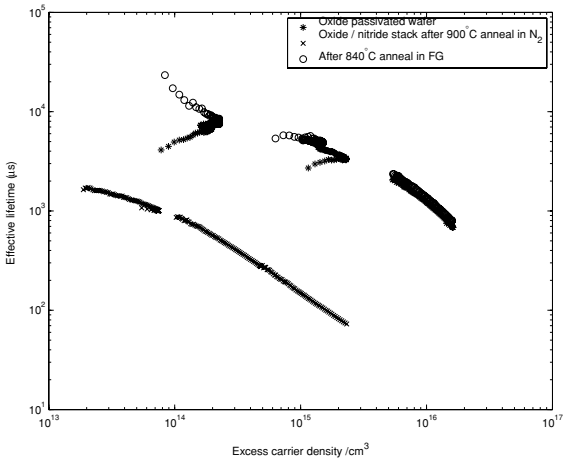

Figure 5 This figure shows how hydrogen can be reintroduced to the wafer to passivate the interface and therefore provide increased effective lifetimes. After hydrogen introduction, the effective lifetime of the wafer was identical to the initial state.

6. CONCLUSIONS

Oxide / LPCVD nitride stacks can provide excellent surface passivation for silicon. We have shown that the drop in effective lifetime following high temperature treatments is due to a loss of surface passivation, rather than to damage to the wafer bulk, except in the case of very thin or no oxides under the nitride. Importantly, surface passivation can be recovered by the re-introduction of hydrogen to the silicon / oxide interface. We believe nitride affects the surface passivation primarily by, at low temperatures, acting as a barrier to hydrogen atoms which may otherwise passivate the interface. When the wafer is subjected to high temperatures in a nitrogen ambient, the hydrogen atoms diffuse from the silicon / oxide interface and from the nitride. Hydrogen from the nitride mainly escapes into the gas phase. However some hydrogen diffuses back towards the bulk and so with a combination of thick nitride and short or low temperature anneals, a thicker nitride may provide some protection against surface passivation degradation. Thick oxides provide minimal protection against degredation in surface passivation. Since the physical damage caused by the nitride is small, even in the case of a 25nm oxide under a 94nm nitride, and hydrogen can be reintroduced to the silicon / oxide interface by an anneal in a forming gas ambient, the thickness of the oxide and nitride layers should be chosen based on processing requirements and antireflection properties.

REFERENCES

[1] D.E. Kane and R.M. Swanson, IEEE Proceedings 1985, 578.
[2] Joseph Z. Xie, Shyam P. Murarka, Xin S. Guo, and William A. Lanford, Journal of Vac Science and Tech. B **7(2)** (1989) 150.
[3] W.M. Arnoldbik, C.H.M. Marée, A.J.H. Maas, M.J. van Boogaard, F.H.P.M. Habraken and A.E.T. Kuiper, Phys. Rev. B. **48(8)** (1993) 5444.
[4] F.H.P.M. Habraken, R.H.G. Tijhaar, W.F. van der Weg, A.E.T. Kuiper, and M.F.C. Willemsen, J. of Appl. Phys. **59(2)** (1986) 447.
[5] Takashi Kuroi, Kenji Umezaw, Kenjiro Oura, and Teruo Hanawa, Jap. J. of Appl. Phys. **27(8)** (1988) 1406.
[6] Christoph Boehme and Gerald Lucovsky, J. of Appl. Phys. **88(10)** (2000) 6055.