65-MICRON THIN MONOCRYSTALLINE SILICON SOLAR CELL TECHNOLOGY ALLOWING 12-FOLD REDUCTION IN SILICON USAGE

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ABSTRACT

Thin (<70 micron) single crystal silicon solar cells have been manufactured through the use of a novel process involving selective etching. Narrow grooves are micromachined through the wafer using a standard micromachining technique with cells manufactured on the resulting silicon strips. These bifacial cells have a much greater surface area than the original wafer, leading to dramatic decreases in processing effort and silicon usage. Individual cells fabricated using the new process have displayed efficiencies up to 17.5% while a $560cm^2$ prototype module has displayed an efficiency of 12.3%. The size, thickness and bifacial nature of the cells offer the opportunity for a wide variety of module architectures and applications.

1. INTRODUCTION

Crystalline silicon remains the major player in the photovoltaic marketplace with 90% of the market, despite the development of a variety of thin film technologies. Silicon's excellent efficiency, stability, material abundance and low toxicity have helped to maintain its position of dominance. However, the cost of the silicon remains a major barrier to reducing the cost of silicon photovoltaics.

Improvements in conventional ingot based technology have mostly arisen through improved wafer sawing to reduce kerf losses and decrease wafer thickness. However, these changes are incremental and are limited by processing yield.

More substantial decreases in silicon usage require a different approach. A variety of techniques for growing or harvesting thin layers of monocrystalline silicon have been developed [1-3] in an attempt to produce thin monocrystalline silicon solar cells. Each has limitations in material quality or yield due to the silicon manufacturing technique.

A new processing technique for thin monocrystalline silicon solar cells has been developed at the Centre for Sustainable Energy Systems at the Australian National University, in conjunction with Origin Energy [1]. The new technology allows for dramatic decreases in silicon usage by up to a factor of 12 (including kerf losses), which means that up to 92% of silicon feedstock can be saved. In addition, it allows for a significant reduction in the numbers of wafers processed per module by up to a factor of 35 compared to standard crystalline silicon technology, which means that the need for wafer throughput is reduced by up to 97%. These factors allow the use of standard moderate quality to high quality silicon and more complicated wafer processing that enable high cell efficiencies while still obtaining significant $/Wp cost savings.

2. THE SLIVER™ CELL CONCEPT

2.1 Selective Micromachining

The new process uses the excellent selectivity of alkaline etches for (111) surfaces, which has been used to good effect in micromachining applications and solar cell texturing. The alkaline etch attacks all crystal planes except the (111) plane relatively rapidly, leaving any etched surfaces covered in (111) planes.

These etchants can be used to form deep narrow grooves in suitably masked wafers oriented such that a (111) plane is perpendicular to the wafer surface. Long narrow slots are opened in the masking layer on the wafer surface, perpendicular to the (111) plane. Etching commences at the surface of these narrow slots.
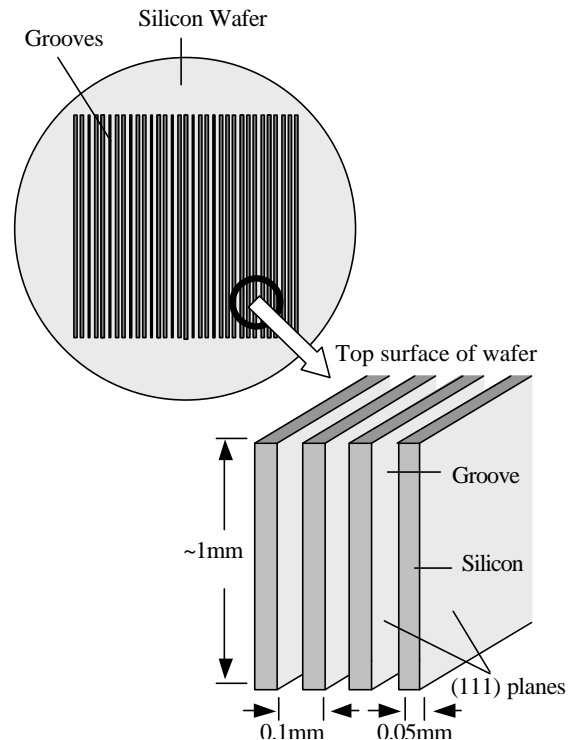

Figure 1. Schematic of selectively etched wafer. Long thin silicon slices are supported by the wafer frame.

A (111) plane extends perpendicular to the wafer surface, so trenches form vertically into the wafer as etching proceeds. The base of the trench etches relatively rapidly compared to the (111) sidewalls. Etching continues until the groove extends the entire thickness of the wafer. The result is a large number of thin silicon strips in the centre of the wafer, held together by the unetched surrounds of the wafer (Figure 1). On 1mm thick 150mm wafers, these strips would typically be

100mm long, 1mm wide (wafer thickness) and 50-65 microns thick.

2.2 Cell design and processing

Cells are constructed on the narrow strips of silicon formed during the micromachining. Cell processing is completed while the silicon strips are still supported by the silicon substrate at the edge of the wafer.

The cells are processed with many of the high performance characteristics of record efficiency device structures, such as heavy doping under the contacts, lightly doped emitter with good surface passivation and surface texturing [4]. A schematic of the cell structure can be seen in figure 2. Heavy phosphorous and boron diffusions are applied to top and bottom surfaces of the wafer. These wafer surfaces become the long narrow edges of the silicon strips and therefore the cells. The edges are subsequently metallised to form the p-type and n-type contacts. The sides of the grooves are textured using a novel texturing technique for (111) surfaces that has been developed at ANU and offers near lambertian light trapping properties. The grooves are then phosphorus diffused and passivated.
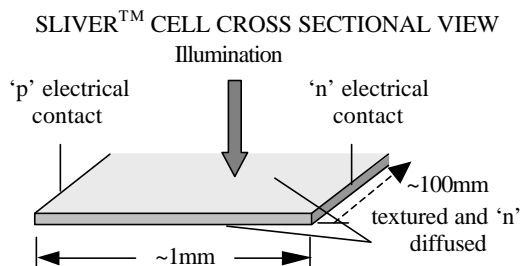
SLIVER^{TM} CELL CROSS SECTIONAL VIEW

Figure 2. Schematic of the Sliver^{TM} cell design.

After processing, the cells are removed from the wafer frame. The resulting cells are long, narrow and thin. Typical Sliver^{TM} cell dimensions are of the order of 60-100mm long, approximately 1mm wide and 50-65microns thick. The cells are illuminated towards either side of the silicon slice (i.e the largest surface area). Since the cell processing is symmetric, the cells are perfectly bifacial – that is, the cell characteristics are identical from either side.

2.3 Sliver^{TM} Cell Performance

The cell structure has the potential for excellent cell efficiencies. Unless the material quality is extremely poor (diffusion length < 100µm), the cell is capable of near unity collection efficiency, since the cell is thin and there are collecting junctions on both sides of the cell. The emitter is also lightly doped and the surface is well passivated. Therefore, almost any quality of monocrystalline silicon from Fz to solar-grade will maintain similar high currents.

The cells structure also offers the opportunity for high cell voltages. The emitter and base contact each cover less than 3% of the cell surface and can be independently doped for optimal passivation of the metal contacts. The cell voltage will be capped more by material quality than surface recombination for most grades of silicon.

To date, the best Sliver^{TM}cell efficiency has been 17.5% for 100 micron thick, 1mm wide devices. Cell characteristics were 655mV V_{oc}, J_{sc} of 34.2mA/cm^2 and 78% FF. These cells were textured and had an oxide antireflection (AR) coating. The oxide AR coating limited cell efficiency due to reflection losses. Efficiencies exceeding 19% are expected with SiN AR coating and further technology optimisation. 19% test devices have been made with dicing saw cut cells that had random pyramid texturing. Voltages on these test cells exceeded 670mV.

3. SLIVER^{TM} CELL MODULES

Sliver^{TM} cells differ significantly from conventional cells in size and shape, being long, narrow, thin and flexible. Since there are typically a thousand or more Sliver^{TM} cells per module, this offers opportunities for flexibility in module design and interconnection compared with conventional modules.

3.1 Novel Module Design

Even greater processing and silicon reductions can be gained (factor of 2 to 3) through the use of a novel module design. Unlike conventional cells, Sliver^{TM} cells have a width that is of the order of the thickness of the module. This allows for the design of efficient reflective structures to redirect light striking the module adjacent to the cells onto the cell for absorption. In addition, the cells are bifacial which further improves the design flexibility and performance of these structures. Conventional cells cannot achieve significant spacing (compared to the cell dimensions) without compromising too greatly on efficiency due to their large size.

A simple design approach is to introduce a lambertian reflector to the rear of a bi-glass module. The cells are positioned between the two layers of glass. The cells are then spaced some multiple of their width, typically from 1.5-3 (See figure 3). Some of the light scattered from the rear reflector is directed onto the rear surface of the bifacial Sliver^{TM} cell while another fraction of the light is reflected onto the glass where it is totally internally reflected back into the module. The remainder of the light is lost through the front glass.
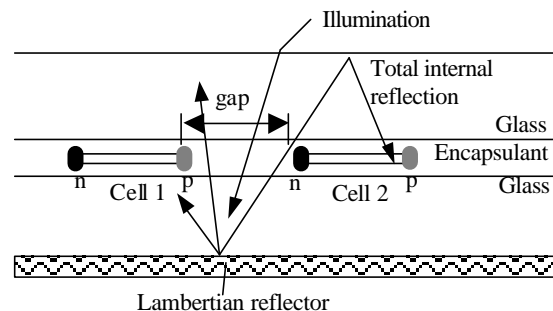

Figure 3. Lambertian reflector module design. The narrow width and the bifacial nature of the Sliver^{TM} cell enables the cells to be spaced (in this example with gaps equal to the cell width), reducing silicon use further.

The efficiency of this simple structure is surprisingly high with greater than 84% of the light entering the module captured for a 50% decrease in the silicon used per square metre (i.e. the cells are spaced with gaps equal to their width) and 74% of the light in the module is captured for the 66% reduction in silicon (gaps double cell width). The saving in grams of silicon per W_{peak} of module power

is approximately reduced by the optical efficiency, compared to the savings in weight per square metre of module.

Even better optical performance is possible with geometric designs. However, the cost of machining appropriate shapes and accurately aligning cells currently outweighs the performance benefits compared to the lambertian reflector.
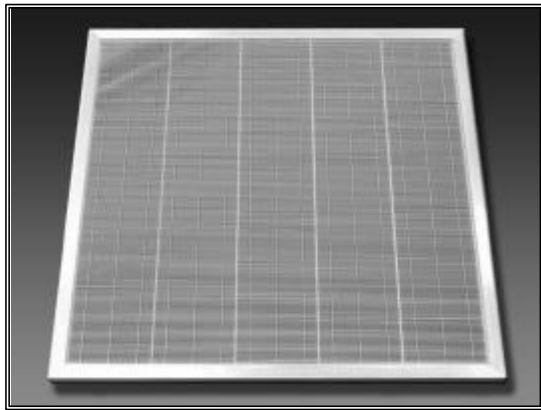

Figure 4. 1000cm^2 Sliver^{TM} module with 5 series strings of cells. The cells are spaced with gaps equal to cell width and the module has a lambertian reflector, as per figure 3.

3.2 Flexible Module Output

The small size of each cell means thousands of cells are required per square metre of module. These are assembled into modules by using high-speed assembling equipment similar to those developed for the microelectronics and opto-electronics industry. This automated cell placement allows tremendous flexibility in cell layout and interconnection.

By connecting cells in series, it is easier to build voltage than in conventional modules where the economies of scale are pushing towards larger and larger cells. Module output can be tuned from standard 12V applications to several hundred volts for grid connected applications. 200-400V modules require several hundred cells in series. Strings of Sliver^{TM} cells with this output only require lengths of the order of tens of centimetres. Series strings can be connected in parallel to increase current. These higher voltage modules could allow for direct conversion from DC to AC without the requirement for a transformer in the inverter, reducing inverter costs.

Since the cells are relatively small in area, so are the cell currents. This decreases the reverse current that any cell needs to tolerate during shading events. Cells can be designed which can reversibly breakdown to 100mA or more, alleviating the need for diode protection in the module. Modules containing strings of Sliver^{TM} cells have passed hot spot tests without by-pass diodes.

3.3 Novel cell applications

In addition to direct competition with conventional PV modules, this novel technology is well suited to satellites, solar-powered aircraft and building integrated PV and other architectural applications where the low power to weight ratio, bifacial nature, size and/or output flexibility offer considerable benefits.

Transparent bi-glass modules can be easily formed for architectural applications simply by removing the lambertian rear reflector from figure 3. Transmission can

be simply tuned by adjusting the cell spacing (at the expense of reduced module output).

The light weight, bifacial nature and high efficiency potential suggest that Sliver^{TM} cells would be well suited to satellite and solar aeroplane applications. The cells are much lighter than conventional silicon cells, and should be more radiation tolerant due to the low thickness. Currents should not degrade significantly until the diffusion length is less than the cell thickness while voltage decreases slowly due to the increased emitter and bulk recombination.

3.3 Module Performance Measurements

A 560cm^2 prototype module was constructed with 500 silicon solar cells fabricated with the Sliver^{TM} cell process, except that they had a SiN AR coat and no texturing. The cells fabricated from 100mm wafers were only 0.56cm^2. The cells were connected in four strings of 125 cells. The cells are spaced in such a way that there is a gap between cells equal to their width. A module efficiency of 12.3% was independently measured by Sandia National Laboratories. Texturing will offer better reflection control after encapsulation and should push this efficiency over 14% (as achieved with a Sandia tested 1000cm^2 module with the test cells described in section 2.3).
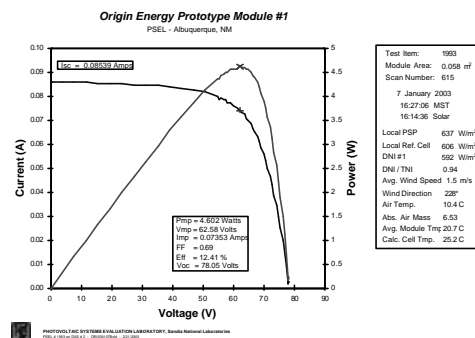

Figure 5. Prototype module results from Sandia. The module demonstrated an efficiency of 12.3% under standard conditions.

The output of this module with the four strings in parallel was V_{oc} 79.6V and V_{mp} 61.6V. With the four strings connected in series, open circuit voltage approached 320V.

3.4 Temperature Response

Sliver^{TM} modules operate at lower temperatures and have lower temperature coefficients than conventional modules. Temperature coefficients are lower since the individual cells are more efficient, with typical V_{oc} near 650mV. This reduces the loss in V_{oc} per degree temperature increase to 2.0mV, approximately 10% less than a conventional cell. The module also operates at a lower temperature since the cells are spaced and some of the light escapes. This means a Sliver^{TM} module will provide more power under operating conditions than a similarly rated conventional module.

4. THE SLIVER^{TM} CELL PROCESSING ADVANTAGE

The combination of the novel cell processing and the module design flexibility provides Sliver^{TM} cells with the

potential for tremendous savings in the amount of silicon required and the number of wafers used per MW of module production. These gains are achieved through the increase in silicon surface area during etching and the spacing of cells in the module.

The gain in surface area from etching is determined from the pitch, p, of the etching, the thickness of the wafer, t_{sliver} and the fraction of the wafer that can be etched to form silicon slices, f. Not all the wafer can be used due to the need for the edge of the wafer to form a frame to hold the cells. The area gain is then given by

$$\text{Area Gain (A)}=f.t_{sliver}/p \qquad (1)$$

For example, a 1mm wafer etched at 100micron pitch with 70% of the wafer used would lead to a 7-fold increase in the surface area of Sliver^{TM} cells compared to the wafer area. Therefore, the area of cells from a single 150mm 1mm thick wafer would be 1237cm^2 compared to the wafer area of 177cm^2. Even greater gains can be achieved with reduced pitch.

Additional area gains can be made by spacing the wafers in the module as described in section 3.1. The area gain per wafer is simply increased by the spacing. If the cells from the wafer described in the previous paragraph were spaced by a factor of double their width (sf=2), the area gain increases to Asf = 7.2 = 14. Greater spacing increases this gain.

The reduction in silicon feedstock required per module compared to conventional technology is reduced compared to the area gain as the conventional wafers are thinner. The weight saving is given by

$$\text{Weight saving (W)}=A.sf.(t_{con} + kerf)/(t_{sliver} + kerf) \quad (2)$$

Assuming a kerf loss and saw damage loss of 260micron and a conventional substrate thickness of 320micron (post saw damage) the weight saving for the previous examples is greater than 6 times.

Of more interest is the saving in grams of silicon per Watt of power output and the number of wafers that are required per MW of power produced. These indicate the true silicon and manufacturing savings.

These savings cannot be determined with simple analytical equations like (1) and (2). A more complicated model is required as cell and module efficiency varies with such factors as the etching pitch (affects the cell thickness), wafer thickness (affects cell width and series resistance losses) and the cell spacing in the module (affects module optical efficiency).

The comparison is made to conventional pseudosquared Cz wafers with thickness 320μm, kerf 260μm and module efficiency of 13.5% yielding around 13g/Wp. Processing yields are assumed to be similar.

A typical mono- or multi-crystalline PV technology requires in the order of 13 tonnes of silicon ingots per MW. The Sliver^{TM} cell technology has already demonstrated a cell power to weight ratio greater than 1500W/kg. The need for silicon ingot can be reduced down to 1.1 tonne per MW, a 12-fold reduction or a 92% saving in silicon material.

Tremendous gains in total cell power per wafer are possible due to the cell area gain and module design. This decreases the number of wafers required to be processed per MW$_{peak}$ of factory output. The modelled savings in reduced silicon usage and wafers per MW of production are displayed for various process assumptions in Table 1. With thicker wafers, large cell spacings and reduced pitch, 35 times fewer wafers are required compared to conventional modules for similar production output, a wafer throughput reduction of 97%.

Wafer thick. (mm)	Pitch (μm)	Gap between cells	Silicon saved (g/W)	Manufacturing saving (Wafers/MWp)	Model module eff (%)
1	100	No gap	4-fold	10-fold	16.8
1	100	Cell width	8-fold	16-fold	14.1
1.5	90	2x cell width	12-fold	35-fold	12.2

Table 1. Silicon weight and manufacturing savings possible with Sliver^{TM} cells.

The reductions in the amount of silicon and the wafers manufactured per MW offer tremendous potential for reduced costs while maintaining design and process flexibility. Due to the silicon savings, better quality silicon can be used to maintain higher efficiency or lower quality material can be substituted to save costs. The saving in manufacturing is particular attractive as it allows for relatively expensive processing to be undertaken (e.g. photolithography, tube furnaces, evaporated and plated contacts) which help maintain high performance.

5. CONCLUSIONS

The Sliver^{TM} cell concept is a new technique for producing thin monocrystalline silicon solar cells. Micromachining of thin silicon sheets enables large areas of cells, and therefore power, to be processed per wafer. Cells are long, narrow, highly efficient and bifacial enabling the use of novel module designs that help to further reduce silicon usage. This can enable up to 12-fold (92%) savings in silicon feedstock and 25-fold (97%) savings in wafers needed per MW of module production.

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