Fabrication of Schottky barrier MOSFETs using self-assembly CoSi₂ nanopatterning and spacer gate technologies

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Abstract

A self-assembly patterning method for generation of epitaxial CoSi₂ nanostructures was used to fabricate 50 nm channel-length MOSFETs. The transistors have either a symmetric structure with Schottky source and drain or an asymmetric structure with n⁺-source and Schottky drain. The patterning technique is based on anisotropic diffusion of Co/Si atoms in a strain field during rapid thermal oxidation. The strain field is generated along the edges of a mask consisting of 20 nm SiO₂ and 300 nm Si₃N₄. During rapid thermal oxinitridation (RTON) of the masked silicide structure, a well-defined separation of the silicide layer forms along the edge of the mask. These highly uniform gaps define the channel region of the fabricated device. The separated silicide layers act as metal source and drain. A poly-Si spacer was used as the gate contact. The asymmetric transistor was fabricated by ion implantation into the unprotected CoSi₂ layer and a subsequent out-diffusion process to form the n⁺-source. I–V characteristics of both the symmetric and asymmetric transistor structures have been investigated.

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1. Introduction

Scaling of MOSFETs becomes difficult when gate lengths shrink below 100 nm. Lithography techniques increase in complexity and new materials and processes need to be developed to fulfill the stringent requirements that the International Roadmap of Semiconductor Devices (ITRS) [1] imposes on the performance of future silicon devices. This encourages the search for alternative and reasonably priced nanopatterning methods as well as for new device concepts. Self-assembly patterning is one attractive

way to produce nanostructures quickly and at a very low cost. Recently, we published a self-assembly method for patterning thin epitaxial CoSi₂ layers into nanostructures by local oxidation of silicide layers [2,3]. Conventional optical lithography and standard silicon processing steps are involved to fabricate CoSi₂ nanostructures. Gaps and CoSi₂ wires with a feature size of 50 nm have been made by applying the stress field at various positions. Using this technique we have also fabricated Schottky barrier MOSFETs (SB-MOSFETs) [2,4,5]. The transistor uses CoSi₂/Si Schottky contacts at both source and drain. It can be operated at both inversion and accumulation modes [4,5]. Due to the high Schottky barrier heights (SBH) (0.64 eV for electrons, 0.46 eV for holes) the transistor works at high applying voltages. Schottky barrier lowering or modified

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device structure have been investigated to improve the transistor performance.

In our previous studies [4,5], a poly-Si gate with a very large overlap to the source/drain was used. In this paper we present results of SB-MOSFETs with a spacer gate which provides a very small overlap between the gate and source/drain. Using the spacer gate as a mask, we can dope the source by ion implantation into CoSi_2 layer and subsequent out-diffusion to form a shallow junction.

2. Device fabrication

First, we have grown a high quality single crystalline CoSi_2 layer with a thickness of 20 nm on Si (100) (with a resistivity $>1000 \Omega\cdot\text{cm}$) or on an SOI substrate by molecular beam allotaxy (MBA) [6]. The MBA process involves growth of a silicon buffer layer resulting in a final SOI-layer thickness of ~ 54 nm under the 20 nm CoSi_2 layer. Then ion implantation of boron and annealing were performed yielding a moderate substrate doping of about $5 \times 10^{16} \text{ cm}^{-3}$. The following device fabrication process on an SOI substrate is sketched in Fig. 1. The process on bulk Si (100) substrate is similar.

First, the device area was defined by patterning of the silicide using wet etching. Reactive ion etching

(RIE) was then performed to etch back the SOI-layer to isolate the individual devices (Fig. 1a) (or etching back a thin Si layer to the bulk Si substrate). Then 20 nm SiO_2 and 300 nm Si_3N_4 were deposited using PECVD and patterned along the $\langle 110 \rangle$ direction of the substrate as shown in Fig. 1b. In the next step rapid thermal oxinitridation (RTON) was performed at 950°C for 1 min in pure N_2O . This is the key step in the fabrication process. During the oxidation a highly homogenous separation of the silicide layer forms near the edge of the nitride mask. This is caused by anisotropic diffusion of the Co atoms in the stress field which is induced by the nitride layer. On top of the gap a thin SiO_2 layer (~ 6 nm) is grown which acts as the gate dielectric. Due to the higher oxidation rate of CoSi_2 , a thicker oxide layer is also grown on top of the silicide. Then highly doped polysilicon is deposited using LPCVD and patterned to form the spacer gate with a contact pad (Fig. 1d).

Fig. 2 shows a scanning electron microscopy (SEM) image of a test structure for the device. The generated gap has a width of ~ 50 nm which defines the channel length. Part of the poly-Si spacer, the oxide on top of the channel region and on top of the unprotected CoSi_2 part were etched before the SEM measurement to obtain optimum SEM imaging conditions. The two separated silicide layers define the source and drain contacts. The poly-Si spacer is used

Fig. 1. SB-MOSFET fabrication process: (a) patterning of the device area; (b) deposition and patterning of the oxidation mask; (c) silicide patterning during RTON; (d) deposition and patterning of the poly-Si gate; (e) metallization of source, drain and gate.

Fig. 2. SEM micrograph of the device structure showing the 50 nm channel length and the poly-Si spacer gate.

as the gate. After passivation of the device with PECVD SiO_2 , contact holes were made by RIE to contact the gate pad, and the two separated silicide parts which act as source and drain. The electrodes were metallized with a 20 nm Ti/300 nm Al stack using the lift-off technique. The final device structure is shown in Fig. 1e. All patterning steps, apart from the nanopatterning step, are performed using conventional optical lithography to generate μm -structures.

3. Device characterizations

The MBA grown epitaxial CoSi_2 forms excellent Schottky barriers on moderately doped silicon with SBH values of 0.64 eV for electrons and 0.46 eV for holes. Because of a mid-gap Schottky barrier of CoSi_2 on Si, the CoSi_2 Schottky source/drain MOSFET can be operated in both inversion and accumulation modes [4,5].

Fig. 3 shows the I–V characteristics of n-channel SB-MOSFETs fabricated on (a) a Si (100) substrate and (b) an SOI substrate in inversion mode. They show typical SB-MOSFET behavior. The drain current increases slowly at low drain-source bias because the electrons cannot pass the Schottky barrier. As soon as the electrons overcome the barrier, normal transistor behavior is observed. The spacer contact shows similar performance compared to the previous results for SB-MOSFET on SOI with a large contact overlap [4,5]. The transistor per-

Fig. 3. I–V characteristics of the SB-MOSFETs with a channel length of 50 nm fabricated on (a) bulk Si substrate and (b) SOI substrate.

formance on the SOI substrate is improved as compared with that on the bulk Si-substrate indicated by higher driving currents. The maximum transconductances are 175 mS/mm and 80 mS/mm at $V_g = 5.5 \text{ V}$ and $V_D = 4 \text{ V}$ for devices on an SOI and on a bulk Si (100) substrate, respectively. The explanation of the difference is not clear. One possible reason is that the stress is different. From our nanopatterning process, it seems that the stress at the edge of the nitride mask is larger on an SOI substrate [7].

The relatively high threshold and saturation voltages are due to the high Schottky barriers on both n- and p-type silicon. Thus silicides with a low Schottky barrier are generally considered for

Schottky barrier MOSFETs. PtSi with a Schottky barrier Φ_p of 0.24 on p-type silicon and ErSi_{1.7} with a Schottky barrier Φ_n of 0.28 on n-type silicon were used for the fabrication of ultrashort channel length SB-MOSFETs [8,9]. SOI helps to lower the high leakage current resulting from the low barrier [9]. According to recent calculations by Knoch et al. [10], the performance of the SB-MOSFETs is highly improved by using ultra-thin SOI layers and thin oxide.

Another possibility to improve the performance of our transistor is to form a shallow n⁺p-junction at source side to avoid the high Schottky barrier. This asymmetric device structure has been reported in Ref. [11] for long channel devices. In our experiments, 10 keV $1 \times 10^{14} \text{ cm}^{-2}$ As⁺ ions were implanted into the CoSi₂ region without nitride cover after the fabrication step shown in Fig. 1d. All the implanted As⁺ ions are located in the CoSi₂ layer according to TRIM calculations. The poly-Si spacer protected the channel from As⁺ implantation. Ultra-shallow junctions can be formed by ion implantation into the CoSi₂ layer and subsequent outdiffusion of the implanted ions by annealing [12,13]. In our experiments, the n⁺p-junction was formed by outdiffusion of As from CoSi₂ at 950 °C for 1 min in N₂ after passivation of the structure with 150 nm PECVD SiO₂. Fig. 4 shows the asymmetric n-channel transistors with n⁺-source and CoSi₂ Schottky drain fabricated on (a) a bulk Si, and (b) an SOI substrate. All the processes except the shallow n⁺p-junction formation are the same as for the transistor shown in Fig. 3. The I–V curves is similar to the conventional n⁺p-junction source/drain MOSFETs except for a small drain voltage offset because of the drain-inversion n⁺-layer Schottky barrier. The driving voltages are much smaller than those transistors shown in Fig. 3. The maximum transconductance of 375 mS/mm has been obtained for the asymmetric transistor on bulk Si. The I–V curves show strong short-channel effects without saturation and large drain currents at $V_G = 0$ V. This is probably due to the non-optimized doping profiles, e.g. the channel doping is very low ($5 \times 10^{16} \text{ cm}^{-3}$) in order to keep a good Schottky contact at the drain side. Further doping optimization and ultra-shallow junctions formed by outdiffusion of ion implantation into epitaxial CoSi₂ layers need to be investigated for the improvement of devices.

Fig. 4. I–V characteristics of the asymmetric transistors with n⁺-source and Schottky drain fabricated on (a) bulk Si substrate and (b) SOI substrate.

4. Conclusions

In conclusion, a nanometer patterning method based on local oxidation of silicides has been used to fabricate 50 nm channel length MOSFETs. The patterning method uses only conventional optical lithography and standard silicon processing steps. The symmetric structure Schottky barrier MOSFETs with CoSi₂ Schottky source and drain, and the asymmetric device structure with n⁺-source and Schottky drain have been fabricated. Poly-Si spacer gates were employed for both kinds of device structures. The asymmetric transistor shows a better

performance than the symmetric Schottky source/drain device.

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