Large capacitance-voltage hysteresis loops in SiO₂ films containing Ge nanocrystals produced by ion implantation and annealing

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Metal-oxide-semiconductor structures containing Ge nanocrystals (NCs) of 3–4 nm diameter and $2 \times 10^{12} \text{ cm}^{-2}$ density are shown to exhibit capacitance-voltage hysteresis of 20.9 V, one of the largest observed in Ge-NC based nonvolatile memories. The Ge NCs were fabricated in an oxide of 30 nm thickness by ion implantation with 30 keV Ge²⁺ ions to an equivalent fluence of $1 \times 10^{16} \text{ Ge cm}^{-2}$ followed by annealing at 950 °C for 10 min. Secondary ion mass spectroscopy and transmission electron microscopy demonstrate the existence of Ge NCs whose average distance from the SiO₂/Si interface is about 6.7 nm. It is shown that the memory effect is a likely consequence of charge trapping at Ge NCs and that it is enhanced by accurately controlling the distribution of Ge NCs with respect to the Si/SiO₂ interface. © 2006 American Institute of Physics. [DOI: 10.1063/1.2175495]

Semiconductor nanocrystals (NCs) embedded in silicon oxide have attracted considerable attention due to their potential for electronic and optoelectronic device applications.^{1–4} Recently, metal-oxide-semiconductor (MOS) structures containing Ge NCs were reported to be very promising for nonvolatile memory (NVM) applications.^{5–7} For high-performance NVM, it is important to achieve long charge retention times and fast switching times. Several models have been proposed to explain charge storage in MOS structures containing Ge NCs with the two most dominant being charge storage in the Ge NCs and charge storage in defect states, with the latter generally being attributed to structural defects at the Ge NCs/SiO₂ and SiO₂/Si substrate interfaces. Indeed, Ge-NC memory structures are strongly influenced by defect states at such interfaces in addition to effects due to the NCs.^{8–11}

It has been reported that ion implantation of Ge into thin SiO₂ layers on Si wafers, followed by annealing, results in Ge accumulation at the Si/SiO₂ interface.^{12–14} Diffusion of Ge atoms during annealing can alter the interface, thereby having a significant influence on the memory characteristics of such structures.^{13–15} It has also been suggested that charge storage is more likely to occur within the NCs rather than at the NC/SiO₂ interface.¹⁶ These reports suggest that the memory effect should depend strongly on the concentration and the position of defects and/or Ge NCs. This letter reports large memory effects in MOS structures containing Ge NCs

which are strongly correlated with the position and concentration of Ge NCs at the Si/SiO₂ interface.

SiO₂ layers with 30 and 50 nm thickness were grown on *n*-type (100) Si substrates in a conventional tube furnace. The SiO₂ layers were implanted at room temperature with 3 keV Ge²⁺ (equivalent to 15 keV Ge⁺) to nominal fluences of 5.0×10^{15} and $1.0 \times 10^{16} \text{ Ge cm}^{-2}$. They were subsequently annealed at a temperature of 950 °C for 10 min in an Ar atmosphere. The peak excess Ge concentration for these implants was calculated, from transport of ions in matter (TRIM) simulation, to be around 6% and 11%, respectively.¹⁷

The density and size of Ge NCs were investigated by transmission electron microscopy (TEM) and depth profile of Ge atoms was evaluated by secondary ion mass spectroscopy (SIMS). Al electrodes with a diameter of 410 μm were deposited on the samples in vacuum for capacitance-voltage (*C-V*) measurements of MOS capacitors. The MOS structures containing Ge NCs were named (A,B), where A and B indicate oxide thickness in nm and implant fluence in cm⁻², respectively. High-frequency (1 MHz) *C-V* measurements were performed at 300 K using a Boonton 7200 capacitance meter.

Figure 1 shows *C-V* hysteresis curves for MOS structures containing Ge NCs in the oxides of 30 and 50 nm thickness together with a similar curve from a sample with no Ge NCs. The MOS capacitor with Ge NCs in a 50 nm oxide as well as the unimplanted sample shows almost no *C-V* hysteresis. However, a voltage shift of the *C-V* curve is evident in the MOS capacitors that contain Ge NCs in the 30 nm oxide. In these samples, the flatband voltage shift (ΔV_{FB}) is strongly enhanced, from 2.2 to 20.9 V, by increas-

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FIG. 1. C - V hysteresis loops of MOS structures, (a) sample ($30, 5 \times 10^{15}$), (b) sample ($30, 1.0 \times 10^{16}$), (c) sample ($50, 1.0 \times 10^{16}$), and (d) unimplanted sample (30 nm SiO_2). The numbers in the parentheses indicate the oxide thickness in nm and the implant fluence in cm^{-2} , respectively.

ing the implant fluence from 5×10^{15} to $1 \times 10^{16} \text{ cm}^{-2}$. Indeed, 20.9 V is the largest flatband voltage shift reported for Ge NCs and is almost double that of a Si-NC MOS capacitor fabricated by implantation with similar implant fluence. Hysteresis in the C - V curve can be attributed to the reversible storage of holes or electrons in the NCs and/or in defect states at the NC/SiO₂ or SiO₂/Si interfaces.¹⁶ The strong dependence of the hysteresis on the oxide thickness and the implant fluence, as shown in Fig. 1, provides some insight into these processes.

Figure 2 shows cross-sectional TEM images of Ge NCs formed in a 30 nm oxide by implantation with Ge ions to a fluence of $1 \times 10^{16} \text{ cm}^{-2}$. Figure 2(a) shows a low magnification image of the interface, highlighting the band of dark contrast located within 5–10 nm of the SiO₂/Si interface. This is attributed to a band of Ge NCs lying parallel to Si/SiO₂ interface. This is confirmed by higher resolution images which clearly show the presence of Ge NCs of approximately 3–4 nm, as indicated by circles in Fig. 2(b). The average distance of Ge NCs from the Si interface is estimated from low and high-resolution TEM images to be 6.7 nm, while the density of detectable nanocrystals is estimated from plan-view TEM images to be around $2 \times 10^{12} \text{ cm}^{-2}$. (The measured nanocrystal density is expected to be a lower limit due to the difficulty of detecting small, $\leq 1 \text{ nm}$, nanocrystals.)

SIMS measurements were performed to investigate the distribution of Ge atoms in these samples. Figure 3 shows

FIG. 3. SMS depth profiles of (a) sample ($30, 1.0 \times 10^{16}$) and (b) sample ($50, 1.0 \times 10^{16}$). (SMS yields are estimated to have an accuracy of $\pm 10\%$ and the integrated Ge yields agree within this error estimate.)

depth profiles of Ge in the direction from SiO₂ surface to Si substrate. TRIM simulations predict a peak Ge concentration at a depth of approximately 15 nm in the SiO₂ layers, ignoring sputtering effects. However, the Ge distribution is affected by annealing. For the sample with a 30 nm SiO₂ layer, three major Ge peaks are observed at 14, 28, and 35 nm from the surface and among them, the highest peak at 35 nm is actually within the Si substrate. (The oxide thickness after implantation is close to 30 nm as confirmed by TEM.) The data suggest that Ge has accumulated on both sides of the Si/SiO₂ interface, with that in the Si substrate having a concentration about four times higher than that remaining in the region of the peak projected Ge range. Significantly, the peak at 28 nm, which has a concentration around twice that remaining at the projected range, coincides with the array of Ge NCs whose average distance from the surface was confirmed by cross-sectional TEM in Fig. 2(a). Therefore, the SIMS signal at 28 nm is attributed to Ge NCs. The SIMS profiles were also confirmed using energy dispersive x-ray spectroscopy, which shows an enhanced Ge-related peak in the region very close to the Si/SiO₂ interface. The sample with 50 nm SiO₂ has two distinct Ge-related SIMS peaks, one in the region of 15–16 nm and a second at around 48 nm. In this case the peak concentration at the Si/SiO₂ interface is comparable to that remaining at the peak projected Ge range. However, no Ge NCs were observed by cross-sectional TEM in this case. (The reason for the lack of Ge NCs in this sample remains unclear. It can be speculated that the nucleation of NCs near the interface requires a threshold Ge concentration which is not achieved in the ($30, 5 \times 10^{15}$) sample due to the lower implant fluence nor in the ($50, 1.0 \times 10^{16}$) sample due to redistribution of the Ge through the thicker SiO₂ layer, but further work is required to clarify this point.)

Based on these observations the C - V hysteresis, as shown in Fig. 1, is discussed in terms of three possible contributions: (a) charge trapping at Ge nanocrystals, (b) charge trapping at implantation- and Ge-related defects within the SiO₂ or at the SiO₂/Si interface, and (c) charge trapping at

FIG. 2. Cross-sectional TEM images of sample ($30, 1.0 \times 10^{16}$).

the band offset caused by GeSi alloying in the Si substrate.

Ge nanocrystals are expected to act as charge traps and to produce significant C - V hysteresis, as previously reported.⁶ This is consistent with the fact that the largest C - V hysteresis is observed for samples (30, 1.0×10^{16}) which have clearly defined nanocrystals located 6.7 nm from the interface, while reduced hysteresis is observed for lower-fluence or thicker-oxide samples where Ge NCs were not observed. The magnitude of the trapped charge, Q , can be estimated from $Q = \Delta V \cdot C_{\text{ox}}$, where ΔV is the measured voltage shift and C_{ox} is the total oxide capacitance. For the (30, 1.0×10^{16}) sample, the measured voltage shift is 20.9 V and the oxide capacitance is 143.8 pF, giving a total trapped charge of 3.0×10^{-9} C. Assuming that this charge is trapped in the vicinity of the SiO_2/Si interface, the carrier density can be estimated to be $\sim 1.4 \times 10^{13}$ carriers cm^{-2} —a value significantly larger than the measured Ge NC density. Even allowing for the fact that the measured nanocrystal density is likely to be an under estimate of the actual density, the carrier density remains 2–5 times greater than the nanocrystal density. Therefore, either several charges are trapped at each nanocrystal or other trapping mechanisms are operative.

Defects produced within the SiO_2 or at the SiO_2/Si interface by ion implantation can also trap charge and may take the form of radiation- or Ge-related defects within the SiO_2 . For the 50 nm SiO_2 layers these defects are confined to the SiO_2 layer, whereas for the 30 nm SiO_2 layers they extend to the SiO_2/Si interface and can therefore act as effective charge traps for carriers tunneling from the Si substrate. Defects produced within the SiO_2 layers appear to have little effect on the C - V characteristics as the thick SiO_2 layers show no significant hysteresis effect. For thin layers, however, the concentration of defects produced at the SiO_2/Si interface is expected to increase with increasing implant fluence. Indeed, Fig. 1 shows significant hysteresis for the (30, 5×10^{15}) sample despite the absence of observable Ge-NCs, consistent with defect related charge trapping at the interface. It is also significant that samples implanted with Si ions and annealed under similar conditions produce poorly defined C - V characteristics (separate study by the present authors). In this case the temperature is too low for the formation of well-defined Si nanocrystals but the effect of radiation-induced defects is expected to be similar. These results suggest that Ge-related defects may play a significant role in charge trapping in the present case.

Finally, a significant amount of Ge exists within the Si substrate close to the Si/SiO_2 interface in sample (30, 1.0×10^{16}). This layer is likely in the form of a thin $\text{Si}_{1-x}\text{Ge}_x$ layer, as previously reported.¹³ Such layers can trap charge carriers (primarily holes) due to the large band offset (mainly in the valence band) between Si and $\text{Si}_{1-x}\text{Ge}_x$ and could therefore contribute to the C - V hysteresis. However, $\text{Si}_{1-x}\text{Ge}_x$ structures specifically designed to exploit this effect show much lower hysteresis (typically less than 0.5 V) than the 20.9 V reported here.¹⁸ This suggests that this effect plays only a minor role in the current study.

In summary, TEM, SIMS, and C - V profiling were employed to study the structural and electrical properties of Ge implanted MOS structures prepared from thermal oxides of 30 and 50 nm thickness by ion implantation with 30 keV

Ge^{2+} ions and subsequent thermal annealing. MOS structures containing Ge nanocrystals of about 3–4 nm diameter in the oxide of 30 nm thickness were shown to exhibit a C - V hysteresis of 20.9 V, the largest ever found in MOS structures containing Ge NCs. TEM images showed that the nanocrystals were located in the SiO_2 layer at an average distance of 6.7 nm from the SiO_2/Si interface and that they had an areal density of $2 \times 10^{12} \text{ cm}^{-2}$. SIMS depth profiling showed that Ge was redistributed throughout the SiO_2 layer and into the underlying Si substrate during annealing and confirmed the existence of a high Ge concentration in the vicinity of the nanocrystal layer. Comparison of the physical and electrical properties of the samples suggests that the large hysteresis effect results from charge trapping at Ge NCs and Ge-related defects near the SiO_2/Si interface and that the presence of Ge and the arrangement of Ge NCs with respect to the Si/SiO_2 interface play an important role in this process.

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