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Formation of nickel-based nanocrystal monolayers for nonvolatile memory applications

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A simple method for fabricating metal silicide nanocrystal layers with narrow spatial distributions is demonstrated and shown to produce structures suitable for nonvolatile memory applications. The method is based on high-temperature annealing of a sandwich structure comprised of a thin metal (Ni) film sandwiched between two silicon-rich oxide (SiO_x) layers and has the feature in which the size of the NCs can be controlled by varying the silicon concentrations in the SiO_x layers or the initial nickel film thickness. The typical nanocrystal diameters and densities are 3.6 nm and $1.2 \times 10^{12} \text{ cm}^{-2}$, respectively. Capacitance-voltage (C - V) measurements on test structures with these characteristics are shown to have C - V characteristics suitable for nonvolatile memory applications, including a C - V memory window of 11.7 V for sweep voltages between -12 V and $+12 \text{ V}$. © 2008 American Institute of Physics. [DOI: 10.1063/1.2952287]

The demand for nonvolatile memory (NVM) devices, such as memory sticks in digital cameras, is rapidly rising and as a consequence there is considerable research effort devoted to realizing devices with smaller size, faster operating speed, and larger storage capacity. One such approach is to use a floating gate transistor where the floating gate consists of discrete charge traps [nanocrystals (NCs)] instead of a continuous conducting layer as used in many conventional devices.¹

Discrete charge storage structures offer many advantages over conventional floating gate structures, including the fact that charge trapped at discrete sites is more stable than in a conventional conductive floating gate as the latter can lose trapped charge through a single leakage path in the gate oxide. As a consequence nanocrystal floating gate memory is expected to have a longer retention time than the conventional devices. The reduced susceptibility to gate oxide failure also means that devices can be scaled to smaller dimensions by reducing the tunnel oxide thickness.

The properties of NVM with floating gates based on semiconducting²⁻⁴ or metallic nanocrystals⁵⁻⁷ have been extensively studied. A comparison of these studies suggests that there are additional advantages in using metallic nanocrystals instead of semiconducting nanocrystals, namely, a reduction in spurious effects caused by traps at the nanocrystals/oxide interface and an enhancement in charge storage capacity and retention time. As a result, floating gates based on various metal nanocrystals, such as Au, Ag, Pt,⁸ and Co,⁹ have received particular attention. As metal silicides have been shown to have physical properties similar to those of pure metals¹⁰ they are also clearly worthy of investigation.

In this work, thermal annealing of a simple sandwich structure consisting of an ultrathin metal (Ni) layer sandwiched between two silicon-rich oxide layers is shown to produce a well-defined nickel-based nanocrystal layer suitable for the fabrication of a floating gate device. These struc-

tures are shown to exhibit characteristic capacitance-voltage (C - V) hysteresis suitable for nonvolatile memory applications.

Nickel-based nanocrystal monolayers were formed by thermally annealing Ni coated silicon-rich silicon oxide (SiO_x) films. SiO_x films were deposited on (100) oriented p -type silicon wafers at a substrate temperature of 300°C by plasma-enhanced chemical vapor deposition using fixed flow rates of SiH_4 and N_2O . Ultrathin Ni layers (0.3–0.8 nm) were deposited using a conventional thermal evaporation system, with sandwich structures made by alternate deposition of SiO_x and Ni layers as required. The as-deposited film composition was determined by Auger electron spectroscopy. Nucleation and growth of Ni-based NCs were achieved by thermal annealing of the sandwich structures at elevated temperature in a quartz-tube furnace using high purity nitrogen gas (99.999 %) as an ambient. The microstructure of Ni-based NCs was investigated by transmission electron microscopy (TEM) using a JEOL JEM 2010 instrument operating at 200 kV. The chemical composition of NCs was analyzed by energy dispersive x-ray spectroscopy (EDS) using an energy dispersive spectrometer attached to the TEM instrument. For the EDS analysis, the electron beam was focused to a spot as small as 1.5 nm in size.

In order to explore potential of these structures for memory applications a test structure was formed with the following layers: tunnel $\text{SiO}_2/\text{SiO}_{1.57}/\text{Ni film}/\text{SiO}_{1.57}/\text{control SiO}_2$. The tunnel and control oxide thicknesses were 5 and 7 nm, respectively, and the thicknesses of $\text{SiO}_{1.57}$ and Ni layers were 3.5 and 0.3 nm, respectively. This structure was subsequently annealed at 900°C for 1 h to form the Ni-based NCs, with the resulting structure shown in the TEM cross section of Fig. 2(a). The MOS capacitors were fabricated for C - V measurements by evaporating Al through a mask with square holes of area 0.09 mm^2 . High-frequency (1 MHz) C - V measurements were performed at 300 K using a Keithley 590 capacitance meter.

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FIG. 1. Cross-sectional TEM images of (a) sample prepared by depositing a 0.5 nm Ni layer between SiO_x layers of composition, $x=1.09$, 1.33, and 1.77. (b) Sample prepared by depositing different Ni thicknesses between SiO_x layers with $x=1.77$.

Figure 1 shows cross-sectional transmission electron microscopic (XTEM) images of SiO_x layers with various Si concentrations [Fig. 1(a)] and Ni layer thicknesses [Fig. 1(b)] after annealing at 1100 °C for 1 h. Figure 1(a) shows an XTEM image from a sample consisting of three layers in the form SiO_x/Ni/SiO_x where the composition of each SiO_x layer was varied, with $x=1.09$, $x=1.33$, and $x=1.77$. The thickness of the Ni layers was held constant at a thickness of 0.5 nm. In contrast, Fig. 1(b) shows an XTEM image of a similar structure in which the SiO_x layers had a fixed composition ($x=1.77$) and the thickness of the Ni layer was varied (0.5, 0.8, and 0.3 nm). It is clear from these images that the size of the nickel-based NCs increases with increasing Si concentration and Ni thickness, consistent with those observed in Ni-implanted SiO_x layers.¹¹ The details of average size and areal density obtained from plane-view TEM images were summarized in Table I. The spatial distribution of the nanocrystals is also much narrower in this case thereby demonstrating the efficacy of the technique for making nanocrystal floating gate structures for nonvolatile memory devices.

TABLE I. Average size, standard deviation, and areal density of Ni-based nanocrystals prepared with different Si concentration and Ni thickness.

SiO _x composition	Ni thickness (nm)	Annealing temperature (°C)	Average size (nm)	Standard deviation (nm)	Areal density (cm ⁻²)
SiO _{1.03}	0.5	1100	13.8	4.06	8.4×10^{10}
SiO _{1.33}	0.5	1100	8.7	3.36	2.0×10^{11}
SiO _{1.77}	0.5	1100	7.5	2.49	3.9×10^{11}
SiO _{1.77}	0.8	1100	11.3	3.46	1.9×10^{11}
SiO _{1.77}	0.3	1100	6.3	1.73	6.5×10^{11}

FIG. 2. (Color online) (a) High-resolution cross-sectional TEM images of a sample prepared using a SiO₂/SiO_{1.57}/Ni/SiO_{1.57}/SiO₂ structure with a Ni film of 0.3 nm thickness. (b) Plane-view TEM image of the sample. The left- and right-side insets represent the high-magnification TEM and EDS spectrum of the nanocrystal marked with a white arrow, respectively.

Figure 2(a) shows a high-resolution TEM image of a sample employed for C-V measurements. This clearly shows the formation of two well-defined Ni-based NC monolayers. The formation of such a double layer clearly results from bidirectional diffusion and trapping of Ni atoms. The size distribution of the NCs is more clearly revealed in the Fig. 2(b), which depicts a plane-view TEM image of the sample, as shown in Fig. 2(a). A lattice image (left-side inset) of the NC marked with a white arrow reveals a regular lattice structure consistent with it being a single crystal phase. The EDS data (right-side inset) show that NCs contain Si and Ni. These results support the premise that NCs are nickel silicide

FIG. 3. (Color online) C - V characteristics of MOS structures provided with the sample shown in Fig. 2: (a) with Ni-based nanocrystals and (b) without Ni-based nanocrystals.

crystallites.¹¹ The NCs are presumed to be nickel disilicide (NiSi_2) because they were formed by annealing at a temperature of 900°C where this is expected to be the stable phase.¹² Analysis of plane-view micrographs shows that the size of the NCs ranges from 2 to 6 nm, with an average diameter of 3.6 nm, and have an areal density of $1.2 \times 10^{12} \text{ cm}^{-2}$. These data are consistent with the realization of floating gate based on the nickel silicide nanocrystal monolayer.

Figure 3 shows C - V curves measured for the MOS capacitors with [Fig. 3(a)] and without [Fig. 3(b)] the Ni-based NCs. [The data shown in Fig. 3(a) were obtained from the sample shown in Fig. 2.] While the data shown in Fig. 3(b) were measured for the sample structure, as shown in Fig. 2, but without the Ni-based nanocrystals for comparison. The

gate voltage was swept from negative to positive values before being swept back from positive to negative values. Both samples exhibit hysteresis loops, indicating the presence of charge traps in the floating gate. There is clearly a distinct difference in the memory window for the two samples. For MOS structures with Ni NCs [Fig. 3(a)] the memory window increases as the sweep range of the gate voltage increases, while MOS structures without Ni NCs [Fig. 3(b)] show no significant change. For sweep voltages between -12 V and $+12 \text{ V}$ the memory window was measured to be 11.7 and 0.6 V for the samples with and without NCs, respectively. The hysteresis in Fig. 3(a) is believed to be associated with the presence of the Ni-based NCs, while the hysteresis in Fig. 3(b) is likely to be associated with defects. These results clearly indicate that the structures produced in this study have great potential for nonvolatile memory applications.

In conclusion, thermal annealing of a simple sandwich structure consisting of an ultrathin metal (Ni) layer sandwiched between two silicon-rich oxide layers was shown to produce narrow bands of nickel-based nanocrystals suitable for the fabrication of a floating gate memory device. The nanocrystal size distribution was shown to be controlled by the excess silicon concentration in the surrounding oxide layers or the thickness of Ni layer. The C - V characteristics of a test structure based on a 0.3 nm Ni film sandwiched between two $\text{SiO}_{1.57}$ layers were also explored and shown to exhibit large C - V hysteresis loops suitable for nonvolatile memory applications.

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