Temperature dependent properties of InSb and InAs nanowire field-effect transistors

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We present temperature dependent electrical measurements on InSb and InAs nanowire field-effect transistors (FETs). The FETs are fabricated from InAs/InSb heterostructure nanowires, where one complete transistor is defined within each of the two segments. Both the InSb and the InAs FETs are n-type with good current saturation and low voltage operation. The off-current for the InSb FET shows a strong temperature dependence, which we attribute to a barrier lowering due to an increased band-to-band tunneling in the drain part of the channel. © *2010 American Institute of Physics*. [doi:10.1063/1.3402760]

During the past years, much attention has been drawn to nanowire wrap-gate field-effect transistors (FETs) due to the excellent control of the channel electrostatics and good scaling properties.[1,2] Moreover, the possibility to use the nanowire technology to integrate a channel of high electron mobility semiconductor in a cheap silicon process has stimulated research.[3] In the nanowire geometry, several channel materials have been investigated, such as InAs, Si, Si/Ge, and ZnO.[4–7] Recent advances in nanowire epitaxy now also enabled the growth of high crystal quality InSb[8–10] and InAs/InSb heterostructure nanowires,[11] which are potential candidates for FETs.[12] This material has shown good low-temperature magnetotransport properties with large g-factors.[13] Here, we explore the use of InSb nanowires as nanowire FETs and in particular we study the temperature dependence of the transport. As a reference we investigate InAs nanowire transistors processed simultaneously within the same nanowires, since InAs is presently the most investigated III-V semiconductor material for nanowire FETs.

The InAs/InSb heterostructure nanowires were grown in a standard metalorganic vapor phase epitaxy reactor at a pressure of 10 kPa. The substrate temperature was set at 450 °C and the InAs nanowire segment was grown for 7 min. using trimethylindium (TMIn) and arsine (AsH_3), with molar fractions, respectively, of 4.6×10^{-6} and 3.8×10^{-4}. Then AsH_3 was switched off and trimethylantimony (TMSb) was switched on immediately with a molar fraction of 8.6×10^{-5} to grow the InSb segment for 20 min. The diameters for InAs and InSb segments were 44 ± 4 nm and 77 ± 4 nm, respectively, and the length could vary considerably depending on position on the substrate (about 700 nm for InAs and 1 μm for InSb). These nanowires have no measurable tapering or lateral growth for neither InAs nor InSb. The interface between InAs and InSb was shown previously to be nearly atomically abrupt[11] and strain is elastically relaxed within a few nanometers from the interface surface.[14] The InAs segment is quite pure wurtzite with few stacking faults, and InSb is stacking fault-free zinc blende, and could contain between 1% and 4% or As.[14,15] During growth of the InSb segments, some arsenic from the InAs segment evaporates due to the lack of As overpressure, but postgrowth high resolution transmission electron microscope (TEM) analysis, in combination with point analysis and line analysis using x-ray energy dispersive spectroscopy prove that the InAs bottom segment remain a pure binary (no antimony enrichment as a shell or InAsSb alloy formation).[15] No intentional doping was used but carbon may be incorporated from the metalorganic precursor at the low temperature used.[16,17] Typical wires after growth are shown in Fig. 1(a).

Two top-gated transistors were fabricated on each wire, one on the InSb segment and one on the InAs segment. The grown InAs/InSb heterostructure nanowires were transferred from the growth substrate to degenerately doped Si substrates with a 100-nm-thick SiO_2 capping layer. Four 140-nm-wide Ti/Au contacts with a spacing of 250 nm were defined to each nanowire by electron beam lithography such that two contacts are placed on each side of the heterostructure interface. Prior to contact metal deposition, the exposed semiconductor contact areas were briefly etched in a $(NH_4)_2S_x$ solution followed by a rinse in H_2O. A 10-nm-thick dielectric was deposited using atomic layer deposition (ALD), at a temperature of 100 °C, in a 3×3 μm^2 square on each wire, also covering the metal contacts. Two samples were fabricated, one using Al_2O_3 and one using HfO_2. Finally, 140-nm-wide Ti/Au finger gates were defined on each center part of the two transistors, such that the gate-contact

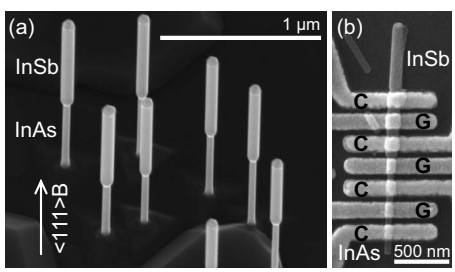

FIG. 1. (a) Scanning electron microscope (SEM) image of InAs/InSb heterostructure nanowires grown on an InAs(111)B substrate using aerosol gold particles with a diameter of 40 nm as initial seeds. The image is recorded with a 30° tilt of the substrate from the horizontal direction and the scale bar is uncompensated for the tilt. (b) SEM image of an InAs/InSb heterostructure nanowire, with one FET fabricated on each segment.

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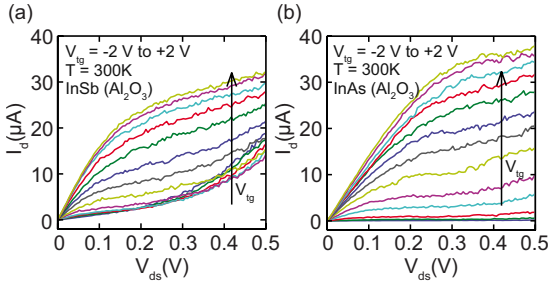

FIG. 2. (Color online) Output characteristics (I-V) of the two materials at RT, (a) InSb and (b) InAs. V_{tg}=−2 to +2 V (step +0.33 V) for Al_2O_3 gate dielectric.

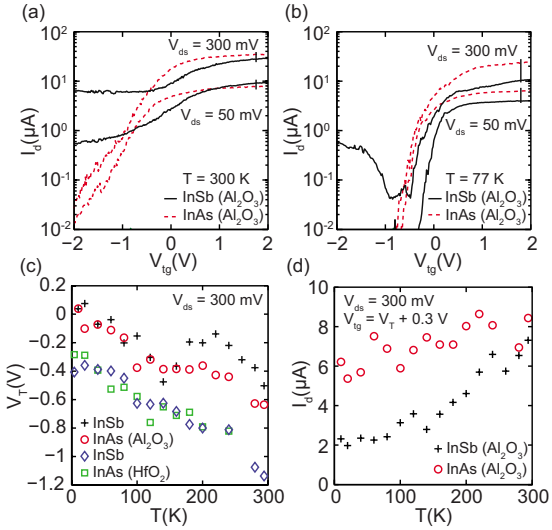

FIG. 3. (Color online) (a) Transfer characteristics at RT, V_{ds}=50 mV and 300 mV. InSb (black solid curve) and InAs (red dashed curve). (b) Transfer characteristics at 77 K, V_{ds}=50 mV and 300 mV. InSb (black solid curve) and InAs (red dashed curve). (c) Temperature dependence of the threshold voltage, V_T, in the range between RT and 4.2 K, for both Al_2O_3 (+, °) and HfO_2 (◇, □) gate dielectrics. V_{ds}=300 mV. (d) Temperature dependence of the conductance at V_g=V_T+0.3 V. InSb (+) and InAs (°), for Al_2O_3 gate dielectric.

spacing was approximately 55 nm on each side of the gate finger. In order to remove the influence of the gate-voltage on the Ohmic contacts, the gates are defined without overlap. However, this also introduces a series resistance where the source and drain extensions remain un-gated. The Ti/Au contact and gate metals were deposited using physical vapor deposition, which produce omeg-alike coverage. A transistor after fabrication is shown in Fig. 1(b).

The output characteristics (I-V) of the InSb and InAs transistors with Al_2O_3 gate dielectric at room temperature (RT), is shown in Figs. 2(a) and 2(b), respectively. During all measurements the Si substrate is kept at a fixed potential, V_{bg}=0 V. Both transistors show n-type conduction. The overall current level is slightly lower in the InSb transistor; however, the channel conductance, $g_D=dI_{ds}/dV_{ds}$ for small source-drain voltage, V_{ds}, and large top-gate voltage, V_{tg}, is higher. Both transistors show good current saturation and low voltage operation, although the InSb transistor saturates already around V_{ds}=100 mV, whereas the InAs transistor saturates around V_{ds}=200 mV. Due to the narrower band gap of InSb, the current below threshold is high as compared to the InAs reference device. We also note that, for negative V_{tg}, the current increases dramatically as V_{ds} is raised above about 300 mV, this is due to direct tunneling or impact ionization also originating from the narrow band gap of InSb.

Figures 3(a) and 3(b) displays the transfer characteristics at RT and at 77 K retrieved at V_{ds}=50 mV and V_{ds}=300 mV (Al_2O_3 dielectric). At RT the InSb (solid black curves) off-current saturates with negative V_{tg} at a large current-level around two orders of magnitude higher than the minimum observed (dashed red curves) off-current for InAs. As the temperature is lowered to 77 K the behavior of the InSb resembles more that of InAs. The InSb transistor shows ambipolar behavior for V_{ds}=300 mV. This is not observed at V_{ds}=50 mV, since it requires a V_{ds} large enough to allow band-to-band tunneling in the gate-drain region.

From the transfer characteristics, it is also possible to deduce the threshold voltage (V_T), which is shown in Fig. 3(c). This is done for temperatures in the range between RT and 4.2 K, for both Al_2O_3 (+, °) and HfO_2 (◇, □) gate dielectrics. All threshold voltages are deduced from a linear extrapolation in the transfer characteristics from the point of maximum transconductance (g_m). All devices show a similar shift in V_T toward higher V_{tg} as the temperature is decreased, however, for Al_2O_3 a plateau appears between T=100 K and T=200 K. A clear shift in V_T can also be observed when the dielectric is changed. The dielectric with the lowest permittivity (Al_2O_3) has a more positive threshold voltage, indicating a strong influence of the high-k material and its interface properties. It is further interesting to note that the threshold voltage has similar temperature dependence for the two gate dielectrics even though the channel material varies. All V_{tg} sweeps shown are recorded at a sweep direction from negative to positive voltage. As the sweep direction is reversed we observe hysteresis in I_{ds}, although of similar magnitude for the two channel materials.

Comparing the I-V characteristics for the InSb and the InAs segments we find a lower drive current for the InSb, for Al_2O_3 as well as HfO_2 dielectric, even though the diameter is larger and the threshold voltage is similar. Moreover, the InSb nanowire FET shows a larger decrease in drive current and transconductance at reduced temperatures (corrected for V_T shift) as compared to InAs, Fig. 3(d). This is partially related to a larger increase in source/drain resistance, $1/g_D$, as the temperature is reduced from RT to 77 K (6.1 to 11 kΩ for InSb and 6.9 to 8.5 kΩ for InAs). However, the increase in InSb series resistance is too low to account for the reduction in transconductance and drive current. Instead, the reduced current level may be attributed to traps at the InSb high-k interface and increased impurity scattering. Possibly the InSb/high-k interface is less perfect than the InAs/high-k interface since there are less structural defects in the InSb and good transport properties of the InSb nanowires have been verified by low-temperature measurements.[13]

Figure 4(a) shows the transfer characteristics at V_{ds}=300 mV of the InSb (Al_2O_3) segment at temperatures ranging from RT to 4.2 K. At each V_{tg} an activation energy, E_{act}, is derived from Arrhenius plots for V_{ds}=300 mV and V_{ds}=50 mV. The result is displayed in Fig. 4(b). The typical quality of the E_{act} fit is displayed as an inset in Fig. 4(b), here for V_{ds}=300 mV and V_{tg}=0 V. For V_{ds}=50 mV, E_{act} approaches the band gap of InSb, E_g=170 meV, as V_{tg} is changed to more negative values. The saturation can thus be explained by strong inversion under the gate that further

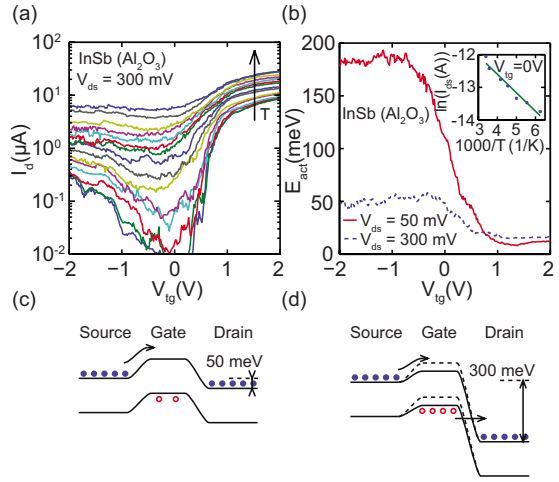

FIG. 4. (Color online) (a) Transfer characteristics of the InSb segment at temperatures ranging from RT to 4.2 K, at V_{ds}=300 mV for Al_2O_3 gate dielectric. (b) Activation energy, E_{act}, as a function of V_{tg}, for V_{ds}=50 mV (red solid curve) and 300 mV (blue dashed curve). The typical quality of the E_{act} fit is displayed as an inset, here for V_{ds}=300 mV and V_{tg}=0 V. (c) Band diagram, illustrating screening of the gate potential due to inversion under the gate. (d) Band diagram, illustrating increased screening of the gate potential due to an increased band-to-band tunneling current from the valence band in the gate region to the conduction band in the drain region.

screens the gate potential and hence the measured electron current cannot be reduced further, as illustrated in Fig. 4(c). As V_{ds} is increased to 300 mV, E_{act} saturates at a much lower value, E_{act}=50 mV. This can be explained by an increased band-to-band tunneling current from the valence band in the gate region to the conduction band in the drain region, which increases the accumulation of holes under the gate and thus increases the potential underneath the gate,[18] as illustrated in Fig. 4(d). This assignment is supported by the deduction in V_T at the two bias conditions (V_T=−0.44 V at V_{ds}=50 mV and V_T=−0.50 V at V_{ds}=300 mV) and a calculation of the characteristic length for a gate-all-around (GAA) structure using,[19]

$$\lambda = \sqrt{\frac{2\varepsilon_{wire} t_{wire}^2 \ln\left(1 + \frac{2t_{ox}}{t_{wire}}\right) + \varepsilon_{ox} t_{wire}^2}{16\varepsilon_{ox}}},$$

where t_{wire} is the wire diameter and t_{ox} is the gate oxide thickness. This gives a characteristic length λ_{InSb}=27 nm for the InSb segment, t_{InSb}=77 nm, and λ_{InAs}=16 nm for the InAs segment, t_{InAs}=44 nm. The thickness of the Al_2O_3 gate dielectric is t_{ox}=10 nm, with an estimated dielectric constant of ε_{ox}=9. From the characteristic lengths we can deduce that both transistors, in a GAA geometry, are well within the long channel regime, $L_g > 4.6\lambda$. While our omega-gated transistors have a slightly larger value of λ as compared with GAA, the used gate length of 140 nm still should be sufficiently long and the reduction in E_{act} should not be related to drain induced barrier lowering. These facts show that the observed phenomenon may not be attributed to short-channel effects. This is also supported by the InAs reference segments, where we deduced a value well above 300 meV both at V_{ds} =50 mV and at V_{ds}=300 mV. This is not surprising as the band gap is larger and hence the influence of the dynamic processes across the band gap is weaker.

Scaling of the nanowire diameter will increase the capacitance as well as the transconductance and the band gap[12] and improved doping control will reduce the negative effect of series resistance. These changes are expected to improve the device performance of the FETs toward the full potential of the InSb material system.

In conclusion, we have investigated the properties of InSb nanowire FETs and compared it to InAs nanowire FETs fabricated within the same wire. Both the InSb and the InAs FETs are n-type with good current saturation and low voltage operation.

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