Liquid Phase Epitaxy of Silicon for Thin Film Silicon Solar Cells

by

Klaus Johannes Weber

A thesis submitted for the degree of Doctor of Philosophy of the Australian National University

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Errata

p.9, section 1.5: After the sentence "...obtained by PC–1D[14]", the sentence "The cell is assumed to have negligible light trapping" should be added.

p.10, in the caption of Fig. 1.7: "... and 100% light absorption at the front surface,..." should read "... and negligible light trapping (R_{back} = 0),..."

p.11, section "Solution growth of silicon": the sentence "However, attempts to..." should read: "However, attempts to produce continuous layers on foreign substrates by means of LPE have proved largely unsuccessful"

p.12, 4th paragraph: "...temperatures is excess of..." should read "...temperatures in excess of..."

p.16, line 11: the second instance of the word "exists" should be deleted.

p.49, Eqn. 3.4: This equation is strictly valid only for the case of field–free samples, i.e. it does not apply to the LPE-grown samples of the present work, due to the doping concentration gradients in these samples.

p.62, section 4.2.1.1: The substrates used for the experiments were Osaka Titanium 0.9Ω–cm and Wacker Chemitronic SILSO (Silicon for Solar cells) 0.015Ω–cm wafers.

p.98, section 5.2.1: 100mAc m^{-2} should read 100mWcm^{-2}.

p.99, the second line following eqn. (5.2) should read:
\[ \tau_{SRH} = \tau_0, \quad \text{with } \tau_0 = 5000, \ 500 \text{ or } 50\text{ns} \]  \quad \text{(model (1))}

p.100, 2nd paragraph: "Table 1" should read "Table 5.1"

p. 106, the caption of Fig. 5.3 should read "...iv): model (2) with \( \tau_0 = 5\mu s.\)"

p.108, the missing references [27] and [28] are:

p. 110, 3rd paragraph: After the first sentence, the sentence "Due to surface recombination effects, the effective lifetimes measured by PCD are lower bounds on the carrier lifetimes." should be added.
Errata

p. 111, Section 6.2.2: The 4th sentence should be modified and a sentence added to read: "Removal of the substrate could be achieved, for example, by mechanical grinding, but the approach presents obvious difficulties since the grinding process must be cheap and since a few microns of the heavily doped substrate would have to be left untouched by the thinning process if the rear high–low junction is to be used to provide a degree of surface passivation. However, a low temperature surface passivation techniques using silicon nitride has recently been developed [1,2] which could be used to passivate the rear following removal of the entire substrate.

I certify that this thesis does not incorporate without acknowledgment, and material previously submitted for a degree or diploma in any university, and that to the best of my knowledge it does not contain any material previously published or written by another person except where due reference is made in the text. The work in this thesis is my own, except for the contributions made by others as described in the acknowledgments.

Klaus J. Weber
Acknowledgments

I would like to thank my supervisor, Dr. Andrew Blakers for his guidance and support, both academic and financial, and for the many interesting ideas and discussions during the course of this work. I would also like to thank Dr. Andres Cuevas, for his enthusiasm and willingness to provide advice, and for the discussions on many issues.

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During my PhD, I spent one month at the Institute for Crystal Growth in Berlin Germany. I would like to express my gratitude to Dr. Gunter Wagner for making this visit possible and for the financial support. He did much to make my stay in Berlin as enjoyable and interesting as possible. I also want to thank all the members of LPE group at the institute for their warm hospitality and helpfulness.

During the course of this work, much use was made of the facilities of the Department of Electronic Materials Engineering (ECV profiling, RBS, DLTS and alpha–step measurements) and the Electron Microscopy Unit (EMU) at the Research School of Biological Sciences (SEM, EDXA and EBIC). I am very grateful to these centres for the free access to their facilities. I would like to express a special thanks to the staff at the EMU, in particular Mr. Roger Heady, Mr. David Vowles and Dr. Sally Stowe for their help and training in the use of the various instruments, and to Dr. Jennifer WongLeung at EME for the RBS measurements.

Several important measurements were done outside of the University. Some of the minority carrier lifetime measurements were done by Dr. Andreas Stephens at the University of New South Wales. Dr. Wilhelm Warta of the Fraunhofer Institute for Solar Energy Research in Freiburg, Germany, carried out light beam induced current measurements on multicrystalline epitaxial solar cells. The verification of the efficiencies of some of the cells was organized by Dr. Paul Basore, then at Sandia National Laboratories. The DLTS measurements initially carried out at the ANU were verified by Drs. Andrew Leitch and Ann Conibear at the University of Port Elizabeth, South Africa. I would like to thank all these people for their time and effort.

Finally, I want to express my deepest gratitude to my parents and my wife Jennifer, for their continued interest, understanding and support.
Abstract

In this work, thin crystalline silicon films have been grown by liquid phase epitaxy (LPE) on single crystal and multicrystalline silicon substrates, with the aim of evaluating and demonstrating the potential of such films for the fabrication of high efficiency solar cells.

On single crystal silicon substrates, smooth and specular layers have been grown from In and In/Ga solutions. The layers were essentially free of extended defects and of high purity. A lower bound on the minority carrier lifetime in the layers of 10µs was established by photoconductivity decay measurements, corresponding to a diffusion length in excess of 100µm, or more than twice the thickness of the epitaxial layers. Solar cells fabricated on single crystalline epitaxial layers grown on heavily doped substrates have reached efficiencies up to 17% with an SiO₂ antireflection coating. Cells fabricated on single crystalline epitaxial layers grown on lightly doped substrates have displayed efficiencies of nearly 18% after the substrate had been completely removed.

Epitaxial layers grown on large grained, cast multicrystalline silicon substrates have shown good grain-to-grain thickness uniformity, despite the essentially random orientation of the grains in the substrates. At the grain boundaries, grooves of various depths were observed following epitaxial layer growth, and the grain boundary direction was seen to change abruptly at the substrate–epi interface. These observations could be explained by considering the energy required for atomic attachment at a grain boundary, and by the fact the the LPE method is a near equilibrium growth process, so that growth proceeds in such a way as to minimize the free energy of the epitaxial layer. It was found that the phenomenon of constitutional supercooling plays an important role in determining the surface morphology. The use of the periodic meltback technique, which consists of alternating growth and meltback cycles, resulted in significantly smoother layers, which are easier to process into solar cells. Epitaxial layers deposited on very small grained multicrystalline silicon substrates with grain sizes of the order of the film thickness or less have been found to be too rough for solar cell applications.

Photoconductivity measurements on multicrystalline epitaxial layers grown from In/Ga solutions again yielded high minority carrier lifetimes of around 10µs for all the growth conditions investigated. Solar cells on large grained multicrystalline epitaxial layers have reached efficiencies up to 15.4%, and there exists a clear potential for even higher efficiencies up to 17%.

The modelling of thin film silicon cells incorporating base drift fields revealed that, in most cases, the presence of drift fields does not result in a significant improvement of cell performance. The results also indicate that even thin film cells not incorporating any light trapping can achieve efficiencies sufficiently high to be commercially interesting, provided minority carrier lifetimes of approximately 1µs or higher can be maintained in the active layer.
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Chapter 1

Introduction

1.1 Principles of solar cell operation

Solar cells convert sunlight into electricity by exploitation of the photovoltaic effect. Fig. 1.1 shows the basic structure of a solar cell, consisting of an emitter layer made of a doped semiconductor material, an absorber or base layer made of material of opposite dopant type, and electrical contacts to the two layers. Sunlight striking the front surface of the cell is absorbed in the emitter and base layers. Photons with an energy greater than the band gap energy \( E_g \) of the semiconductor can generate an excess electron-hole pair by promoting an electron from the valence band to the conduction band, while photons with an energy less than \( E_g \) do not contribute significantly to the electrical output power of the device. Photogenerated minority carriers in the emitter and base regions must then diffuse to the p–n junction where they are swept across to the oppositely doped side by the large electric field which exists in the depletion region. To maintain electrical neutrality in the cell, electrons and holes are supplied by the metal contacts to the p type and n type semiconductor, respectively, resulting in current flow in the external circuit.

![Figure 1.1: The basic structure of an n+/p solar cell](image)

The ideal current–voltage characteristic of a p–n junction solar cell is given by the superposition of the current flowing in the cell in the dark at a bias voltage \( V \), and the current flowing in the cell under short circuit conditions, \( I_{sc} \):

\[
I = J_0 A \left( e^{qV/kT} - 1 \right) - I_{sc}
\]

Here \( J_0 \) is the dark saturation current per unit area, \( A \) is the cell area, \( q \) is the electronic charge, \( k \) is Boltzmann’s constant and \( T \) is the temperature in Kelvin. Under open circuit conditions, the current flow must be zero and the open circuit voltage is
\[ V_{oc} = \frac{kT}{q} \ln \left( \frac{I_{sc}}{J_0} A + 1 \right) \]  

The maximum power can be extracted by operating the solar cell at a particular point \((V_{mp}, I_{mp})\) on the I–V curve (fig. 1.2). An important characteristic of a solar cell is its fill factor, defined by

\[ FF = \frac{I_{mp}V_{mp}}{I_{sc}V_{oc}} \]  

The maximum solar cell output power is then simply the product of the three parameters \(I_{sc}, V_{oc}\) and FF.

![Figure 1.2: The current–voltage characteristics of a solar cell in the dark and under illumination](image)

**1.2 Solar cell design considerations**

**1.2.1 Loss mechanisms in solar cells**

The efficient conversion of sunlight into electricity places several demands on the semiconductor material and the solar cell structure. Since photons with an energy less than the semiconductor bandgap do not contribute to the generation of photocurrent in the cell, while any photon energy in excess of the bandgap is wasted, the maximum theoretical cell efficiency is a function of both the semiconductor bandgap and the spectral distribution of the sunlight. For air mass 1.5 illumination, the standard for the comparison of terrestrial PV systems, efficiencies in excess of 20% can be achieved for bandgaps in the range 1 to 2eV, with a maximum around 1.4eV [1]. Silicon, with a bandgap of 1.1eV, is thus well suited to terrestrial photovoltaic applications.
Short circuit current losses

Fig. 1.3 illustrates several loss mechanisms which may reduce solar cell efficiencies in practical devices below the theoretical limits. Photons striking a solar cell may be reflected off the top surface (1), absorbed in an electrically inactive substrate (2), or absorbed in the emitter or base layer of the cell, creating an electron–hole pair in the process (3,4). The excess minority carriers generated in this way may recombine in the bulk or at the surfaces of the semiconductor (5,6) or diffuse towards the p–n junction, where they will be swept across to the opposing side by the built-in electric field (7).

Maximization of the short circuit current requires minimization of optical losses (1,2) and electronic losses (5,6). Minimization of optical losses is achieved most easily in direct bandgap semiconductors such as GaAs or amorphous silicon, in which all photons with energy greater than the bandgap are readily absorbed within a few µm of the surface. Reflection losses from the top surface can be controlled by texturing the surface and through the use of antireflection coatings.

Minimization of electronic losses requires a sufficiently large diffusion length $L$ to enable minority carriers to diffuse to the p–n junction before recombining, where $L$ is defined as the square root of the product of the diffusion coefficient and the lifetime of the minority carrier, $L = \sqrt{D\tau}$. For minority carriers which are photogenerated at a distance $x$ from the p–n junction in a semi-infinite semiconductor, the collection efficiency is

$$f(x) = e^{-x/L} \quad (1.4)$$

For perpendicularly incident monochromatic light of absorption coefficient $\alpha$ in the semiconductor and intensity $I_0$ (photons/cm²·s), the number of electron–hole pairs photogenerated a distance $x$ into the semiconductor is equal to the rate of decay of the light intensity per unit distance:

$$G = \alpha I_0 e^{-\alpha x} \quad (1.5)$$

Under the assumption of an infinitely thin emitter, integration over the distance $x$ allows the internal quantum efficiency IQE to be obtained, defined as the ratio of the number of minority carriers which reach the junction to the total number of photogenerated minority carriers:

$$IQE = \frac{La}{La + 1} \quad (1.6)$$

Thus, for an infinitely thick base layer, efficient current collection requires that the product of the diffusion length and the absorption coefficient be much larger than one.

Silicon is an indirect bandgap semiconductor and only weakly absorbs sunlight with an energy near 1.1 eV. Efficient use of this part of the solar spectrum in a silicon cell can be achieved either through the use of an base layer several hundred microns thick and high quality silicon with very large diffusion lengths, or through the incorporation of light confinement into the device structure. The application of a reflective rear contact at the base–substrate interface and texturization of the top surface will result in sunlight being made to traverse the cell for several passes before being coupled out of the cell, thus increasing the probability of absorption within the device. The thick-
ness of the base layer may then be reduced without incurring significant current losses, and the demands on the electronic quality of the material are relaxed, since all the minority carriers are now generated closer to the p–n junction.

For cells in which the diffusion length is comparable to or greater than the base thickness, the rear surface recombination velocity significantly influences minority carrier collection. For a surface recombination velocity $S$, and with the condition $\alpha W_B >> 1$ so that none of the light reaches the rear surface, eq. (1.6) becomes [2]:

$$\text{IQE} = \frac{L_{\text{eff}} \alpha}{L_{\text{eff}} \alpha + 1}$$  \hspace{1cm} (1.7)

with $L_{\text{eff}} = L/F$ and

$$F = \frac{SL}{D} + \frac{\tanh (W_B/L)}{1 + \frac{SL}{D} \tanh (W_B/L)}$$  \hspace{1cm} (1.8)

Inspection of eqs. (1.7) and (1.8) illustrates that, as the device thickness decreases, the achievement of low surface recombination velocities becomes increasingly important for efficient carrier collection.

![Figure 1.3: Illustration of various loss mechanisms in a solar cell](image)

**Open circuit voltage and fill factor losses**

From eq. (1.2), the open circuit voltage can be seen to be only a weak function of $I_{sc}$ and $J_0$. However, $J_0$ may vary over orders of magnitude, depending on the material quality and passivation of the surfaces, and thus has a significant bearing on $V_{oc}$. $J_0$ consists of contributions from the emitter and base layers, as well as a contribution from the depletion region at the p–n junction:
The contribution to $J_0$ from the base layer is:

$$J_{0B} = q \sqrt{D \frac{n_i^2}{\sqrt{N}}} F$$

(1.10)

with $F$ as defined in eq. (1.8). Here $n_i$ is the intrinsic carrier density and is a property of the particular semiconductor, $N$ is the net dopant concentration and all parameters refer to the base layer. Analogous expressions can be written for the emitter region. For very thick base layers $W_B \gg L$ and eq. (1.8) simplifies to $F = 1$, while for $L \gg W_B$, $F \approx S \sqrt{L/D}$ and eq. (1.10) simplifies to

$$J_{0B} = \frac{q S n_i^2}{N}$$

(1.11)

In general, to achieve a low value for $J_0$, high minority carrier lifetimes and low surface recombination velocities are required. It can be seen from eqs. (1.10) and (1.11) that, as the device thickness is decreased, the importance of the surface recombination velocities increases, while that of the minority carrier lifetime decreases. Due to a generally observed decrease in minority carrier lifetime with increasing net doping concentration $N$, the value of $N$ must be optimized to achieve a low value of $J_0$ while maintaining a sufficiently large diffusion length for efficient minority carrier collection.

In the absence of significant series and shunt resistances, the fill factor is a function only of the open circuit voltage [1]:

$$FF = \frac{v_{oc} - ln \left( \frac{v_{oc} + 0.72}{v_{oc} + 1} \right)}{v_{oc}}$$

(1.12)

with $v_{oc} = V_{oc}/(kT/q)$. A larger open circuit voltage therefore leads to larger values of the fill factor.

### 1.2.2 Economic considerations

Reduction of the cost of electricity from a PV installation can be achieved through a reduction in the cost of the PV modules or through an increase in their efficiency. Currently, the great majority of the installed terrestrial PV capacity is based on crystalline (either single- or multicrystalline) silicon cells. The cost of the silicon wafer typically comprises nearly half of the cost of the finished module, and is therefore a major target for cost reductions. The cost of the PV module, in turn, is the major cost in an installed flat plate PV system. The remainder of the PV system costs is made up of balance of systems (BOS) costs. These include the cost of the land, support structures, wiring, inverters and power conditioners. Most of these costs (eg. the cost of the land, support structures and wiring) are proportional to the total area of the modules, while others are proportional to the peak power produced by the installation. The area-related BOS costs create a strong incentive for high cell efficiencies. Thus, if one module is twice as efficient as another and costs twice as much, the cost of electricity from this module will be less. As a result of these area-related BOS costs, it is generally accepted that an efficiency around 10% is the minimum efficiency for a solar module to be commercially viable, regardless of its price.
1.3 Status of solar cell technologies

Of the many materials investigated as possible candidates for terrestrial photovoltaic applications, the highest cell efficiencies have been achieved using the III–V semiconductors GaAs and InP, as well as single crystal, float–zoned silicon. The high cost of these materials (particularly of the III–Vs) has restricted their use chiefly to space applications and solar concentrator systems. For one–sun applications, several technologies have emerged as possible contenders over the past decades. Table 1.1 summarizes the highest independently confirmed cell efficiencies for the most promising materials.

Amorphous silicon has long suffered from light induced degradation caused by the Staebler–Wronski effect, causing the initial module efficiencies to fall by about 20% (relative) before stabilizing [3]. Recent designs have been able to minimize this effect; however, module efficiencies above 10% have not been achieved. Further, the potential for significant efficiency increases at the cell level seems limited.

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<tr>
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<th>a–Si</th>
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<th>CdTe</th>
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<td>Efficiency (%)</td>
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<td>12.7</td>
<td>13.9</td>
<td>15.8</td>
</tr>
<tr>
<td>Area (cm²)</td>
<td>1.0</td>
<td>1.0</td>
<td>6.64</td>
<td>1.05</td>
</tr>
<tr>
<td>Institute</td>
<td>Georgia Tech</td>
<td>Sanyo</td>
<td>NREL</td>
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Table 1.1: Terrestrial cell efficiencies under global AM1.5 spectrum illumination at 25°C [4]

While comparatively high cell efficiencies have been achieved with CdTe, module efficiencies have been only around 8%, due to the difficulty of forming a high quality n type CdTe top layer. The stability of CdTe modules has been very variable, and the mechanisms responsible for the degradation are not sufficiently understood, making it an area of significant concern. The use of highly toxic cadmium in the modules presents a potential environmental hazard, although it appears that the problem is manageable [3].

Copper indium diselenide based cells, including copper indium gallium selenide (CIGS) and copper indium gallium selenium sulfur (CIGSS) have recently achieved efficiencies up to 17.1% [3]. Further, modules tested for up to six years have shown no degradation. However, the commercial manufacture of modules has proved difficult and module efficiencies have been limited to 11%.

1.4 Multicrystalline silicon solar cells

Silicon is currently by far the most commonly used semiconductor material for terrestrial photovoltaic systems. It owes much of its success to the wealth of knowledge about the properties and processing techniques of silicon that has been gained by the integrated circuit industry over the past decades. Silicon also has the advantages over the materials listed above of relative simplicity, non–toxicity, abundance and unmatched stability. In contrast to the above materials, multicrystalline silicon is an indirect bandgap semiconductor, requiring layers several hundred microns thick.
for efficient absorption of light with near bandgap energies in the absence of light confinement. Efficient utilization of this part of the solar spectrum therefore requires large diffusion lengths (eq. (1.6)). However, a large fraction of the usable photons in the solar spectrum are absorbed within just a few microns of the incident surface (fig. 1.4). Thus, moderately efficient solar cells can still be produced with much shorter diffusion lengths.

![Figure 1.4](image)

**Figure 1.4**: The maximum silicon cell short circuit current and the absorbed solar photon fraction, as a function of base thickness under global AM1.5 illumination.

**1.4.1 Cast multicrystalline silicon**

Several different silicon casting techniques have been developed, such as electromagnetic continuous casting [5] or the various directional solidification techniques used by several producers such as Eurosolare [6] or Daido Hoxan [7]. In all these techniques, a molten column of silicon, typically 400cm² in cross section is gradually solidified under carefully controlled conditions. The melt is contained in a crucible (directional solidification) or by magnetic repulsion (continuous casting). Ingots of 200kg weight can be produced in this way. Large grain sizes with dimensions of up to several cm² can be achieved, and the minority carrier lifetimes can in some cases approach those of Czochralski–grown silicon wafers, particularly after the application of gettering procedures. Following casting, the ingot is sliced into wafers 300–500µm thick.

The chief limitation of casting techniques is the still comparatively high cost of the multicrystalline wafers as a result of the cost of the growth equipment, the relatively low growth rates (typically 1–2mm/min), the cost of wafering and the low yield, with the kerf loss amounting to approximately 50% of the ingot. Since the diffusion length is usually less than the wafer thickness.
the thickness is greater than optimal and cell efficiencies are lower than those of single crystal silicon cells.

1.4.2 Ribbon growth techniques

The direct growth of silicon sheets or ribbons from a melt has the potential to avoid the significant materials loss associated with wafering of silicon ingots, as well as enabling potentially higher growth speeds. Various techniques have been developed which involve the growth of silicon sheets with the growth direction either parallel or nearly perpendicular to the silicon sheet surface (fig. 1.5). Examples of the former are the dendritic web (D-web) and edge-defined film fed growth (EFG) processes [8, 9] in which a silicon sheet is pulled from a melt and the Silicon Sheet from Powder (SSP) method [10] involving the melting and recrystallization of silicon powder, while examples of the latter are the Supported Web (S-Web) and Ramp Assisted Foil Casting (RAFT) techniques [11, 12]. Techniques where the growth direction is perpendicular to the silicon sheet (and the pulling direction) permit the rate of solidification of material to be decoupled from the pulling speed, thus enabling very high throughput rates to be obtained in some cases. For the RAFT process, throughput rates of up to 20,000 cm²/min have been quoted.

Figure 1.5: Illustration of ribbon growth, (a) growth direction nearly perpendicular to the silicon sheet, and (b) growth direction parallel to the silicon sheet

Most of the ribbon growth processes have been abandoned due to various technical difficulties, including high defect densities and high residual stresses in the grown films caused by large temperature gradients encountered by the sheets during growth and by particle incorporation, poor shape of the films including nonuniform thicknesses and bowing, and relatively low throughput rates, particularly for techniques in which the growth direction is parallel to the sheet surface. Solar cells made on ribbon silicon have reached efficiencies greater than 16% in some cases, but the corresponding throughput rates have been low, while processes achieving high throughput rates have struggled to reach efficiencies greater than 10%.

Research into at least three of the ribbon growth techniques is continuing and at least one (the EFG process) has moved into the pilot production stage. In common with silicon wafers pro-
duced by casting, the thickness of silicon ribbon of at least 250µm is much greater than optimal for solar cells. However, recent attempts with the string ribbon method, a process similar to the D-web technique, have shown that ribbon as thin as 100µm can also be grown [13]. Small area cells with efficiencies of nearly 15% have already been produced on this material. If the demands of high throughput rates and high processing yields can be met, this approach may prove attractive.

1.5 Thin film silicon cells

Thin film silicon cells, in which the active silicon layer is much thinner than silicon ribbon or the wafers cut from cast silicon ingots, have several advantages over self-supporting silicon wafers or sheets. The amount of high-quality silicon needed per unit area may be reduced by an order of magnitude or more since the active silicon layer thickness is reduced by an equivalent amount. Also, kerf losses are avoided. Since all the minority carriers are generated closer to the p–n junction, thin film cells can be more efficient at minority carrier collection. Thus, for the same material quality, thin film cells can produce higher short circuit currents than thick cells, provided the sunlight can be effectively confined in the thin film by suitable light trapping schemes. Even in the absence of any light trapping, the optimum thickness of silicon solar cells can shift towards values well below 100µm for low lifetime material Fig. 1.7 shows the variation of short circuit current with cell thickness for a rather ideal cell with \( S=0 \) at both front and rear surfaces, obtained by PC–1D [14]. For each lifetime modelled, the short circuit current drops as the cell thickness is increased past the optimum of between 10 and 30µm, although the decrease is small. Provided the surfaces of the active regions of the device are well passivated, thin film cells also have the potential of achieving higher open circuit voltages than thick cells, due to a decrease in the bulk recombination in the device.

\[ \sim 30 \, \mu m \]

**Superstrate**

**Epitaxial layer**

**Substrate**

Reflective rear contact

Heavily doped multicrystalline silicon

**Figure 1.6**: A thin film silicon cell structure incorporating light trapping: The active silicon layer is several tens of microns thick and is passivated at the rear surface by several microns of heavily doped silicon, providing a back surface field. Light confinement is achieved by texturing the top surface and applying a reflective rear contact.
Figure 1.7: Solar cell short circuit current as a function of base thickness for a cell with perfectly passivated surfaces (S=0) and 100% light absorption at the front surface, under global AM1.5 illumination.

1.5.1 Thin film silicon cells on silicon substrates

The deposition of silicon layers directly on an existing silicon substrate has the advantages that no thermal expansion mismatch problems exist between the film and the substrate, and that the grain structure of the substrate can act as a template for the thin silicon film. Thus, if the substrate is a multicrystalline silicon wafer with reasonably large grains (of the order of 1 mm or more) then the film, if it grows epitaxially, will exhibit nearly identical grain structure. Such large grains have to date been impossible to achieve by direct silicon deposition on a foreign substrate. In principle, multicrystalline silicon can be produced relatively cheaply using suitable casting or ribbon growth techniques, especially if the purity requirements imposed on the substrate are relaxed, allowing for example the use of metallurgical grade (MG) silicon. The most significant challenge arising from deposition on silicon is the difficulty of incorporating an effective rear reflector in the device structure. This requires the removal of all of the heavily doped substrate following cell processing except for approximately 5 µm, in order to maintain a back surface field (BSF) effect at the rear surface. However, even if the heavily doped substrate is not removed, high cell efficiencies in excess of 16% can still be achieved, as is shown theoretically in chapter 5 and verified experimentally in chapter 4. Thus, the potential disadvantage of a lack of light trapping needs to be weighed against the benefit of significantly higher material quality.

1.5.2 Thin film silicon deposition and growth techniques

Vapour phase deposition of silicon

The chemical vapor deposition (CVD) of silicon has been extensively studied and is routinely used in the processing of integrated circuits. Silicon is deposited on a substrate by reduction of
a silicon containing gas, usually a chlorosilane SiH₉Cl₄₋ₓ at temperatures generally above 700°C and deposition rates up to 10µm/min. The deposition of silicon on a silicon substrate is usually carried out at temperatures above 1100°C in atmospheric pressure (APCVD) or low pressure (LPCVD) reactors. CVD layers grown on single crystal substrates can be of high quality, with minority carrier diffusion lengths well in excess of 100µm. Solar cells made on these layers have reached efficiencies above 17% while on multicrystalline substrates, efficiencies around 12% have been measured [15]. First solar cells on small grained RGS ribbons have achieved efficiencies up to 10.4% [16].

CVD silicon deposition on high temperature foreign substrates has been attempted by Chu [17, 18] and Robinson [19], who deposited silicon on steel and graphite. Due to the small grain sizes they achieved, efficiencies were low (around 1.5%). The use of low temperature substrates such as commercial glass requires deposition temperatures below 700°C. Reasonable deposition rates at these low temperatures can be achieved through the dissociation of some of the silicon containing gas in a variety of ways, such as through the use of a plasma in plasma enhanced CVD (PECVD) reactors or through the use of a hot tungsten wire in hot wire CVD (HWCVD). The layers deposited in this way are amorphous or microcrystalline, with grain sizes of the order of 1µm [20]. The deposition of silicon by CVD has several disadvantages, including the high deposition temperatures required to achieve large grain sizes, the cost and complexity of the deposition equipment and the cost of the silane gases.

The physical vapor deposition of silicon onto a variety of foreign substrates has to date not produced films of sufficient quality for solar cell production. Current attempts involving ion assisted deposition has resulted in grain sizes below 2µm, while single crystal epitaxial solar cells have displayed open circuit voltages up to 580mV [21].

Solution growth of silicon

The deposition of silicon from a solution has the advantages that the deposition equipment is relatively simple and inexpensive and that usually no toxic chemicals are involved. Silicon is first dissolved in a suitable metal solvent such as indium or tin at temperatures usually between 500 and 1100°C, and subsequently redeposited on a suitable substrate by cooling of the saturated melt. Layers deposited by liquid phase epitaxy (LPE) have resulted in cell efficiencies around 15% on single crystal substrates [22] and around 12% on multicrystalline substrates [15]. Due to the lower deposition temperatures, the diffusion of impurities from the substrate into the epitaxial layers is reduced compared to the CVD process. However, attempts to produce continuous layers on foreign substrates have proved largely unsuccessful. The use of a silicon seeding layer appears to be a necessary prerequisite. Solution growth of silicon is described in more detail in chapter 2.

Recrystallization

The comparatively small grain size of silicon films deposited on foreign substrates can be considerably improved by post deposition recrystallization processes. In the zone melting recryst-
tallization (ZMR) process, the amorphous or microcrystalline silicon films are scanned by strip heaters, resulting in narrow bands of molten silicon. Through accurate control of the heating power and scanning speed, grains up to several mm wide and several cm long can be realized. The use of capping layers is frequently necessary to prevent balling up of the molten silicon. Ishihara et al. [23] recrystallized a-Si layers deposited on oxidized silicon wafers and subsequently grew 60µm of Si by CVD. Cell efficiencies up to 16% were achieved. ZMR of a-Si films on graphite substrates, using halogen lamp heaters or electron irradiation is also under investigation [24,25].

Due to the high temperatures (>1414°C) required to melt crystalline silicon, low temperature substrates appear unsuitable for a melt recrystallization process. However, a-Si has a melting point several hundred Kelvin lower than that of crystalline silicon. This fact may be exploited by rapidly heating a-Si layers above their melting point (but below the melting point of c-Si) and allowing them to recrystallize rapidly. If crystallization times are short enough (below 1ms), glass substrates can be used. Individual grain sizes in excess of 10µm have been realized in layers up to 300nm thick[26]. However, the process requires heating rates in excess of 10^6 K/s, which can only be achieved with pulsed lasers.

Attempts at solid phase recrystallization (SPC) of a-Si layers have yielded polycrystalline layers with grain size below 1µm. While efficiencies of 9.2% have been reported for heterostructure a-Si/µc-Si cells, no cells were reported on the recrystallized silicon.

ZMR appears a promising technique for the production of c-Si seed layers with suitably large grain sizes on which epitaxial layer can then be grown, from the liquid or vapor phase. However, the cost involved, the generally low speed of recrystallization and the requirement for a low cost substrate capable of withstanding temperatures is excess of the melting point of silicon, still present major challenges for the process.

1.6 Purpose of the thesis

Thin film silicon cells have several important advantages over current cells produced on thick wafers and are a strong contender to dominate the future PV market. The development of suitable thin film deposition techniques is therefore of importance for photovoltaics. The liquid phase epitaxy process is one of the most promising thin film deposition techniques currently available, having already demonstrated considerable potential for photovoltaic applications.

The purpose of this thesis was to investigate the growth of silicon by LPE on single crystal and multicrystalline silicon substrates. LPE on low cost silicon substrates has the potential for the production of high efficiency, low cost solar cells, while avoiding the problems encountered during growth on foreign substrates. Specifically, the aims of the work were:

i) The investigation of the structural, compositional, morphological and electronic properties of the epitaxial films, as well as the influence of the growth conditions on these properties.
ii) The fabrication and characterisation of solar cells on the epitaxial layers, and the demonstration of high cell efficiencies.

iii) The modelling of various thin film solar cell structures, in order to determine the influence of electric 'drift fields' in the base of these cells on the cell performance, and to determine the range of optimal cell parameters as a function of cell structure and material quality.

Chapter 2 reviews the process of liquid phase epitaxy of silicon. Chapter 3 describes the results of experiments carried out on single crystal silicon substrates, including the fabrication and characterization of solar cells. The experiments carried out on various types of multicrystalline silicon are discussed in chapter 4, while the results of modelling of thin film silicon cells by PC–1D are summarized and discussed in chapter 5. Chapter 6 provides a summary of the work described in this thesis and outlines possible directions for future work.

1.7 References


Chapter 2

The Liquid Phase Epitaxy Growth Process

2.1 The principle of liquid phase epitaxy

Liquid phase epitaxy (LPE) involves the growth of crystals from the liquid phase. The process makes use of the limited solubility of many substances in suitable solvents, at temperatures well below the melting point of the pure substance. The growth process can usually be divided into two steps:

i) Saturation of the solvent with the solute, and

ii) Crystallization of the solute from the solvent, on an appropriate substrate

The processes are illustrated in figure 2.1 with the aid of the eutectic phase diagram of two components, A and B. The region labelled L is a liquid phase while region α is a solid phase comprised of component A saturated with component B. Similarly, region β is a solid phase comprised of component B saturated with component A. The solidus (s) and liquidus (l) curves indicate the temperature dependence of the solubility of the components in the solid and liquid phases, respectively. The minimum temperature of the liquidus curve occurs at the eutectic point E, with composition $X_e$. This is the lowest temperature at which a mixture of A and B will be molten.

![Figure 2.1: Binary eutectic phase diagram for the system A–B.](image)

In order to dissolve and recrystallize component B using solvent A, B is brought in contact with A and heated to a temperature $T_0$. Dissolution of B will occur until the composition of the liquid phase is $X_{0l}$, and the solvent is saturated with component B. Subsequent cooling below temperature $T_0$ results in supersaturation of the melt with B. The β phase will begin freezing, with com-
position $X_0$, at temperature $T_0$ and composition $X_1$ at temperature $T_1$. In the presence of a suitable crystal template, epitaxial growth of phase $\beta$ on the seed may take place.

### 2.2 Crystal growth from solution

In the presence of a crystalline seed of the phase to be crystallized out of solution, growth can be said to proceed by heterogeneous nucleation, once supersaturation of the melt has been established. The mechanism of crystal growth can be divided into two steps [1,2]:

i) Diffusion of solute to the growing interface

ii) Incorporation of solute atoms into the crystal lattice.

Figure 2.2 shows the region near the solid–solution interface of a growing crystal. It is often a useful approximation to assume that the bulk of the melt is perfectly stirred and thus homogeneous, while near the interface there exists a thin stagnant film exists across which the transport of solute is governed by diffusion. The rate of mass flow across the stagnant film per unit area is given by:

$$\frac{dm}{dt} = \frac{D}{\delta}(C-C_i) = k_d(C-C_i)$$  \hspace{1cm} (2.1)

where $C$ and $C_i$ are the solute concentrations at the two boundaries of the stagnant film, $D$ is the diffusion coefficient of the solute, $\delta$ is the thickness of the stagnant film and $k_d = D/\delta$ is a mass transfer coefficient. Away from the boundary film, mass transport may occur by free or forced convection as well as diffusion.

Solute atoms which cross the stagnant film are eventually incorporated into the crystal lattice. A useful approach to describe this process is based on adsorption layer theories. The solute atoms crossing the stagnant film are not immediately incorporated into the crystal but are adsorbed and form a thin surface layer (adsorption layer). Atoms in this surface layer can migrate relatively freely across the crystal surface, finding the most favorable site for incorporation into the crystal lattice. The incorporation of atoms into the crystal is governed by a kinetic equation which may be written as:

$$\frac{dm}{dt} = k_r(C_r-C^*)^n$$  \hspace{1cm} (2.2)

where $k_r$ is a rate constant for the surface reaction, $C^*$ is the equilibrium concentration of the solute and $n$ is the order of the reaction.

Often, one of the processes will be much slower than the other and will therefore be the rate limiting step in the growth process. For the case of rapid interfacial kinetics and with $n = 1$, $k_r \gg k_d$ and therefore $C_i \approx C^*$. Growth then occurs in a diffusion limited regime. On the other hand if diffusion is rapid compared to interfacial kinetics then $k_d \gg k_r$, $C_i \approx C$ and growth occurs in a kinetically limited regime.
The most favorable sites for attachment on a crystal surface are those sites which result in the greatest loss of energy of the growth unit. Generally this corresponds to the site where the growth unit can form the greatest number of atomic bonds.

Figure 2.3 shows a growing crystal surface where the growth units are represented by cubes. Three different sites for attachment can be identified, namely flat faces (F), steps (S) and kinks (K). Attachment will be easiest at a kink, since here the greatest number of bonds are formed. Next easiest will be attachment at a step, requiring one dimensional nucleation. Growth on a flat face requires two-dimensional nucleation and usually very high amounts of supersaturation. Thus, F faces are the slowest growing planes and often dominate the crystal morphology. A useful model for the classification of planes into F, S and K faces is the periodic bond chain (PBC) model of Hartmann and Perdok [3]. Uninterrupted chains which contain crystal growth units strongly bonded to each other are designated as periodic bond chains. For silicon the PBC vectors run in the <110> directions. Planes containing at least 2 PBC vectors within a layer of thickness $d_{hkl}$, the interplanar distance, are F planes, corresponding to the $\{111\}$ planes of silicon. S planes contain one PBC vector, while K planes contain none.
2.3 Choice of solvent for silicon epitaxy

For the specific purpose of the growth of silicon for photovoltaic applications, several demands are made on the solvent which restrict the solvent choice.

- **Silicon solubility**: Due to the low absorption coefficient of silicon in the visible and infra-red spectrum, the active layer of thin film silicon solar cells will require a thickness greater than 10 µm [4]. The silicon solubility in the solvent, or more importantly the change in silicon solubility over the temperature range used during growth, must be sufficient to enable the growth of the active layer in reasonable time. The solubility change over the growth temperature range should thus be at least around 0.5 atomic percent.

- **Epitaxial layer purity**: Although the demands on the electronic quality (in particular the minority carrier lifetime) of thin film silicon cells are reduced compared to thick cells, the achievement of high efficiencies still requires silicon of high quality. Minority carrier lifetimes in the range of microseconds are desirable. During the process of LPE, solvent atoms are incorporated into the crystal lattice at close to their solubility limit at the growth temperature. Their incorporation can influence the electronic properties of the epitaxial layer in several ways. Many metallic impurities such as gold act as efficient recombination centers in silicon and reduce the lifetime of minority carriers when present in very low concentrations. Incorporation of such impurities must be kept below levels which will seriously degrade solar cell performance. The impurity levels which can be tolerated in solar cells are fairly well known [5]. Elements such as Al or Sb on the other hand, form acceptor or donor levels in silicon respectively. Their high solid solubility at the growth temperatures results in layers which are too heavily doped to be used for the absorber layer of solar cells, although they could be used to grow the emitter layers of p+n or n+p solar cells, or to grow the heavily doped region of a BSF solar cell. Sn is an isoelectronic impurity in silicon and does not lead to the formation of either shallow acceptor or donor levels, or deep recombination centers. However, due to its high solid solubility in silicon (above $5 \times 10^{19} \text{cm}^{-3}$) and large atomic size, silicon layers grown from Sn have a significantly larger lattice constant than pure silicon, giving rise to the generation of misfit dislocations at the interface between the substrate and the epitaxial layer. The electronic quality of these layers is significantly lower than that of unstrained layers.

- **Formation of silicides**: Many metals, such as Cu, form silicides at sufficiently low temperatures and the appearance of these phases must be avoided.

- **Vapor pressure of the solvent**: A low vapor pressure of the solvent in the projected growth temperature range is desirable in order to prevent excessive loss of solvent during growth.

- **Toxicity of the solvent and its compounds**: Metals such as Pb which are highly toxic, and/or which can react to form toxic compounds during LPE, should be avoided where possible.

Several solvents have been studied for LPE of silicon, including Bi [6], In [6–19], Sn [17,18,20–28], Sb [6], Ga [10,29–32], Al [30,33], Cu [34] as well as their alloys [35–37].
solvents which appear promising for LPE of silicon for photovoltaic devices are In, Ga, Sn, Cu and Al. Table 2.1 summarizes the silicon solubilities as well as the solid solubilities of these metals in silicon at 800 and 1000°C. Silicon grown from Al or Ga melt is too heavily doped to be used as the absorber layer in solar cells. However, silicon grown from alloys such as In/Ga [37], Sn/Al [37], or Cu/Al [36] may have sufficiently low doping levels for this purpose.

<table>
<thead>
<tr>
<th></th>
<th>Silicon solubility at 800°C (atomic %)</th>
<th>Silicon solubility at 1000°C (atomic %)</th>
<th>Solid solubility at 800°C (cm⁻³)</th>
<th>Solid solubility at 1000°C (cm⁻³)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In [6]</td>
<td>0.38</td>
<td>1.9</td>
<td>$3 \times 10^{15}$</td>
<td>$8 \times 10^{16}$</td>
</tr>
<tr>
<td>Ga [6, 38]</td>
<td>3.9</td>
<td>12</td>
<td>$1.5 \times 10^{19}$</td>
<td>$3 \times 10^{19}$</td>
</tr>
<tr>
<td>Sn [6, 38]</td>
<td>0.62</td>
<td>2.5</td>
<td>$3 \times 10^{19}$</td>
<td>$4 \times 10^{19}$</td>
</tr>
<tr>
<td>Al [38, 39]</td>
<td>27</td>
<td>44</td>
<td>$1 \times 10^{19}$</td>
<td>$2 \times 10^{19}$</td>
</tr>
<tr>
<td>Cu [38, 39]</td>
<td>30*</td>
<td>43</td>
<td>$4 \times 10^{16}$</td>
<td>$3 \times 10^{17}$</td>
</tr>
</tbody>
</table>

* At the eutectic temperature of 802°C

Table 2.1: Silicon solubilities and solid solubilities of various metals at 800 and 1000°C.

2.4 Choice of substrate

2.4.1 Epitaxy of silicon on silicon substrates

Silicon LPE experiments on single crystalline silicon wafers have been motivated chiefly by the potential application of the process in the areas of microelectronics and photovoltaics. Some of the earliest work was carried out by Kim [20], Girault et al. [30] and Sumner and Foley [32]. The first solar cells on silicon LPE layers were reported by Ito [31,33] who measured cell efficiencies of 9.0% and 10.4% using Al and Ga as solvents, respectively. Epitaxial layers grown on dislocation-free substrates have been found to be essentially free of extended defects, provided a clean substrate surface, free of oxide remnants and other surface contaminants, can be obtained. The majority carrier mobilities have been measured in epitaxial layers grown from a number of solvent systems, such as Sn/Al, Sn/Ga, In/Ga and In/As [9,37] and have generally been found to lie within the range of values observed in bulk-grown single crystal silicon of the same doping level. Solar cells with efficiencies above 14% and with high open circuit voltages have been realized on epitaxial layers grown on heavily doped substrates [12,13,40,41]. In these cells, the substrates were sufficiently heavily doped as to be electrically virtually inactive and not contribute significantly to the high cell efficiencies. Measurements of the minority carrier lifetimes and diffusion lengths in LPE grown silicon have shown the lifetimes to be in the microsecond range [13,22,36,42]. These results have demonstrated the feasibility of processing high efficiency solar cells on silicon films grown by LPE.

The cost of single crystal silicon wafers is too high for them to be used in a low-cost solar cell process. However, multicrystalline silicon may be sufficiently cheap for this purpose. Silicon
LPE on multicrystalline silicon is very similar to LPE on single crystal silicon, with the following differences:

i) Multicrystalline silicon contains grains of different crystallographic orientations. Depending on the growth method, multicrystalline silicon may or may not exhibit a preferred grain orientation. The growth kinetics will be slightly different for every grain orientation, leading to possibly different growth velocities and inhomogeneous epitaxial layers.

ii) The grain boundary regions in multicrystalline silicon are regions with electrical and structural properties very different from those of silicon crystal, leading to different growth kinetics. The significance of these regions increases as the grain size of the multicrystalline substrates decreases.

iii) The defect density and impurity concentrations in multicrystalline silicon are significantly higher than in monocrystalline silicon. Impurities may diffuse into the epitaxial layer, while defects may propagate into it, decreasing its electronic quality in both cases.

LPE of silicon on multicrystalline substrates was reported briefly in [30,46]. These authors noted that the grain structure of the epitaxial layer replicates that of the substrate. More recent studies have demonstrated the feasibility of this process for the fabrication of solar cells [43–45]. An open circuit voltage of 643mV was reported for a solar cell on a multicrystalline epitaxial layer grown by LPE [45], a record at the time for a multicrystalline silicon solar cell.

2.4.2 Epitaxial lateral overgrowth (ELO)

ELO of oxidized silicon through windows opened in the oxide has been investigated chiefly due to the interest in three-dimensional integration of semiconductor circuits, although the process is also of potential interest for solar cell fabrication. Fig. 2.4 shows overgrowth of an oxidized, (100) oriented silicon wafer. The oxide has the advantage that it can act as an optical rear surface reflector, thus eliminating the need for substrate removal after cell processing, in order to obtain good light trapping in the cell structure [46]. An important number characterizing ELO is the aspect ratio, defined as the lateral to vertical overgrowth ratio of silicon over the oxide [47]. For effective light trapping, the fraction of unoxidised silicon substrate should be small and therefore the aspect ratio should be large. Aspect ratios of 40:1 are possible on near – (111) oriented wafers, while on (100) surfaces only √2:1 is achieved [47]. The coalescence of silicon layers from different seeding windows is difficult and frequently results in metallic inclusions [7, 48].

An interesting approach to the achievement of larger aspect ratios on arbitrarily oriented substrates is based on the use of very thin solutions. Leamy and Doherty [49], for example, deposited 0.5µm Si followed by several µm Al on an oxidized, (100) oriented Si wafer containing via holes. Following heating of the sample to 720°C and cooling to room temperature, the silicon was observed to have overgrown the oxide near the via holes. The thickness of the silicon layer was between 0 and 15µm and was determined by the thickness of the Al melt. However, due to the limited amount of silicon, continuous overgrowth could not be achieved with this technique.
Figure 2.4: Cross sectional view of the overgrowth of an oxidised (100) oriented silicon wafer through a window. The development of (111) faces results in a triangular cross section and a low aspect ratio. After Bergmann [47].

2.4.3 Deposition of silicon on foreign substrates

Deposition of silicon from the liquid phase onto foreign substrates is attractive for photovoltaic applications, due to the many possible low cost substrates available and, in some cases, the ease of incorporation of effective light trapping into solar cells processed on the thin silicon films. However, the deposition of silicon on foreign substrates introduces several difficulties. Due to the absence of a crystal template, crystallites of different orientations will nucleate on the substrate, giving rise to small grained polycrystalline layers after the silicon islands have impinged to produce a continuous film. Further, there are several requirements which the substrate must meet for photovoltaic applications, including a thermal expansion coefficient matched to that of Si in order to avoid the creation of stresses or cracking of the epitaxial film, and sufficient purity to avoid contamination of the epitaxial layer.

Deposition on low temperature substrates

Several authors have investigated solution growth of silicon on glass substrates. Glass has the advantages that it is cheap, and mechanically and chemically stable. Since it is transparent it can be used as the superstrate or the substrate of a solar cell, or possibly both. Shi et al. [50] investigated several approaches in order to achieve continuous layer coverage and reasonable grain sizes. A borosilicate glass with a thermal expansion coefficient similar to that of silicon was used in these experiments. Deposition of a 1µm thick a–Si layer on the glass surface prior to LPE resulted in continuous silicon films. However, the average grain size was small (around 50µm) due to a high nucleation density effected by the a–Si film.

Better results were achieved by growing on bare glass substrates near the softening point of glass (rheotaxy) which resulted in grain sizes up to 350µm and a preferred (110) orientation of the grains. The improved results were explained by a higher nucleation density at the higher growth temperatures and the greater mobility of the crystallites on the liquid-like substrate surface during the initial stages of growth at the highest temperatures. The greater mobility allows the movement
of the crystallites on the surface and their realignment with respect to each other, in order to decrease
the overall free energy of the layer [51]. The layers were found to be very rough due to the different
growth rates of the crystals with different orientations. Further improvements were obtained by the
use of the periodic regrowth technique whereby, after an initial deposition of a silicon film, the film
is alternately etched and regrown, with the amount of regrowth in each cycle being always greater
than the amount of etchback [52]. With this technique, the layer smoothness could be improved and
the average grain size increased. Despite these achievements, the fabrication of solar cells with rea­
tion efficiencies on silicon films grown on glass has not been realized to date, due to the still
relatively poor material quality, as well as the difficulty in finding a suitable low-temperature cell
process.

Deposition on high temperature substrates

Deposition of silicon on high-temperature substrates has yielded some more promising re­
sults, many of which have been summarized in [53]. A process of solution growth of silicon on a
ceramic substrate has been developed by the company Astropower. The highest reported efficiency
with this process was 14.9% on a 1cm² cell [54]. Lee et al. [55] and Bergmann et al. [56] investi­
gated the use of a liquid intermediate layer by evaporating Al and Si onto quartz and glass substrates
substrates prior to growth. Improved wetting of the substrate and very large grain sizes were ob­
tained. However, it was not possible to obtain continuous silicon films with this method. Further,
growth on quartz led to cracking of the films due to the much lower thermal expansion coefficient
of quartz, compared to silicon. Another concept which has been explored with limited success is
the growth of silicon on substrates with microrelief structures (graphoepitaxy). Microrelief struc­
tures can result in preferred orientations of the nucleating grains by providing favorable nucleation
sites for crystals of certain orientations or by inducing reorientation of mobile crystals during the
growth process. While the presence of microrelief structures was found to have a marked effect on
the size and orientation of the grown crystals [51,57], continuous epitaxial layers were not
achieved. The exact mechanisms responsible in each case for the growth of crystals of certain
orientations are not completely understood [51].

2.5 LPE growth apparatus and growth techniques

The LPE growth process requires supersaturation of the solvent with the solute, in order to
provide a driving force for growth. This supersaturation can be achieved in various ways:

i) Cooling of a saturated melt (transient growth)

ii) Establishment of a temperature gradient between a silicon source and substrate

iii) Exploitation of solutal gradients in the melt

iv) The use of a source with a higher chemical potential than the substrate

Growth by cooling of a saturated melt can be carried out through the use of a slider boat [2],
a tipping boat [58], a dipping system [35] or a centrifuge [59]. The slider boat and the centrifugal

22
systems have the advantage that more than one layer can be grown in a single run, thus enabling the growth of multilayer structures. Fig. 2.5 illustrates several possible growth schemes. For the equilibrium cooling process, the saturated melt is brought into contact with the substrate and is then cooled, usually at a constant rate of $R^\circ C/min$. Growth is terminated at temperature $T_1$ by removing the substrate from the melt. For step cooling, the melt is removed from the source and supersaturated by $\Delta T^\circ C$. The supersaturated melt is contacted with the substrate and growth occurs until equilibrium has been reestablished at the temperature $T_h - \Delta T$. Supercooling is a combination of the above techniques, where the melt is supersaturated by $\Delta T^\circ C$ as for step cooling. Upon contact with the substrate, the melt is further cooled at a rate of $R^\circ C/min$. For all of the above methods, the amount of epitaxial material that can be grown is limited by the amount of solute which can be dissolved in the solvent at the saturation temperature, $T_h$.

**Figure. 2.5:** Possible growth schemes for liquid phase epitaxial growth by cooling of the melt

Fig. 2.6 illustrates the growth process utilizing a temperature gradient. The temperature of the source wafer is kept above that of the substrate, resulting in a solute concentration gradient in the solution. The solute is transported toward the substrate by diffusion and convection. Long et al. [60] investigated several temperature gradient systems for the growth of GaAs. They were able to obtain thick epitaxial layers; however, the thickness uniformity was found to be significantly poorer than for epitaxial layers obtained by a transient growth technique. The thickness nonuniformity was attributed to convection in the melt, arising primarily from the solutal concentration gradients. Scott and Hager [61] applied a vertical temperature gradient system to the growth of Si from In solution at high temperatures (900–1300°C), using columns of In of several cm in height. The obtained growth rates were found to correlate well with calculations which assumed only diffusive transport of silicon, particularly at the lower growth temperatures. However, growth rates be-
low 1000°C were low (< 200µm/day). Balyuk and Popov [62] and Popov et al. [63] studied the growth of Si from Al melts for both horizontal and vertical source—solution—substrate arrangements, with the temperature gradients applied perpendicular to the wafers. The thickness of the solution columns used was up to 100µm. Growth rates as high as 100µm/hr were obtained, by effectively utilizing the convective flows in the melt to aid transport of silicon to the substrate. Peter et al. [64] also obtained growth rates around 100µm/hr using a process temperature of only 900°C and Sn as a solvent. Again, it is likely that convection played a critical role in obtaining the high growth rates observed. Thickness nonuniformity of the epitaxial layers may be a major problem with temperature gradient solution growth, particularly if convective flows are present in the melt.

Convective flows in the melt of a source—solution—substrate sandwich may be established in the absence of temperature gradients. This effect has been utilized for the epitaxial growth of silicon by Sukegawa and coworkers [14,15,18,19]. Fig. 2.7 shows the solutal gradients that develop during heating (dissolution) and cooling (growth) of an initially saturated melt. During heating, dissolution of the wafers results in the solution near the wafers having a higher concentration of solute and therefore a different density. For the specific case of Si ($\rho = 2.5g/cm^3$ at 1414°C) grown from In ($\rho = 6.45g/cm^3$ at 1000°C) or Sn ($\rho = 6.6g/cm^3$ at 1000°C), the density of the solution near the wafers will be lower than in the bulk. The density gradient near the top wafer will be stable while the gradient near the bottom wafer is unstable, resulting in convection currents which transport silicon upwards. As a result, the amount of silicon dissolved at the source will be greater than at the substrate. During cooling, the concentration gradients and solutal stability criteria are reversed, resulting in greater deposition of silicon on the substrate than on the source. Using cyclic temperature modulation, Sukegawa et al. were able to obtain epitaxial layers of arbitrary thickness and growth rates up to 20µm/hr [18].

Figure 2.6: Temperature gradient solution growth: (a) possible growth system using a horizontal source—solution—substrate arrangement, (b) temperature and silicon concentration gradients in the melt during growth
The difference in chemical potential between single crystal and polycrystalline or stressed crystal material can be used to establish a solute concentration gradient in the melt of a source–solution–substrate sandwich. The higher chemical potential of polycrystalline or stressed crystal sources compared to unstressed single crystals results in the creation of a supersaturated solution near the source. Losovsky and Konstantinova [65] grew single crystal epitaxial layers from polycrystalline silicon sources using Al melts up to 30µm in thickness. Growth rates over 200µm/hr were observed at temperatures below 960°C.

2.6 References


[34] T.F. Ciszek, T.H. Wang, R.W. Burrows and X. Wu, "High Temperature Solution Growth of Thin Film Crystalline Silicon Layers", in proc. 11th EC PV Specialists Conference, Montreux, Switzerland, p. 423 (1992)


Chapter 3

LPE of Silicon on Single Crystal Silicon Substrates

3.1 Introduction

This chapter describes the results of LPE experiments carried out on single crystal silicon substrates. The aim of this work was to obtain high quality epitaxial layers suitable for processing into high efficiency solar cells and to characterize the layers. The demonstration of high cell efficiencies on single crystal layers is a prerequisite to achieving high efficiencies on epitaxial layers grown on lower quality multicrystalline silicon substrates.

3.2 The LPE growth process

LPE growth was carried out in a graphite crucible using the 'tipping boat' technique, as illustrated in fig. 3.1. Initially the system is heated to the saturation temperature, typically 970°C. The solvent is then brought into contact with the source, and dissolution of the source will take place until the solvent is saturated with silicon. A period of 1 hour has been found to be sufficient for this purpose. Following saturation, the melt is supersaturated by tipping the solvent back into the centre of the crucible and reducing the furnace temperature by 0 to 5°C. After about 5 minutes, the temperature of the system has stabilized and the solvent is brought into contact with the substrate and cooled at a rate R°C/min. Finally, growth is terminated at a temperature T₁ by tipping the solvent into the centre of the crucible and turning the furnace heating elements off.

In was selected as the solvent for the experiments, due to the superior quality of epitaxial layers grown from an In melt [1]. The substrates were (100) oriented Cz wafers (p-type, B doped 0.015Ω-cm) cleaved to a size of 3.2 × 5 cm², while 8Ω-cm B doped Cz wafers were used as silicon sources. (100) oriented silicon wafers provide a more stringent test of the successful removal of the native oxide due to the low aspect ratio, that is, the ratio of lateral to vertical growth over the oxide [2]. Pinholes in the oxide result in pyramidal growth on (100) oriented wafers; these pyramids take much longer to join up than the facets that grow on near (111) Si. Prior to insertion into the LPE chamber all wafers were cleaned as summarized in table 3.1. The wafers were pulled out of the final HF solution dry and were immediately loaded into the crucible.
Figure 3.1: The liquid phase epitaxial growth process using a tipping boat. (a) Position of the solvent during (i) heating and supersaturation, (ii) saturation and (iii) growth. (b) Temperature versus time during LPE growth. The shaded regions correspond to times when the solvent contacts either the source or substrate wafer. (c) H₂ flow rates during LPE growth.
<table>
<thead>
<tr>
<th>Solution</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>HNO₃:HF 20:1</td>
<td>10 secs (agitated)</td>
</tr>
<tr>
<td>DI water rinse</td>
<td>2 mins</td>
</tr>
<tr>
<td>H₂O:H₂O₂:NH₄OH 5:1:1 (boiling)</td>
<td>5 mins</td>
</tr>
<tr>
<td>DI water rinse</td>
<td>2 mins</td>
</tr>
<tr>
<td>H₂O:H₂O₂:HCl 5:1:1 (boiling)</td>
<td>5 mins</td>
</tr>
<tr>
<td>DI water rinse</td>
<td>2 mins</td>
</tr>
<tr>
<td>H₂O:HF 10:1</td>
<td>Approx. 10 secs (until hydrophobic)</td>
</tr>
</tbody>
</table>

Table 3.1: The standard cleaning procedure for the silicon wafers used in the LPE growth experiments

### 3.3 Achievement of epitaxial layer growth on an oxide free silicon surface

#### 3.3.1 Prerequisites for epitaxial layer growth

LPE of silicon on silicon substrates requires the existence of an oxide free surface prior to epitaxy. Due to the rapid growth of a thin oxide on bare silicon upon exposure to air, achievement of a clean surface usually requires in-situ oxide removal. This is commonly done by removing the oxide thermally at elevated temperatures. Thermal oxide removal in a vacuum in the presence of low pressures of water or oxygen has been studied by Ghidini and Smith at temperatures of 890°C and above [3,4]. The partial pressures of both oxygen and water vapor which could be tolerated while maintaining an oxide free surface were found to depend exponentially on the inverse of the absolute temperature. Thus the creation of a clean Si surface becomes significantly easier at higher temperatures. Similar dependencies were observed by Agnello and Sedgwick at temperatures between 650 and 850°C [5].

The LPE process is usually carried out at atmospheric pressure in an ultrapure hydrogen ambient in order to avoid excessive loss of solvent. Hydrogen is known to aid in the reduction of the native oxide [6], thought to occur via the reaction

\[
2\text{SiO}_2(s) \rightleftharpoons 2\text{SiO}(g) + \text{O}_2(g)
\]

Tabe [7] showed that thermal oxide removal is only successful if the oxide is relatively thin. In his experiments, he found no reduction in oxide thickness for oxide films greater than 2.5nm thick after 1 hour at 1100°C, while SiO₂ films thinner than 2.5nm could be removed at all temperatures above 800°C. Transport of SiO from the SiO₂–Si interface to the SiO₂ surface was considered the critical step in determining the etching rate of the oxide. The practical implication of these results is that the partial pressures of oxygen and water vapor must be kept below certain threshold values throughout the epitaxy process.
Two other approaches have been frequently used to obtain an oxide free silicon surface, namely the addition to the melt of a reducing agent such as Al \[2,8\], or the use of meltback of the substrate prior to epitaxy. However, these techniques have distinct disadvantages. The use of Al was found not to result in the homogeneous removal of the native oxide \[2\], while other metals which could be used to reduce the oxide, such as Mg or Ca, are undesirable due to their potentially deleterious effects on the electronic quality of the epitaxial layers \[8\]. The process of substrate meltback introduces additional surface roughness and may lead to contamination of the melt, if the substrate used is of low purity. Therefore it is desirable to achieve oxide removal prior to contacting the substrate with the melt.

### 3.3.2 LPE system design

Fig. 3.2 shows the LPE reaction chamber which was designed and constructed. High purity hydrogen is further purified at point-of-use using a zirconium based getter purifier in one system and a palladium diffusion cell in a second system. The specified outlet concentrations of O\(_2\) and H\(_2\)O for the getter purifier are less than 1 ppb. N\(_2\) from liquid N\(_2\) boiloff can be introduced to enable safe loading and unloading of the chamber in the absence of H\(_2\). Following loading, a high purity atmosphere is established by flushing the growth chamber with hydrogen for several hours prior to growth. The graphite crucibles used for LPE were machined from high purity, densified graphite.

![Figure 3.2: Schematic diagram of the LPE growth chamber. A cylindrical quartz insert increases the flow of H\(_2\) around it, thus preventing the backstreaming of desorbed gases.](image)

A problem that can be encountered during epitaxy experiments are the long flush times required to desorb reactive gasses from quartz tubes of the epitaxy systems. In their experiments, Agnello and Sedgwick \[5\], did not expose the reaction chamber to the atmosphere for several weeks to obtain suitably low partial pressures of H\(_2\)O. Particularly significant is adsorption of water vapor and oxygen traces near the extremities of the tube, especially the downstream end. During the heating cycle the tube center, where the sample and melt are located, heats up first. Desorption from the tube center occurs at relatively low furnace temperatures, while the silicon surface is still rela-
tively unreactive. However, when the extremities of the tube are warm enough for desorption to become significant there, the silicon sample is hot and its surface is much more reactive. Backflow of these desorbed gases to the tube center, where the silicon samples are located may then result in the growth of an oxide too thick for subsequent removal by conversion to volatile silicon monoxide.

The diameter of the quartz tube of the LPE growth chamber is 105mm. The hydrogen flow rate of up to 11/min used during the heating phase is insufficient to prevent backstreaming of gas from the downstream end to the center of the tube. One solution is to employ a load lock which prevents exposure of the tube to the atmosphere. A simpler and effective alternative was found to be the use of a quartz insert next to the graphite boat, as shown in fig. 3.2. The insert increases the hydrogen flow speed in its vicinity by a factor of about 5, virtually eliminating any backstreaming of desorbed gases from the downstream end of the tube to the tube center. The effectiveness of the quartz insert was evidenced by the fact that complete oxide removal was achieved with it, giving smooth and specular epitaxial layers, whereas only localized pyramidal growth through pinholes in the native oxide resulted without it. Adsorption of gases upstream of the furnace center is reduced by pinching the tube to a diameter of approximately 20mm. The overall construction of the tube minimizes the volume where gas purity is critical for oxide removal, in order to ensure rapid dilution of backstreamed air with nitrogen and then hydrogen following the closure of the chamber.

3.3.3 Baking of system components

The thorough baking of all graphite components was found to be essential for achieving epitaxial growth, in order to prevent large increases in oxygen and water vapor levels due to outgassing during the heating up of the LPE chamber prior to epitaxy. All graphite components were baked for several hours at 1000°C in an ultrapure H₂ atmosphere. Once baked, the graphite boat could be subjected to the atmosphere for periods longer than one hour without affecting epitaxy. After a period of about a day the adsorption in the graphite of oxygen and moisture had become significant, and epitaxial growth was not achieved. All graphite parts were stored in an ultra–high purity hydrogen atmosphere in the LPE chamber. It was also found necessary to bake the metal solvents used, as significant amounts of gases are released during initial heating.

3.3.4 Catalytic oxidation of silicon in the presence of indium

Indium can play a catalytic role in the oxidation of silicon. Evidence for this was obtained in a series of experiments as follows. A single wafer of silicon was placed on a quartz boat together with approximately 5g of In. When small amounts of air were allowed to enter the system (for example, through a leak) interference fringes due to the growth of an oxide were observed on the area of the wafer directly adjacent to the In melt.
The composition of the oxide was investigated by energy-dispersive X-ray analysis (EDXA) and Rutherford Backscattering (RBS). Fig. 3.3 shows the result of EDXA on an approximately 1µm thick oxide. The absence of the In Lα1 and Lβ1 lines at 3.287 and 3.487 keV respectively confirms the composition of the oxide as SiOx. Fig. 3.4 shows the results of RBS measurements on a different region of the oxide, together with a computer simulation of a 420nm thick layer of SiO_{1.8} (smooth line). Based on these results, the ratio of silicon to oxygen in the oxide is estimated to be in the range Si:O = 1:1.5 to 1:2.

Figure 3.3: EDX analysis of a 1µm thick oxide grown in the presence of In. In order to increase the surface sensitivity of the measurements, a low beam voltage of 10keV was used and the sample was tilted 45° relative to the incident beam. The sample was coated with 20nm of C prior to analysis to ensure electrical conductivity.

To quantify the In enhanced oxidation rate, the oxide thickness was determined as a function of partial water vapor pressure. Water vapor was added to the high purity H_{2} gas via a shutoff valve connected to a deionized water reservoir, as illustrated in fig. 3.5. The moisture content was measured using a Mitchell 2000 dewpoint meter. Following oxide growth, stripe patterns were etched in the oxide using standard photolithographic techniques. The thickness of the oxide was then measured using a surface profilometer. Fig. 3.6 shows the results for a 4 hour oxidation at 960°C. For
comparison, an oxidation in pyrogenic steam at 1000°C for 4 hrs would yield an oxide thickness of approximately 1µm.

**Figure 3.4**: RBS profile of an oxide grown in the presence of In. The smooth line is a computer simulation of a 420nm thick layer of SiO$_{1.8}$.

**Figure 3.5**: Incorporation of a water reservoir and a dewpoint meter into the H$_2$ line for the determination of oxide thickness as a function of H$_2$ gas moisture content.
A possible mechanism responsible for the rapid oxidation has been proposed by Hiraki [9] for the catalytic oxidation of Si by Au. According to this model, a thin film of In would exist at the Si/SiOₓ interface. Dissolution of silicon at elevated temperatures would result in an In/Si alloy in which the silicon atoms are highly mobile and easily oxidized by the oxidizing species diffusing through the oxide (fig. 3.7). Thus, In may catalyze the oxidation of Si by weakening Si–Si bonds and aiding the transport of dissolved Si to the growing SiOₓ layer. Another important mechanism in the formation of an SiO₂ layer in the Cu₃Si/Si system has been shown to be the presence of surface copper, which aids in the dissociation of molecular oxygen at the surface. It is the atomic oxygen species which then participates in the oxidation process [10]. Further work is required to determine the kinetics of silicon oxidation in the presence of In.

![Figure 3.6](image_url)  
**Figure 3.6**: Maximum oxide thickness versus partial water vapor pressure of the H₂ carrier gas for a 4 hour oxidation at 960°C.

![Figure 3.7](image_url)  
**Figure 3.7**: Model for the catalytic oxidation of silicon. Dissolution of silicon results in the presence of silicon atoms in a metallic environment; these are highly mobile and easily oxidised by the oxidising species at the oxide/alloy interface. After Hiraki [9].

---

3.4 Surface Oxidation of Si
3.4 Surface morphology

In general, the epitaxial layers on single crystal substrates were of smooth and specular appearance, and free of extended defects such as dislocations and stacking faults. Various surface features which were occasionally observed are described and discussed in the following paragraphs.

3.4.1 Formation of depressions

Fig. 3.8 shows a depression on the surface of an epitaxial layer. The cause of the depression was established to be crystallites of silicon which were present in the indium melt upon contact with the substrate wafer. These crystallites attach themselves to the substrate during the initial stages of growth. During subsequent growth they increase in size at the expense of the surrounding epitaxial layer, leading to the formation of a depression. The crystallites usually break off during cleaning of the wafer in aqua regia solution. Staining of the wafer in Yang’s etch [11] showed that the epitaxial layer thickness at the bottom of the depression was essentially zero, resulting in a yellowish discoloration of the depression characteristic of the heavily doped silicon of the substrate. The more lightly doped epitaxial layer surrounding the depression was not stained by the etch.

Figure 3.8: A depression in an epitaxial layer. The sample was tilted 65° relative to the beam.

The development of depressions was observed whenever the melt contacted the silicon source wafer during the ramp-up to saturation temperature, while silicon crystallites were still present in the melt (usually from a previous growth experiment). Saturation of the melt occurs primarily by dissolution of the source wafer, while the crystallites are not completely dissolved. It is therefore necessary to carry out growth in the three distinct stages of heating, saturation and growth, as illustrated in fig. 3.1. Dissolution of any crystallites present in the melt will then take place during the heating phase.
3.4.2 Formation of meniscus lines

LPE layers grown by the tipping boat technique frequently exhibit meniscus lines, consisting of voids and depressions which occur along well defined lines, often surrounded by hillocks with square or rectangular base, as shown in fig. 3.9. These lines correspond with the solution front at a particular instance as the solution is tipped onto the substrate wafer. It is apparent from fig. 3.9 (a) that the deposition of foreign particles has prevented epitaxy and led to the development of a void. Upon further growth, increased local supersaturation in the vicinity of the void leads to thicker epitaxial growth around it. Finally, prominent facets develop and the shape of the features becomes more complex (fig. 3.9 (b)). In some cases, the hole in the centre of the hillock overgrows and with further growth, the features of the hillock become smoother. EDX analysis of the particles reveals the presence of carbon (fig. 3.10).

The observations described above are qualitatively similar to those made by Bauser [12], who studied the development of depressions and voids in GaAs using a horizontal centrifuge LPE system. She found that these voids could be caused by small particles which locally inhibit nucleation. In one experiment, GaAs powder was deliberately left on the GaAs substrate prior to growth. A very high density of depressions and voids resulted in the epitaxial layer. Some of the particles were swept along by the solution, resulting in particularly high densities of voids along well defined meniscus lines. A similar mechanism is likely to be responsible for the features reported here. The use of a graphite crucible results in the presence of particles of C and possibly SiC in the melt. Due to their lesser density compared to the density of the melt, the particles float to the top of the solution. During tipping of the LPE boat, they may contact the substrate wafer along the solution front and become attached to it, resulting in the characteristic meniscus lines.

Meniscus lines do not appear to have been reported in the literature for LPE growth by the slider boat technique. Their absence in this case may be due to the different mechanism of moving the melt onto the substrate wafer, which prevents contact between precipitates which float on top of the solution and the substrate.

Slight meltback of the substrate by 3°C prior to growth, in an attempt to dislodge the precipitates from the surface, proved unsuccessful. It was found that the development of the hillocks could be minimized by rapid rotation of the melt onto the substrate wafer.
Figure 3.9: SEM images of the features constituting meniscus lines. (a) deposit at the substrate-epi interface in a thin epitaxial layer, (b) Faceted features in a thick (30µm) epitaxial layer. The sample tilt was 30° and 15°, respectively.
3.4.3 Faceted growth

Faceted growth pyramids bounded by (111) faces are observed to develop on (100) oriented substrates at very high growth rates. High growth rates may result from growth at very high cooling rates, or they may be the result of temperature nonuniformities in the growth apparatus. In the latter case, the presence of a temperature gradient leads to the establishment of a concentration gradient of silicon due to the increase in silicon solubility at higher temperatures. Diffusion of silicon along the concentration gradient results in an increased rate of supply of Si to the coolest regions of the wafer. Fig. 3.11 shows growth pyramids which developed near the cool end of a wafer subjected to a temperature gradient. The development of (111) facets on (100) oriented silicon substrates has been observed by Appel for growth from several solvents, particularly Bi [13]. In this case their development could be explained on the basis of Jackson’s theory of the free energy of atomically smooth and rough surfaces [14]: a larger entropy change of a transition (from a higher to a lower temperature) will result in the fraction of surface sites occupied by atoms taking a value closer to 0 or 1, corresponding to an atomically flat surface. The more dilute the solute is in the solution, the larger the entropy change of the transition. Thus, for growth from Bi with a very low Si solubility
(less than 0.4 atomic percent at 1000°C), the development of atomically smooth (111) faces is favoured. A further reason may be an additional stabilization of the (111) faces through the adsorption of Bi atoms [13]. However, for the growth from In solution, smooth layers could be grown down to 600°C, where the Si solubility is essentially zero.

Figure 3.11: Development of pyramids due to the presence of a temperature gradient across the wafer. The sample tilt was 45°.

The development of pyramids in the case reported here may be attributed to the phenomenon of constitutional supercooling, which becomes more pronounced at higher growth rates. This is illustrated in fig. 3.12, which shows possible temperature and solute concentrations during growth. If a protuberance on a growth interface encounters a less supersaturated liquid, the protuberance will decay with time and the interface is considered to be stable. On the other hand, if the protuberance encounters a more supersaturated liquid, it will tend to grow with time, leading to a roughening of the surface. Due to the low growth rates and the high thermal conductivity of the metal melt and graphite substrate, the temperature variations in the melt during LPE growth are likely to be small, resulting in an unstable growth interface. With increasing growth rates, the solute concentration gradient near the growth interface increases, leading to a further deterioration of the stability of the interface and a roughening of the surface. At sufficiently high growth rates, the particular stability and low growth rate of the (111) planes results in the formation of facets with (111) oriented faces.

A further possible influence on the surface morphology may be exercised by convection in the melt, which is also expected to become more significant at higher growth rates. In the growth of thick layers of GaAs, the presence of a convecting solution has been proposed as the cause of cellular patterns [15]. Thus the presence of convection may result in an initial roughening of the
surface. The resulting protuberances may then develop further during subsequent growth as a result of constitutional supercooling.

![Diagram](image)

**Figure 3.12**: Possible solute and temperature profiles during solution growth. $C_s$ denotes the solute concentration and $T_e$ is the corresponding equilibrium temperature. Lines $T_a$ and $T_b$ are possible profiles for the actual temperature distribution. Constitutional supercooling occurs when the amount of supercooling increases with distance into the solution, such as in the case of profile $T_b$.

### 3.5 Epitaxial layer composition

Epitaxial layers grown from pure In solution exhibit p type doping, since In forms an acceptor level at $E_v + 0.16eV$ [16]. In is incorporated substitutionally into the epitaxial layer at a concentration near its solid solubility in silicon at the growth temperature. Appel [13] combined the results of C–V measurements on epitaxial layers grown from pure In with the data of Scott and Hager [17] obtained by Hall effect measurements. The line of best fit for the In concentration in the temperature range 700 – 1100°C can be expressed as

$$X_{In} = C e^{-D/T}$$

(3.2)

with $C = 3.53 \times 10^{24} \text{ cm}^{-3}$ and $D = 2.228 \times 10^4 \text{ K}$, where $T$ is the growth temperature in Kelvin. However, the scatter in the data is considerable. The relation is plotted in fig. 3.13. The concentration of ionized acceptor atoms in a doped semiconductor with fermi level $E_f$ is

$$N^+ = \frac{N_A}{1 + g \exp \left( \frac{E_A - E_F}{kT} \right)}$$

(3.3)

where $N_A$ and $N_A^+$ are the concentrations of the total and ionized number of acceptor atoms respectively, $E_A$ is the acceptor level and $g$ is the ground–state degeneracy factor. For acceptor levels, $g=4$ [18]. Fig. 3.14 plots this relation for In together with the corresponding relation for Ga, for which $E_A = E_v + 0.065eV$ [16]. The equation assumes that the semiconductor is non–degenerate. At dopant concentrations around $1 \times 10^{18} \text{ cm}^{-3}$, the effects of the formation of impurity bands and band
tailing [19] render eq. 3.3 inaccurate. For concentrations above $1 \times 10^{18}$ cm$^{-3}$, 100% ionization is usually assumed [20].

![In concentration vs. temperature graph](image1)

**Figure 3.13**: The dependence of In concentration in Si LPE layers grown from an In melt on temperature, according to data by Appel [13] and Scott and Hager [17]. Reproduced from Appel [13].

![Fraction of ionised acceptors](image2)

**Figure 3.14**: The fraction of ionised acceptor atoms and the dopant concentration as a function of the hole concentration in silicon, for the dopants In and Ga. The dopant vs. hole concentration curves assume no other doping species is present in the material.
Inspection of figs. 3.13 and 3.14 indicates that the doping concentration in layers grown from pure In solution below 1000°C will not exceed approximately $2 \times 10^{16}$ cm$^{-3}$. For solar cell applications, the optimum doping level is in the range $10^{16} - 10^{17}$ cm$^{-3}$ (see chapter 5). This necessitates the addition of a p type dopant to the melt. Ga has been found to be an excellent choice in this respect.

Fig. 3.15 shows the carrier concentration profiles of epitaxial layers grown from In and In/Ga solutions obtained by spreading resistance (SR) analysis. Growth from an In melt resulted in n doped silicon layers at the lower growth temperatures, with a peak concentration of approximately $10^{17}$ cm$^{-3}$ at the surface, grown near 600°C. The addition of a small amount of Ga to the melt resulted in an almost entirely p type epitaxial layer (fig. 3.15 (b)). The impurity responsible for the n type doping was identified as P by secondary ion mass spectrometry (SIMS) analysis.

In order to determine the contribution to the net doping of each of the three chief dopants In, Ga and P, SIMS profiles were obtained on an epitaxial layer grown from In/Ga solution. In contrast to the SR measurements, the SIMS technique measures the total amount of a certain impurity, rather than net hole or electron concentration. The profiles are shown in fig. 3.16. Ga can be seen to be the dominant p type impurity. The In peak of $3 \times 10^{16}$ cm$^{-3}$ is less than the value indicated by the line of best fit in fig. 3.13 by a factor of about 2, but is in good agreement with the values measured by Scott and Hager [17]. It is also possible that the incorporation of P and Ga has led to a reduction in the segregation coefficient for In. The P concentration of $9 \times 10^{16}$ cm$^{-3}$ at the surface of the sample corresponds well with the n type peak of $1.1 \times 10^{17}$ cm$^{-3}$ measured by SR analysis (fig. 3.15). It is evident from fig. 3.16 that the incorporation of P increases as the growth temperature decreases. This type of retrograde doping behavior has also been observed in silicon layers grown from Ga solution, in the temperature range 600–400°C [13,21].

The P concentration that must be present in the melt to account for the observed n type doping may be estimated using the results of Appel [13], who measured the carrier concentrations in silicon grown from a P-doped In melt at temperatures between 950 and 750°C. Extrapolation of these results yields an effective segregation coefficient of approximately 8, where the effective segregation coefficient $K$ is defined as the ratio of the atom fraction of the impurity in the solid to that in the melt [22]. The mean P concentration in the epitaxial layer between 950 and 750°C may be estimated at $4 \times 10^{16}$ cm$^{-3}$, or $8 \times 10^{-5}$ at.% from fig. 3.16, giving a value for the P concentration in the melt of approximately $10^{-5}$ at.%. This figure is a rough estimate only, due to the considerable uncertainty of the extrapolated value for the phosphorus segregation coefficient and the scarcity of data on the P concentration in the epitaxial layers. The exact source of the phosphorus has not been determined to date. Possible sources are the as-supplied In melt or the graphite crucible.
Figure 3.15: Carrier concentration profiles obtained by spreading resistance analysis. (a) Epitaxial layer grown from In solution, (b) epitaxial layer grown from 99.64 at% In/0.36 at% Ga solution. The growth interval in both cases was from 970 - 600°C; the cooling rate was 0.7°C/min.
Figure 3.16: SIMS profile of the elements In, Ga and P in an epitaxial layer grown from 99.64 at% In/0.36 at.% Ga solution. The growth interval was 975 – 600°C.

3.6 Electronic properties

The electronic properties of the single crystal epitaxial silicon layers were investigated by several techniques. Deep Level Transient Spectroscopy (DLTS) measurements were used to search for deep – level trapping centres in the silicon bandgap [23]. These trapping centres are often introduced by metallic impurities and act as efficient recombination sites for minority carriers. The minority carrier lifetimes were determined by the photoconductivity decay (PCD) method.

3.6.1 DLTS measurements

Samples for DLTS measurements were prepared on an epitaxial layer grown from In solution on a 0.015Ω−cm, B doped Cz substrate. The growth interval was 975 – 910°C, so that the region of the thin film probed by DLTS was grown around 910°C. Small area (1mm diameter) p–n diodes were fabricated on the layers using standard photolithographic techniques. The process steps are summarized in table 3.2. The room temperature majority carrier (hole) concentration was determined at $6 \times 10^{15}$cm$^{-3}$ from evaluation of the capacitance – voltage characteristics.
The DLTS measurements did not reveal the presence of any traps. Given that the sensitivity limit of DLTS is approximately $10^{-4}$ of the majority carrier concentration [23], the concentration of electrically active impurities in the measured samples is likely to be below $10^{12}\text{cm}^{-3}$. However,
the sensitivity of the technique to traps in the upper half of the bandgap may be considerably less, since only a certain fraction of the trapping sites would be filled with electrons during the forward bias pulse. It must also be kept in mind that only a fraction of the metallic impurities are electrically active, with this fraction ranging from 0 to 1 and being dependent on several factors, such as the impurity type, the thermal history of the sample and the presence of other defects, such as structural defects or other impurities [23,24]. Nevertheless, the results give an indication that the purity of the LPE layers is very high, and the material therefore of good quality.

3.6.2 Determination of the minority carrier lifetime using photoconductivity decay (PCD)

3.6.2.1 The PCD technique

The PCD technique allows the determination of the minority carrier lifetime in a silicon layer through the contactless measurement of the conductivity change in the layer following illumination by a light pulse. Fig. 3.17 illustrates two variants of the PCD technique. In the transient PCD technique, a light pulse much shorter in duration than the minority carrier lifetime in the sample is used. Once the minority carriers have had sufficient time to distribute throughout the sample \( (D \cdot t)^{1/2} \gg T \), under low level injection conditions the excess minority carrier concentration \( \Delta N(t) \) decays exponentially:

\[
\Delta N(t) = \Delta N(0) \exp\left(-\frac{t}{\tau_{\text{eff}}}\right) \tag{3.4}
\]

where \( t \) is the period of time that has elapsed since the light pulse, and \( \tau_{\text{eff}} \) is the effective lifetime at low level injection. \( \tau_{\text{eff}} \) depends on the bulk lifetime and the surface recombination velocity through [25]:

\[
\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{B}} + D\beta^2 \tag{3.5}
\]

with

\[
\beta \tan \left( \frac{\beta T}{2} \right) = \frac{S}{D} \tag{3.6}
\]

where \( \tau_B \) is the bulk lifetime of the sample, \( D = D_p D_n (n + p)/(nD_n + pD_p) \) is the ambipolar diffusion coefficient, \( T \) is the sample thickness and \( S \) is the surface recombination velocity (assumed equal on both surfaces). The transient PCD technique has the advantage that knowledge of the carrier mobilities is not critical, since both the conductivity \( \sigma \) and its rate of change with time \( d\sigma/dt \) are proportional to the mobility. Also, the number of electron–hole pairs generated by the light pulse need not be known accurately.
In quasi steady state PCD, the duration of the light pulse is much longer than the minority carrier lifetime and the conductivity decay in the sample follows the decay of the light intensity. The minority carrier lifetime can be determined from the absolute magnitude of the signal, provided the rate of photogeneration of electron–hole pairs in the sample is known:

\[ \tau = \frac{\Delta N}{G} \]

The advantage of the quasi steady state PCD method is that very low lifetimes can be measured without the requirement of very fast electronics and short light pulses. However, in addition to the rate of photogeneration G, the carrier mobilities \( \mu \) of the sample must be known.

### 3.6.2.2 Experimental

Epitaxial layers were grown from an In/Ga solution on 0.015Ω–cm p type Cz substrates. Following saturation at 970°C, the solution was supersaturated by 5°C for 2 min by removing the melt from the silicon source and lowering the temperature to 965°C. Growth was terminated around 600°C. In order to determine the influence of the cooling rate on the minority carrier lifetime, epitaxial layers were grown at cooling rates of 0.3, 0.7 and 2°C/min. The layers were grown consecutively in order to minimize the possibility of additional contamination of the melt or change of melt composition during the experiments. Electrochemical voltage (ECV) profiling of an epitaxial layer grown from the same melt just prior to the samples yielded a mean carrier concentration in the film of \( 1 \times 10^{17} \text{cm}^{-3} \). Table 3.4 summarizes the average thicknesses of the layers obtained using a micrometer dial gauge.
<table>
<thead>
<tr>
<th>Epilayer</th>
<th>K145</th>
<th>K147</th>
<th>K150</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cooling rate ( (^\circ\text{C/min}) )</td>
<td>0.7</td>
<td>0.3</td>
<td>2.0</td>
</tr>
<tr>
<td>Average thickness ( (\mu\text{m}) )</td>
<td>32.9</td>
<td>38.5</td>
<td>35.3</td>
</tr>
</tbody>
</table>

Table 3.4: Average thicknesses of the epitaxial layers used for PCD measurements

Following epitaxial layer growth, the heavily doped substrates were removed by a chemical etching technique (fig. 3.18): The epitaxial layer and the edges of the substrate were covered with acid resistant adhesive tape and mounted on an inert substrate. The majority of the substrate was removed using a solution of 10:1:13 HF/HNO₃/H₃PO₄. This solution results in a uniform etch profile over the entire exposed region. When the substrate thickness was estimated to be less than 50µm, the solution was changed to 1:3:8 HF:HNO₃:CH₃COOH. The silicon etch rate of this solution decreases dramatically for dopant concentrations below 10^{18} cm\(^{-3}\) and therefore acts as an 'etch stop' which completely removes the substrate but leaves the epitaxial layer intact [26]. Following removal of the tape, the wafers were cleaned in acetone, rinsed and given a final etch in a solution of HF:HNO₃ 1:40 for 5sec. The final thicknesses of the samples were measured by fourier transform infra-red spectroscopy (FTIR) to be around 30µm [27]. Comparison of the thickness of a cleaved sample, measured both by SEM and by FTIR, yielded good agreement between the two methods.

Electrical passivation of the surfaces was achieved using an ethanol/0.08M iodine solution. This solution has been found capable of achieving very low surface recombination velocities [28]. Just prior to immersion in the solution, the samples were dipped in 10% HF until the surfaces became hydrophobic. The PCD measurements were carried out with a microwave detected transient PCD system. A 904nm GaAs laser, defocussed to an area of approximately 1cm\(^2\) was used to excite minority carriers in the sample. A detailed description of the system is given by Basore and Hansen [29]. A white bias light of approximately 1/6th of one sun intensity was used to approximate the carrier concentrations in the wafer which would exist at maximum power point in a solar cell. The laser pulse intensity at maximum power setting is \(2 \times 10^{12}\) photons/pulse [29], resulting in a maximum of \(3 \times 10^{14} \text{cm}^{-3}\) photogenerated electron–hole pairs in a 30µm thick layer, thus maintaining low injection conditions in the device. Due to light absorption in the iodine/ethanol solution and reflection losses, the actual photogenerated carrier concentrations will be lower than this figure.
3.6.2.3 Results

Table 3.5 shows the average effective lifetimes obtained. For thin samples, very low surface recombination velocities are necessary to ensure that $\tau_B = \tau_{eff}$. For low surface recombination velocities, $(S \ll D/T)$ eq. (3.5) becomes:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_B} + \frac{2S}{T} \quad (3.8)$$

The thinness of the samples used means that the bulk lifetimes are likely to be significantly higher than the values for the effective lifetimes.

<table>
<thead>
<tr>
<th>Epilayer</th>
<th>K147 0.3°C/min</th>
<th>K145 0.7°C/min</th>
<th>K150 2°C/min</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective lifetime, $\tau_{eff}$ ($\mu$s)</td>
<td>9.6 ± 0.4µs</td>
<td>10.0 ± 0.1µs</td>
<td>7.6 ± 0.1µs</td>
</tr>
<tr>
<td>Comments</td>
<td></td>
<td></td>
<td>Surfaces were not completely hydrophobic</td>
</tr>
</tbody>
</table>

Table 3.5: Effective minority carrier lifetimes obtained from photoconductivity decay measurements. The values shown are the averages of 5 measurements.
The differences in the measured effective lifetimes may be due to a dependence of the bulk lifetime on cooling rate, or to different surface recombination velocities. Effective passivation using the iodine/ethanol solution requires the surfaces to be hydrophobic prior to immersion of the samples in the solution. On K150, it was not possible to obtain a completely hydrophobic surface, which may explain the slightly lower effective lifetime. The minority carrier diffusion length exceeds 100µm in all cases (assuming D=20cm²s⁻¹), indicating that the epitaxial layers are of high quality, regardless of the cooling rate used.

### 3.7 Fabrication and characterization of solar cells on single crystal epitaxial layers

#### 3.7.1 Cells on heavily doped substrates

The demonstration of high cell efficiencies on single crystal epitaxial layers is an important prerequisite for the achievement of high efficiency, low cost solar cells using the epitaxy process. Epitaxial layers for solar cells were deposited on 0.015Ω·cm, B doped Cz substrates. Typically growth was commenced at 960°C–970°C and terminated at 600°C. The cooling rate was 0.7°C. Solar cells with an area of 2×2cm² were then fabricated on the layers. Table 3.6 summarizes the process.

<table>
<thead>
<tr>
<th>Step</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide growth</td>
<td>1100°C, 80 min, O₂ + TCA</td>
</tr>
<tr>
<td>Oxide patterning and KOH etching</td>
<td>Inverted pyramids in the front active area</td>
</tr>
<tr>
<td>Oxide growth</td>
<td>1100°C, 100 min, O₂ + TCA</td>
</tr>
<tr>
<td>Oxide patterning</td>
<td>Finger pattern in the front active area</td>
</tr>
<tr>
<td>n⁺⁺ phosphorus diffusion</td>
<td>900°C, 30 min, N₂ (20Ω/□)</td>
</tr>
<tr>
<td>Oxide removal</td>
<td>BHF</td>
</tr>
<tr>
<td>Oxide growth</td>
<td>1100°C, 80 min, O₂ + TCA</td>
</tr>
<tr>
<td>Oxide patterning</td>
<td>Cell area, 2 × 2cm²</td>
</tr>
<tr>
<td>n⁺ phosphorus diffusion</td>
<td>860°C, 30min, N₂ (120Ω/□)</td>
</tr>
<tr>
<td>Oxide removal</td>
<td>BHF</td>
</tr>
<tr>
<td>Oxide growth</td>
<td>1000°C, 95min, O₂ + TCA (blue antireflection oxide)</td>
</tr>
<tr>
<td>Oxide patterning</td>
<td>Finger pattern in the front active area</td>
</tr>
<tr>
<td>Metallization</td>
<td>Front: 25nm Cr + 25nm Pd Rear: 500nm Al</td>
</tr>
<tr>
<td>Silver Electroplating</td>
<td>Finger width 24µm</td>
</tr>
<tr>
<td>Sintering</td>
<td>400°C, 30min, 4% H₂ / 96% Ar</td>
</tr>
</tbody>
</table>

*Table 3.6:* Process steps for the fabrication of solar cells on single crystal epitaxial layers

53
Table 3.7 lists the parameters of solar cells on heavily doped Cz substrates. The epitaxial layer thickness ranges from 4 to 45µm. A striking feature of the cell results is that the open circuit voltage of all of the cells except 2K83 prior to thinning is in the range 655 to 658mV, independent of epitaxial layer thickness. Control cells fabricated on high quality, moderately doped float zone wafers with identical processing have substantially higher $V_{oc}$. The explanation is that most of the recombination current is due to the heavily doped substrate. The epitaxial layer and emitter region contribute little to the recombination current within the cell.

<table>
<thead>
<tr>
<th>Cell ID</th>
<th>Thickness (µm)</th>
<th>Open circuit voltage (mV)</th>
<th>Short circuit current (mA)</th>
<th>Fill factor</th>
<th>Efficiency (%)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>2K25</td>
<td>20</td>
<td>656</td>
<td>28.4</td>
<td>0.798</td>
<td>14.9*</td>
<td>Single Diffusion.</td>
</tr>
<tr>
<td>2K26</td>
<td>30</td>
<td>656</td>
<td>31.1</td>
<td>0.780</td>
<td>15.9</td>
<td></td>
</tr>
<tr>
<td>2K32</td>
<td>28</td>
<td>656</td>
<td>31.2</td>
<td>0.800</td>
<td>16.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>651</td>
<td>32.6</td>
<td>0.803</td>
<td>Thinned to within 10µm of epi</td>
</tr>
<tr>
<td>2K35</td>
<td>6</td>
<td>655</td>
<td>22.6</td>
<td>0.826</td>
<td>12.2</td>
<td></td>
</tr>
<tr>
<td>2K41</td>
<td>35</td>
<td>657</td>
<td>30.5</td>
<td>0.820</td>
<td>16.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>655</td>
<td>30.8</td>
<td>0.813</td>
<td>Thinned to within 25µm of epi</td>
</tr>
<tr>
<td>2K42</td>
<td>30</td>
<td>658</td>
<td>29.8</td>
<td>0.802</td>
<td>15.7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>649</td>
<td>30.8</td>
<td>0.820</td>
<td>Thinned to within 10µm of epi</td>
</tr>
<tr>
<td>2K83</td>
<td>10</td>
<td>653</td>
<td>27.7</td>
<td>0.821</td>
<td>14.8</td>
<td></td>
</tr>
<tr>
<td>K90</td>
<td>20</td>
<td>656</td>
<td>28.2</td>
<td>0.810</td>
<td>15.0</td>
<td>Single Diffusion</td>
</tr>
<tr>
<td>K102</td>
<td>4</td>
<td>655</td>
<td>21.8</td>
<td>0.821</td>
<td>11.7</td>
<td></td>
</tr>
<tr>
<td>K107</td>
<td>40</td>
<td>656</td>
<td>31.2</td>
<td>0.823</td>
<td>16.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>651</td>
<td>32.3</td>
<td>0.824</td>
<td>Thinned to within 20µm of epi, MgF₂/Al reflector on rear</td>
</tr>
<tr>
<td>K108</td>
<td>30</td>
<td>658</td>
<td>31.1</td>
<td>0.812</td>
<td>16.5</td>
<td></td>
</tr>
<tr>
<td>K109</td>
<td>45</td>
<td>656</td>
<td>32.3</td>
<td>0.816</td>
<td>17.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>655</td>
<td>33.3</td>
<td>0.809</td>
<td>Thinned to within 15µm of epi, MgF₂/Al reflector on rear</td>
</tr>
</tbody>
</table>

Table 3.7: The parameters of solar cells fabricated on 0.015Ω-cm Cz substrates. Cell area = 4cm², T=25°C. * = Sandia measurement

It is apparent from the results in table 3.7 that the major factor limiting the efficiencies of the cells is the value of $J_{sc}$. Due to the absence of a rear reflector, weakly absorbed infra-red light which passes through the epitaxial layer is absorbed in the heavily doped, low lifetime substrate and will have little chance of contributing to the cell current. For cells of 30µm thickness, the con-
trituation from the substrate, assuming a diffusion length of 12µm, is of the order of 1 mA cm⁻² [30]. Improvement of the cell efficiency therefore requires removal of most of the heavily doped substrate and the application of a reflective rear contact, in order to bring the rear optical reflector closer to the p–n junction.

Some of the cells were chemically thinned from the rear and then remeasured, with Al redeposited on the rear after every thinning step. The Al acts as both a rear contact and an optical reflector. Fig. 3.19 shows the final structure. Thinning was performed in a similar way to the thinning process of epitaxial samples for PCD measurements (section 3.6.2). The cell was mounted, emitter side down, on an inert substrate using acid resistant adhesive tape. A solution of 10:1:13 HF:HNO₃:H₃PO₄ was used as the etchant. Following thinning, the cell was detached from the substrate.

![Diagram of solar cell structure](image)

**Figure 3.19**: (a) The structure of solar cells on single crystal epitaxial layers, following etch removal of the majority of the substrate, (b) the rear contact structure for the cells grown on 0.3Ω–cm FZ substrates.

Due to the lack of passivation of the rear surface of the cells, the rear surface recombination velocity is expected to be close to the theoretical limit of $1 \times 10^7$ cm s⁻¹ following deposition of the Al rear contact. Thinning of the substrate to less than the value of the substrate diffusion length will therefore result in a significant increase in the saturation current and a decrease in $V_{oc}$. Further, since minority carriers generated in the substrate at a distance less than a diffusion length from the epitax-
inal layer have a high probability of being collected, no significant increase in $J_{sc}$ can be achieved. In fact, the increased effective surface recombination velocity at the epi–substrate interface will result in a decrease in $J_{sc}$ for small values of the substrate thickness [31]. Thus the optimum substrate thickness is of the order of the substrate diffusion length. This is in agreement with the parameters of thinned cells, also shown in table 3.7. As the substrate thickness is decreased to around 10µm, $V_{oc}$ begins to drop significantly due to an increase of the effective rear recombination velocity.

The thinning process increased cell efficiencies by about 5% (relative). However, evaporation of Al onto the bare Si substrate provides a nonoptimal optical mirror. Sandwiching a thin layer of MgF₂ between the substrate and the Al would result in further improvements in $J_{sc}$. The highest independently confirmed efficiency of a thinned cell is 17.0% (AM 1.5, 100mW/cm², 25°C) on cell 2K32, with $V_{oc} = 651$ mV, $J_{sc} = 32.6$ mA/cm², FF = 0.803. This cell was measured at Sandia National Laboratories.

### 3.7.2 Cells on lightly doped substrates

Further improvements in solar cell efficiency are possible if the rear recombination velocity can be reduced. This can be achieved by passivating the rear surface with an oxide rather than relying on the back surface field formed by a high–low junction. Epitaxial layers were grown for this purpose on 0.3Ω·cm FZ substrates. The fabrication process was similar to that of table 3.6, with the following differences. The majority of the FZ substrate was chemically removed following the sheet phosphorus diffusion, rather than at the end of the process. Boron was diffused under rear contact dots, 100µm in diameter and spaced 800µm apart, followed by growth of a passivating oxide on both the front and rear surfaces and aluminium deposition over the rear. The rear contact structure is shown in fig. 3.19.

The results obtained with this approach are shown in table 3.8. For most of these cells, the improvements in the cell parameters are due in part to carrier collection from the remaining FZ substrate. However, even on cell 2K70, where the substrate has been completely removed, the efficiency is significantly higher than for the cells fabricated on heavily doped substrates, as a result of improved rear surface passivation. The highest independently confirmed efficiency was achieved on cell K141, with the parameters $V_{oc} = 666$ mV, $J_{sc} = 35.0$ mA/cm², FF = 0.775, $\eta = 18.1\%$ (measured at Sandia National Laboratories). The comparatively low fill factor may be due in part to a high series resistance during measurement of the cell, since contacting the rear of the cell proved difficult. Fig. 3.20 compares the spectral response curve for the 17.0% efficient cell with that of the 18.1% efficient cell. The spectral response for cell K141 is better throughout the useful spectrum, with the largest improvement occurring in the infra–red, due to the combined effects of improved surface passivation and higher collection efficiency of minority carriers generated in the substrate on which the epitaxial layer is grown. The poorer spectral response of 2K32 in the short wavelength region may be the result of an inferior antireflection scheme on this cell.
<table>
<thead>
<tr>
<th>Cell ID</th>
<th>Thickness (µm)</th>
<th>Open circuit voltage (mV)</th>
<th>Short circuit current (mA)</th>
<th>Fill factor</th>
<th>Efficiency (%)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>2K70</td>
<td>45</td>
<td>666</td>
<td>34.2</td>
<td>0.781</td>
<td>17.8</td>
<td>Thinned down to epi layer</td>
</tr>
<tr>
<td>2K62</td>
<td>35</td>
<td>640</td>
<td>35.6</td>
<td>0.808</td>
<td>18.4</td>
<td>Thinned to within 45µm of epi layer</td>
</tr>
<tr>
<td>2K67</td>
<td>25</td>
<td>650</td>
<td>35.2</td>
<td>0.799</td>
<td>18.3</td>
<td>Thinned to within 60µm of epi layer</td>
</tr>
<tr>
<td>K134</td>
<td>35</td>
<td>669</td>
<td>34.9</td>
<td>0.789</td>
<td>18.4</td>
<td>Thinned to within 15µm of epi layer</td>
</tr>
<tr>
<td>K141</td>
<td>35</td>
<td>666</td>
<td>35.0</td>
<td>0.775</td>
<td>18.1*</td>
<td>Thinned to within 15µm of epi layer</td>
</tr>
</tbody>
</table>

Table 3.8: The electrical parameters of solar cells fabricated on 0.3Ω-cm FZ substrates. Cell area = 4cm², T=25°C. * = Sandia measurement

![Graph showing internal spectral response curves for high efficiency epitaxial cells fabricated on heavily doped Cz substrate (2K32) and moderately doped FZ substrate (K141).](image)

Figure 3.20: The internal spectral response curves for the high efficiency epitaxial cells fabricated on a heavily doped Cz substrate (2K32) and on a moderately doped FZ substrate (K141).

### 3.7.3 Estimation of the minority carrier lifetime from cell results

The electrical parameters of the cells fabricated on heavily doped substrates (table 3.7) can be used to estimate the minority carrier lifetime in the base of the cell. Verhoef and Sinke [32] developed an analytical solution for the minority carrier transport in a nonuniformly doped quasi-neutral...
silicon region. This solution was used to calculate the open circuit voltage of solar cells of similar thicknesses and doping profiles to those in table 3.7. A base thickness of $W = 30\mu m$ was assumed. The constants in the equations describing the variation of doping with distance from the p–n junction, and the variation of the mobility with doping, were adjusted to give front and rear doping levels of $10^{16}$ and $10^{17} \text{cm}^{-3}$ respectively, and values for the diffusion constant $D$ of 30 and 20 cm$^2$s$^{-1}$ for $N=10^{16}$ and $10^{17} \text{cm}^{-3}$, respectively:

$$N(x) = 10^{16}e^{767.5x}$$  \hspace{1cm} (3.9)

$$\mu(N) = 7.6 \times 10^5 N^{-0.1761}$$  \hspace{1cm} (3.10)

The exponential base doping profile assumed in the solution is a reasonable approximation to the measured doping profile (fig.3.15 (b)). The intrinsic carrier density was taken as $n_i=8.6 \times 10^9 \text{cm}^{-3}$ at 25°C. The influence of the substrate is taken into account as an effective surface recombination velocity $S_{\text{eff}}$ at the rear of the base, whose value is given by

$$S_{\text{eff}} = \frac{D_{\text{sub}}N(W)}{L_{\text{sub}}N_{\text{sub}}} \exp(\Delta E_g/kT)$$  \hspace{1cm} (3.11)

where $D_{\text{sub}}$, $L_{\text{sub}}$ and $N_{\text{sub}}$ refer to the values of the parameters in the substrate, $N(W)=10^{17} \text{cm}^{-3}$ is the doping at the rear of the cell and the amount of bandgap narrowing $\Delta E_g$ is calculated from the model of King and Swanson [33]:

$$\Delta E_g = C_\alpha \left( \ln \left( \frac{N_{\text{sub}}}{N_{ao}} \right) - \ln \left( \frac{N(W)}{N_{ao}} \right) \right)$$  \hspace{1cm} (3.12)

with $N_{ao}=2.3 \times 10^{17} \text{cm}^{-3}$, and $C_\alpha = 17.8 \text{meV}$ for p type silicon. A lower bound on $S_{\text{eff}}$ is obtained by substituting $D_{\text{sub}} = 3.3 \text{cm}^2\text{s}^{-1}$ and $L_{\text{sub}} = 12\mu m$, the values for high quality float–zoned silicon doped to $N_{\text{sub}} = 5 \times 10^{18} \text{cm}^{-3}$, giving $S_{\text{eff}} = 475 \text{cm} \text{s}^{-1}$. A more realistic value for $S_{\text{eff}}$ can be estimated from the value of $J_0$ of very thin cells, such as cell K102 in table 3.7. Assuming that the contribution from the base to $J_0$ is negligible, and assuming that the contribution from the emitter is $J_{0,e} = 2 \times 10^{-14} \text{Acm}^{-2}$, the contribution of the substrate is approximately $J_0 = 2 \times 10^{-13} \text{Acm}^{-2}$. $S_{\text{eff}}$ is then given by

$$J_0 = \frac{qN_{ao}^2}{N(W)} S_{\text{eff}}$$  \hspace{1cm} (3.13)

giving $S_{\text{eff}} = 1700 \text{cm} \text{s}^{-1}$.

Fig. 3.21 plots the dependence of the open circuit voltage on the minority carrier lifetime for an assumed short circuit current of 30mAcm$^{-2}$. In the case of the lower bound on the value of $S_{\text{eff}}$, an open circuit voltage of 658mV gives a lower bound on the minority carrier lifetime of 7µs, while the more realistic case $S_{\text{eff}} = 1700 \text{cm} \text{s}^{-1}$ implies a lifetime of around 20µs. These values are in good agreement with the minority carrier lifetimes determined by PCD. The results also suggest that the minority carrier lifetime of the epitaxial material is not significantly affected by the high temperature solar cell fabrication process.
**Figure 3.21**: The calculated dependence of the open circuit voltage on the minority carrier lifetime in a 30µm thick epitaxial silicon cell, for two values of the effective rear recombination velocity. The doping concentrations at the front and rear of the epitaxial layer are assumed to be $10^{16}$ and $10^{17}$ cm$^{-3}$, respectively.

### 3.8 References


[27] A. Stephens, private communication


Chapter 4

LPE of Silicon on Multicrystalline Silicon Substrates

4.1 Introduction

The study of the growth of multicrystalline epitaxial layers is of interest due to their potential for low cost solar cell applications. The layers could be deposited on a foreign substrate, such as glass, or on low cost multicrystalline silicon. In the former case, the steps of nucleation of crystals on the substrate, followed by impingement of the crystals, must occur before a continuous multicrystalline film can grow. The nucleation conditions must be well controlled in order to obtain crystals of reasonable size, and in order for these crystals to impinge on each other to produce a continuous layer. In the latter case, due to the presence of a crystal template, a continuous layer is always produced provided the surface is clean. Deposition on multicrystalline silicon substrates is therefore considerably easier than deposition on foreign substrates.

The deposition of silicon from solution on multicrystalline silicon substrates introduces several complications not encountered during deposition on single crystal wafers. The presence of many grains with different crystallographic orientations will lead to different growth kinetics on each grain. This may result in different growth rates and non-uniform layer thickness. Grain boundaries are regions of crystalline disorder, containing dangling and strained atomic bonds. Epitaxial growth in the vicinity of grain boundaries is therefore significantly different from the growth in intragrain regions. Finally, the presence of many structural defects such as dislocations and stacking faults which are normally absent in single crystal silicon may also be expected to influence the growth mechanisms and the epitaxial layer properties.

In this chapter, the growth of epitaxial layers on multicrystalline silicon substrates and the fabrication of solar cells on these layers is described. The layers were grown mostly on large grained, cast silicon wafers, using similar growth parameters to those used for growth on single crystal substrates.

4.2 Epitaxial layers on large grained multicrystalline silicon

4.2.1 Surface morphology and behavior of grain boundaries

4.2.1.1 Experimental

Two types of cast multicrystalline silicon wafers, supplied as-sawn, were used as the substrates: Osaka Titanium 0.9Ω-cm and Wacker Chemitronic 0.015Ω-cm (both B doped). The wafers were mechanically polished with 1µm particle size diamond paste and cleaned by degreasing
in acetone followed by immersion in 3:1 H₂SO₄:H₂O₂ for 3 minutes. They were then chemically etched using a solution of 40:1 HNO₃:HF for 5 minutes to remove polishing damage. The Osaka Ti substrates were given a boron diffusion by first depositing borosilicate glass during a 15 minute prededposition at 1000°C in a N₂ ambient, using BN solid source wafers. This was followed by a 20 hour drive in at 1100°C in N₂. Finally the substrates were oxidized for 1 hour in dry O₂ at 900°C with the oxide subsequently removed in HF. This diffusion gives a deep B doping profile with a relatively low surface B concentration. High B concentrations will result in lattice mismatch and significantly degrade the quality of resulting epitaxial layers [1]. For the B diffusion just described, no lattice mismatch effects of the type mentioned by Blakers et al. [1] were observed and epitaxial layer quality appeared not to have been degraded. The B diffusion enables delineation of the substrate – epi interface through the use of various etches, as described below.

Growth was carried out from an In/Ga melt at temperatures between 960 and 600°C, using cooling rates between 0.3 and 2°C/min. Prior to growth, the solution was supersaturated by 5°C to prevent a possible dissolution of the substrate in the initial stages of growth. Following growth, some of the wafers were cleaved and etched to delineate the substrate/epi interface and, in some cases, the grain boundaries.

4.2.1.2 Epitaxial layer morphology

Epitaxial layers grown on polished multicrystalline substrates at low cooling rates were generally found to be smooth and specular. On grains with a near (111) orientation, terrace growth is observed. This mode of growth was studied by Bauser and Strunk [2]. The misorientation steps that exist on the substrate along the intersection lines of the substrate and the (111) plane act as nucleation sites for growth. Prior to growth, these steps will be unevenly distributed and of varying height. During crystal growth, the steps display different lateral growth rates, with the growth rate being inversely proportional to the step height. Steps can therefore bunch together, leading to the formation of relatively flat, near (111) oriented surfaces and macrosteps. This is illustrated in fig. 4.1. Growth proceeds chiefly by the motion of small steps across the treads, which are emitted from the base of the risers and move across the surface much more rapidly than the risers, due to their small height. Fig. 4.2 shows an epitaxial layer grown on grains with near (111) orientation, showing the formation of terraces.

The epitaxial layer thickness may be expected to vary from grain to grain due to the different densities of atomic attachment sites an grains with different crystallographic orientations. On a macroscopic level, this difference may be expressed by different values of the rate constant for the surface reaction (see chapter 2)

\[
\frac{dm}{dt} = k_r A(C_r - C^*)^n
\]  

(4.1)

where \(k_r\) is a rate constant for the surface reaction, \(C^*\) and \(C_r\) are the equilibrium concentration of the solute and the solute concentration at the crystal–liquid interface, respectively, and \(n\) is the order of the reaction. Thus the degree of supersaturation of the solution over the various grains may differ
during growth, leading to a redistribution of solute by lateral diffusion. For example, perfectly oriented (111) surfaces have no atomic attachment sites in the absence of defects and require formation of a two-dimensional nucleus for the growth of an additional atomic layer. The amount of supersaturation required to achieve this is usually very large, and (111) faces would be expected to grow more slowly than other orientations. However, the presence of many defects in multicrystalline silicon can introduce further attachment sites and reduce the differences in the growth rates. Dislocations and dislocation partials are well known to provide monatomic or subatomic growth steps, for growth on (111) oriented silicon [2]. The energy for atomic attachment at the defect in this case is significantly less than that required for two-dimensional nucleation.

Figure 4.1: Profile of a terraced growth interface. The growth face is tilted with respect to the (111) plane by an angle $\delta$. After Bauser and Strunk [2].

Figure 4.2: The surface of an epitaxial layer grown on grains with near (111) orientation. Sample tilt 45°.
The epitaxial layer thicknesses were measured on both sides of several grain boundaries using a scanning electron microscope, at a distance of approximately 100µm from the grain boundary. For all the cooling rates used, the average variation in thickness was less than 5% of the epitaxial layer thickness, with a maximum thickness variation between adjacent grains of approximately 5µm, or 15% of the layer thickness.

4.2.1.3 Epitaxial layer growth in the vicinity of grain boundaries

Fig. 4.3 shows the cleaved edge of a multicrystalline substrate with a 35 µm thick epitaxial layer. It is apparent that growth in the vicinity of the grain boundary was severely retarded. This lack of growth has resulted in thicker growth on either side of the grain boundary. Inspection of many grain boundaries shows that the depth of the grain boundary grooves is highly variable and may extend nearly all the way to the substrate – epi interface. Such a deep groove is shown in fig. 4.4.

It can also be seen from fig. 4.3 that the direction of the grain boundary changes at the substrate – epi interface, in this particular case its direction tends towards the vertical to the substrate – epi interface. This observation was made on most of the grain boundaries studied. On 20 grain boundaries studied, the mean angle of the grain boundary in the substrate relative to the substrate-interface normal was 26°, while in the epilayer it was 13°.

The influence of coherent twin boundaries on epitaxial growth is illustrated in fig. 4.5. The grooves are much shallower than for the case of a general grain boundary, and no change of direction is observed at the substrate – epi interface. These observations were made on all the coherent twins studied in this way. The behavior of coherent twins is thus different from that of general grain boundaries.

The development of grain boundary grooves under non-equilibrium conditions may be understood qualitatively in terms of the larger energy required for incorporation of atoms at the grain boundary compared with the intragrain regions, leading to localized supersaturation of the melt in the vicinity of the grain boundary and therefore increased growth on either side of the grain boundary. Once a groove has developed, growth at the grain boundary is further retarded by a reduced supply of solute, due to the fact that that solute diffusing towards the substrate first encounters the raised walls on either side of the grain boundary, leading to a high probability of incorporation of solute into this region.
Figure 4.3: Cleaved section of an epitaxial layer, showing a change in grain boundary direction at the substrate–epi interface.

Figure 4.4: Cleaved section of an epitaxial layer at a deep grain boundary groove. The dashed line indicates the substrate–epi interface.
Figure 4.5: Cleaved section of an epitaxial layer in a twinned region of the crystal.

Under near-equilibrium conditions (very low growth rates) the groove angle at a grain boundary can be described quantitatively. For three phases in equilibrium, as shown in fig. 4.6, and assuming that the surface tensions are isotropic, the angle $\phi$ formed between the $\alpha$ and $\beta$ phases is given by [3]:

$$\sigma_{\alpha\alpha} = 2\sigma_{\alpha\beta} \cos \left( \frac{\phi}{2} \right)$$  \hspace{1cm} (4.2)$$

According to eq. (4.2), the angle formed at a grain boundary groove can be used to estimate the grain boundary energy. Values obtained in this way are in reasonable agreement with calculated values [4]. Due to the low energy associated with them, the angles formed by coherent twins are close to 180°, and the grooves are very shallow.

Figure 4.6: Schematic illustration of a grain boundary groove formed at the intersection of two $\alpha$ phases and a $\beta$ phase, with surface tensions $\sigma_{\alpha\alpha}$ and $\sigma_{\alpha\beta}$. After ref. [3].

The change in direction of the grain boundaries at the substrate-epi interface may be understood by considering the variation of the energy associated with a grain boundary with the angle it makes relative to the substrate surface. The grain boundary may propagate in a direction which
minimizes its overall energy, within the one degree of freedom available. For an isotropic grain boundary (with energy independent of the direction of grain boundary propagation), the overall energy would be a minimum in a direction normal to the substrate surface. In practice, the anisotropic nature of grain boundaries results in deviations of the propagation direction from the substrate normal. Further, the groove which is created at the grain boundary restricts the range of angles along which it can propagate. Thus, grooves with steep sidewalls restrict propagation of the grain boundary to directions close to the normal to the substrate surface. No change of direction is observed for coherent twins because the direction of propagation in the substrate already represents the lowest energy grain boundary configuration.

LPE growth at the re-entrant corner at a twin junction has been discussed by Faust and Johns [5] for the case of crystals bounded by the most stable planes (corresponding to the (111) planes in silicon). In this case, growth proceeds by nucleation at the re-entrant edge since this is energetically more favorable than two-dimensional nucleation. In the case discussed here, the bounding planes are not (111) planes and no re-entrant edge is formed by the twin. Consequently, rather than promoting growth, growth is slightly retarded in the vicinity of twins. However, twins do play a dominant role in determining the growth on small grained silicon substrates (section 4.3).

4.2.1.4 Implications for solar cells on multicrystalline epitaxial layers

The development of grooves at grain boundaries can have several implications for solar cells. The resulting nonplanarity of the layers makes them more difficult to process. At very deep grain boundaries, preferential diffusion of phosphorus down the grain boundaries may result in intimate contact between the heavily doped n+ emitter and the p+ substrate, giving rise to the possibility of a shunt due to trap assisted tunneling. Very deep grain boundary grooves, extending to within less than 5µm of the substrate-epi interface, have been observed for all the cooling rates studied.

In some cases, the structures developing near grain boundaries may prove detrimental to solar cell performance. Fig. 4.7 (a) shows an example of a grain boundary which does not exhibit an upward open structure. In this case, the emitter layer which would be diffused in or grown on top of the base may not be complete, giving rise to the possibility of shunting if a metal finger contacts both diffused and undiffused regions. Fig. 4.7 (b) shows a grain boundary with an unusually high grain boundary wall. Breakage of this wall after emitter formation could again result in an undiffused surface region, and the possibility of shunts.
Figure 4.7: Examples of grain boundaries in epitaxial layers which may lead to shunting of solar cells.
4.2.2 Influence of cooling rate and supersaturation on multicrystalline epitaxial layers

4.2.2.1 Surface morphology

Fig. 4.8 shows optical micrographs of epitaxial layers grown on polished substrates at cooling rates of 0.3 and 2°C/min respectively. The increased surface roughness at the higher cooling rate may be attributed to constitutional supercooling, with convection in the melt also playing a possible role in the process, as discussed in section 3.4.3. At sufficiently high growth rates, faceting is observed, analogous to the development of pyramids described in section 3.4.3.

4.2.2.2 Grain boundary growth

The cooling rate during growth may be expected to influence the amount of growth, or the lack of it, at the grain boundaries. At very low cooling rates, conditions in the melt approach equilibrium and the grain boundary angle may be expected to be given by eq. 4.2. At higher cooling rates, the supersaturation of the melt increases and growth kinetics play an important role in determining the grain boundary shape.

The influence of cooling rate and supersaturation on the development of grain boundary grooves was investigated in several experiments. In the first experiment, epitaxial layers were grown on both sides of a multicrystalline silicon substrate at cooling rates of 0.3 and 2.0°C/min, respectively. The amount of supersaturation used was 5°C. In a second experiment, epitaxial layers were again grown on both sides of a multicrystalline silicon substrate, with the melt supercooled by 5 and 25°C respectively prior to growth, and a cooling rate of 0.7°C/min. The procedure of growing on opposite sides of the same wafer enables the same location at a grain boundary, grown under different conditions, to be investigated. Finally, three epitaxial layers were grown at cooling rates of 0.3, 0.7 and 2.0°C/min on multicrystalline silicon substrates from adjacent sections of the growth ingot and displaying the same grain boundary structures. All growth surfaces had been mechanically polished and chemically etched prior to epitaxial layer deposition. Following growth, the wafers were cut on a dicing saw and etched for 5 seconds in Yang’s etch [6]. For each grain boundary investigated, the epitaxial layer thickness was measured at the bottom of the grain boundary groove and at a distance approximately 100µm away from the grain boundary, where the grain boundary no longer had any effect on the layer thickness. It must be kept in mind that the grain boundary character (i.e. the depth and width of the grain boundary groove) can change very rapidly and can thus be different even on the opposite surfaces of the same wafer. This is illustrated in fig. 4.9., which shows an area on an epitaxial layer containing several regions where the grain boundary character changes suddenly. Thus, the determination of the effect of the growth parameters requires the investigation of a large number of grain boundaries.
Figure 4.8: SEM micrographs of epitaxial layers grown on multicrystalline silicon substrates at cooling rates of (a) 0.3°C/min and (b) 2°C/min. The white lines are the metal fingers of the solar cell. Sample tilt 45°.
Figure 4.9: The surface of a multicrystalline epitaxial layer. In the encircled regions the grain boundary groove depth changes rapidly.

Fig. 4.10 (a) and (c) show the influence of the cooling rate on grain boundary growth. Based on this limited number of data points, there does not appear to be a significant change in the ratio $W_{gb}/W_{epi}$. However, as the cooling rate is increased, the epitaxial layer thickness decreases, from 45µm at a cooling rate of 0.3°C/min, to 30µm at 2.0°C/min. This decrease points to spontaneous nucleation in the melt: as the cooling rate increases, the upper layers of the melt reach high levels of supersaturation more quickly and spontaneous nucleation sets in. Once nuclei have formed, these will compete with the epitaxial layer for silicon. Similarly, changing the amount of supersaturation does not have a significant influence on the ratio $W_{gb}/W_{epi}$ (fig.4.10 (b)). Again the average layer thickness decreases from 40µm to 30µm as the amount of initial supersaturation is increased, due to the earlier onset of spontaneous nucleation.

4.2.3 Influence of surface preparation on the surface morphology

Fig. 4.11 shows epitaxial layers grown on substrates with the same grain boundary structures. The substrates were either mechanically polished with 1µm diamond paste, followed by a short chemical etch in HF/HNO$_3$ prior to growth (fig. 4.11 (a)) or only given a chemical etch (fig. 4.11 (b)). In both cases the cooling rate was 0.3°C/min. Fig. 4.11 (c) shows the surface of the substrate prior to growth. It can be seen that the roughness of the epitaxial layer is significantly greater than the roughness of the unpolished surface prior to growth. The dramatic influence of the surface roughness on the epitaxial layer morphology can again be attributed to constitutional supercooling as well as the particular stability of the Si (111) planes, as discussed in section 3.4.3.
Figure 4.10: The ratio of epitaxial layer thickness at a grain boundary, \( W_{gb} \), to the epitaxial layer thickness approx. 100\( \mu \)m away from the grain boundary, \( W_{epi} \), at several grain boundaries.
Figure 4.11: SEM micrographs of epitaxial layers grown on (a) a mechanically polished surface, and (b) a chemically etched surface. Sample tilt 45°.
4.2.4 Improvement of surface morphology by application of periodic meltback

The results of sections 3.4.3 and 4.2 indicate that constitutional supercooling can have a significant effect on surface morphology, resulting in rough surfaces which may present problems for the processing of solar cells. The morphology may be improved by employing periodic meltback during the growth. Fig. 4.12 illustrates a typical temperature profile. Shi and Green [7] used this approach to improve the morphology and grain size of silicon layers grown by LPE on glass substrates.

![Figure 4.12](image)

Figure 4.12: The temperature–time profile for epitaxial growth with periodic meltback.

Figure 4.11 (c): the chemically etched surface of the substrate prior to the growth of the epi layer. Sample tilt 75°C.
Epitaxial layers were grown using the periodic meltback technique on both polished and unpolished (but chemically etched) SILSO substrates. Typical cooling and heating rates were 0.7 and 2.0°C/min, respectively, while typical cooling and heating intervals were ΔTc=70 and ΔTh=20°C, respectively. Fig.4.13 shows cross sections of the same grain boundary from epitaxial layers grown without and with meltback. In both cases, grooves develop at the grain boundaries. However, in the case of layer grown with meltback, the sidewalls of the groove are less steep. Further, the growth near the grain boundary displays no raised sections on either side of it, resulting in a smoother layer. Comparison of the ratio W_g/\text{W_epi} at nearly identical grain boundaries in epitaxial layers grown with and without periodic meltback shows that the average depth of the grain boundary grooves appears to be slightly less in layers grown with periodic meltback (fig. 4.14).

Fig. 4.15 shows the surface of an epitaxial layer grown on an unpolished substrate. Compared to growth obtained without periodic meltback (fig.4.11), the surface is much smoother and faceting is absent. The surface also displays surface ripples with a period of several mm (not visible in the micrograph), indicating that convection cells were set up in the melt during the meltback cycles.

The above observations may be explained on the basis of the distribution of solvent during meltback: During the meltback cycles, silicon is transported from the wafer surface to the bulk, resulting in a decreasing silicon concentration with distance away from the wafer surface. Thus, any protuberances will encounter a more severely undersaturated melt and will be preferentially dissolved. Due to the absence of the raised grain boundary sidewalls, the supply of solute to the grain boundaries is improved during the growth phase, resulting in the observed slight reduction in the ratio W_g/\text{W_epi}.

The use of periodic meltback requires careful choice of cooling rates as well as the temperature intervals used for heating and cooling. The use of high cooling rates together with nearly equal heating and cooling intervals has been observed to lead to dissolution of the substrate rather than epitaxial layer growth, due to spontaneous nucleation in the melt. Once silicon crystallites have nucleated in the melt, these will float to the top of the melt. During subsequent growth/meltback cycles, the higher density of the solvent compared to silicon leads to the development of convection cells which result in the transport of silicon to the top of the melt, resulting in overall dissolution of the silicon wafer and the growth of the silicon crystallites on top of the melt (section 2.5).
Figure 4.13: The effect of periodic meltback on the development of grain boundary grooves. Cross sections of a grain boundary grown (a) without meltback and (b) with meltback. The dashed lines indicate the substrate-epi interface.
Figure 4.14: The ratio \( \frac{W_{gb}}{W_{epi}} \) for several grain boundaries in epitaxial layers grown with and without periodic meltback. The average layer thicknesses were 40\( \mu \)m and 30\( \mu \)m for the layers grown without and with meltback, respectively.

Figure 4.15: The surface of an epitaxial layer grown on an unpolished substrate using periodic meltback. Sample tilt 75°.

4.2.5 Growth of epitaxial layers from In/Cu solutions

The application of periodic meltback discussed in the previous section provides one possible method to improve the surface morphology of the multicrystalline epitaxial layers. Another approach may be the use of different solvents. Of particular interest are solvents with a higher silicon
solubility, as growth from these solvents also enables thicker layers to be grown in a shorter period of time.

Cu is a metal which has a high silicon solubility (43 at% at 1000°C), combined with a comparatively low solid solubility in silicon (3 x 10^{17} \text{cm}^{-3} at 1000°C [8]). Thus, Cu would appear to be an interesting solvent, either in its pure form or alloyed with another metal such as In, Sn or Al. The use of Cu as a solvent introduces potential problems, since Cu is known to be capable of degrading photovoltaic device performance in two ways. Firstly, Cu introduces trapping levels which act as recombination centres for minority carriers. Davis et al. [9] showed that, in single crystal silicon cells, Cu begins to affect the performance of single crystal cells at levels of approximately 10^{17} \text{cm}^{-3}. In multicrystalline silicon, Cu may also interact with the various defects and other impurities. The dramatic effect of Cu on the electrical activity of grain boundaries and dislocations has been demonstrated by Voigt and Strunk[10] using EBIC imaging. Secondly, cells made from Cu contaminated silicon have displayed non-ideal p–n junction effects, with ideality factors greater than 2. This was attributed to the formation of precipitates in the p–n junction region [9]. Nevertheless, Ciszek et al [11] obtained a high fill factor of 0.816 on a 5µm thick single crystal epitaxial layer grown from Cu solution. On multicrystalline silicon substrates, Wang and Ciszek [12] measured a minority carrier lifetime of 4.5µs, although the performance parameters reported so far for solar cells on multicrystalline layers grown from Cu solution have been low [11].

In order to investigate the applicability of Cu for LPE, epitaxial layers were grown on heavily doped Wacker SILSO substrates from In/Cu solutions with varying Cu concentrations. Epitaxial layer growth was carried out between 970 and 930°C, with a cooling rate of 0.7°C/min. Fig. 4.16 shows the effect of solution composition on epitaxial layer thickness. For each growth, the melt mass was approximately 53g.

In order to determine whether the addition of Cu could result in an improvement of the surface morphology at the grain boundaries, the epitaxial layer thickness at and away from grain boundaries was measured for layers grown from a pure In melt and from a 65at.%In/35at.%Cu melt. Fig. 4.17 compares the ratio W_{GB}/W_{epi} for several corresponding grain boundaries. It can be seen that the average depth of the grain boundary grooves is slightly less for layers grown from In/Cu solution. This reduced grain boundary depth may be the result of the higher degree of supersaturation which exists during growth from In/Cu solution, since the same cooling rates were used for both layers, but the rate of change of silicon solubility per unit temperature change is much higher for the case of growth from an In/Cu alloy. The high degree of supersaturation results in growth conditions which are further removed from equilibrium. Under these conditions, the importance of the difference in energy between the grain boundary and the intragrain regions may be reduced, leading to more uniform epitaxial growth.

A problem that was encountered when growing from In/Cu alloys was the formation of copper silicides. Following growth, it was often found that some of the melt remained back on the substrate wafer during cooling to room temperature. This leads to the formation of copper silicides,
which have different thermal expansion coefficients to silicon and can thus lead to fractures in the epitaxial layer and substrate [13]. As a consequence, the epitaxial layers grown from a solution with 10at% or more Cu were found to be brittle in those regions where some melt had remained on the wafer down to room temperature. This problem could probably be avoided, for example, in a sliding boat system, where the melt is wiped off the wafer following growth.

![Graph showing the thickness of epitaxial layers grown from In/Cu alloys as a function of the Cu concentration in the melt.](image)

**Figure 4.16**: The thickness of epitaxial layers grown from In/Cu alloys, as a function of the Cu concentration in the melt.

![Graph showing the ratio W_{gb}/W_{epi} at several grain boundaries for epitaxial layers grown from In and 65at.% In/35at.% Cu solutions.](image)

**Figure 4.17**: The ratio $W_{gb}/W_{epi}$ at several grain boundaries for epitaxial layers grown from In and 65at.% In/35at.% Cu solutions. The growth intervals were 970–600°C for the layer grown from In solution and 970–930°C for the layer grown from In/Cu solution. The average layer thicknesses were 30 and 50µm, for the layers grown from In and In/Cu, respectively. The cooling rate was 0.7°C/min in both cases.
4.3 Epitaxial layers on small grained multicrystalline silicon

Epitaxial layers were grown from In solution on S-Web, RGS and SSP ribbon wafers. The grain sizes on the S-Web and RGS substrates were of the order of several hundred microns, while the grains on the SSP ribbons were frequently smaller than 50µm across. Fig. 4.18 (a) shows a region of an epitaxial layer grown on RGS ribbon. It can be seen that in the regions where the grain sizes are very small, the epitaxial layer is rough due to facetting of the individual grains. Such a rough surface is likely to lead to significant problems during solar cells processing, as described in section 4.2.1.4. Fig. 4.18 (b) shows an epitaxial layer grown on an SSP substrate. In this case the epitaxial layer is so rough that processing of solar cells has become impossible.

Several factors are important in determining the surface morphology of layers grown by LPE on very fine grained multicrystalline silicon substrates. In the absence of coherent twin boundaries, silicon growth on each of the grains proceeds until stable (111) faces have developed, due the limited amount of growth at the grain boundaries. At this stage, further growth becomes difficult since it requires either growth at the grain boundaries, or growth on atomic or subatomic steps provided by dislocations [2]. Thus larger grains generally give rise to larger epitaxial crystals. Once a significant surface roughness has been established, constitutional supercooling leads to further enhancement of the growth of protruding crystals, while small crystals are starved of solute material.

Inspection of fig. 4.18 (b) also shows that twin boundaries play a dominant role in the growth of crystals on small grained substrates. In this case, the re-entrant corners at twin junctions appear to be a very effective source of atomic steps, as was demonstrated by Faust and Johns [5].

For epitaxial layers grown on SSP substrates, the use of periodic meltback did not result in a significant improvement of the surface morphology. An epitaxial layer grown using periodic meltback is shown in fig. 4.19. The lack of improvement of the surface morphology may be ascribed to the lack of growth at the grain boundaries, which is not sufficiently improved by periodic meltback. Similarly, growth from an In/Cu melt resulted in some improvement of the surface roughness, but the layers were still too rough for cell processing (fig. 4.20). Thus, it appears that LPE of silicon is a suitable technique for the production of solar-grade silicon films only when the grain size of the film is significantly larger than the layer thickness. This would place a lower limit on the tolerable grain size in the substrate of about 100µm, for epitaxial films of 20–50µm thickness.
Figure 4.18: SEM micrographs of epitaxial layers grown on multicrystalline silicon ribbon substrates. (a) Epitaxial layer grown on RGS ribbon and (b) a layer grown on an SSP substrate. The sample tilt in (a) was 55°. The epitaxial layer on RGS ribbon was grown at the Institute of Crystal Growth, Berlin.
Figure 4.19: An epitaxial layer grown on an SSP substrate using periodic meltback. The heating and cooling rates and intervals were 2.0 and 0.5°C/min, and 10 and 20°C, respectively. Growth was carried out from 970 to 750°C. The dashed line indicates the substrate–epi interface.

Figure 4.20: A cross sectional view of an epitaxial layer grown on an SSP substrate from a 35at%Cu/65at%In melt.
4.4 Electrical characterization of multicrystalline epitaxial layers

4.4.1 Determination of the minority carrier lifetime

4.4.1.1 Experimental

In order to determine the minority carrier lifetimes in multicrystalline epitaxial material, epitaxial layers were grown on cast multicrystalline substrates (Wacker SILSO, 0.015Ω·cm) at cooling rates of 0.3, 0.7 and 2°C/min. The doping concentration of the layers was determined by ECV profiling to vary from approximately $1 \times 10^{16}$ cm$^{-3}$ at the front to $1 \times 10^{17}$ cm$^{-3}$ at the rear. Two layers were grown on top of each other to obtain a thicker layer for greater mechanical strength. The multicrystalline substrates were selected from the same part of the growth ingot and so had nearly identical grain structures. Following growth, the substrates were completely removed by chemical etching, as outlined in sect. 3.6.2. Surface passivation was achieved by a light phosphorus diffusion of 300Ω·cm on both sides of the layer followed by growth of a thin passivating oxide at 900°C for 1 hour. Following processing, the average thickness of the layers was determined using a micrometer dial gauge.

The minority carrier lifetimes were determined by both the transient and quasi steady state PCD techniques. The transient PCD measurements were carried out as described in section 3.6.2.2. For the quasi steady state measurements, an inductively coupled PCD system was used. The entire sample was illuminated with a flash of several ms duration, while the sample area sensed by the inductor coil was 20mm in diameter. Measurements were carried out at light intensities of approximately 10 suns. At lower light intensities, interpretation of the data became difficult, due to the presence of minority carrier traps in the multicrystalline silicon and due to the limited sensitivity of the measurement system. The cells were in low injection throughout the measurements.

4.4.1.2 Results

Table 4.1 shows the values for the effective minority carrier lifetime obtained by the two PCD methods. For the extraction of the lifetimes by the QSS–PCD method, the mobility and the rate of photogeneration of excess electron–hole pairs were estimated as follows. The mobility in the epitaxial layers is assumed to follow the same doping dependence and to be 0.75 times the mobility in single crystalline silicon. Lölgen [14] estimated the minority carrier diffusion coefficient in lightly doped SILSO material to be 26 cm$^2$/s$^{-1}$, or 0.75 times the diffusion coefficient of intrinsic single crystalline silicon. An exponential doping profile is assumed in the base, extending from $1 \times 10^{16}$ cm$^{-3}$ at the front to $1 \times 10^{17}$ cm$^{-3}$ at the rear. The mean mobility is then:
\[ \mu_{av} = \frac{\int_0^{W_{epi}} (\mu_e(x) + \mu_h(x)) N(x) \, dx}{\int_0^{W_{epi}} N(x) \, dx} \]  
\[(4.3)\]

where \( x \) is the distance from the front of the epilayer in microns, \( N \) is the excess minority carrier concentration and the integration is carried out over the whole epitaxial layer. Under quasi steady-state conditions, the quasi fermi levels will be nearly constant throughout the layer, and the number of excess minority carriers is approximately inversely proportional to the doping concentration:

\[ N(x) = \frac{K}{e^{ax}} \]  
\[(4.4)\]

K is a constant and \( a \) is adjusted to give a change in \( N(x) \) by a factor of 10 over the thickness of the epilayer. From evaluation of the mean mobility, the 'effective' doping concentration of the layers was calculated as \( 5.2 \times 10^{16}\text{cm}^{-3} \).

The rate of generation of excess electron–hole pairs in the samples was estimated by modelling the current \( I_{test} \) flowing in a silicon cell with a bare front surface and no light trapping using PC–1D [15], under the condition of collection of all minority carriers and AM1.5 illumination. The reflectance of the rear surface was assumed to be 29%, the reflectance of long–wavelength light perpendicularly incident on the rear surface. The generation rate \( G \) is:

\[ G = \frac{I_{ref}}{I_{ref,1\text{sun}}} \frac{I_{test}}{q} \]  
\[(4.5)\]

where \( I_{ref} \) is the current flowing through the reference cell at a particular instant and \( I_{ref,1\text{sun}} \) is the current flowing through the reference cell under AM1.5 illumination conditions (\( I_{ref,1\text{sun}} = 38\text{mA/cm}^2 \)).

<table>
<thead>
<tr>
<th>Epi layer number and cooling rate</th>
<th>K175</th>
<th>K176</th>
<th>K178</th>
<th>K179</th>
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<tr>
<td></td>
<td>0.3°C/min</td>
<td>2°C/min</td>
<td>0.7°C/min</td>
<td>0.7°C/min</td>
<td>0.7°C/min</td>
</tr>
<tr>
<td>Wafer type</td>
<td>Multi</td>
<td>Multi</td>
<td>Multi</td>
<td>Multi</td>
<td>Cz</td>
</tr>
<tr>
<td>Substrate surface preparation</td>
<td>Polished</td>
<td>Polished</td>
<td>Polished</td>
<td>Chem. etch</td>
<td>Polished</td>
</tr>
<tr>
<td>Thickness (µm)</td>
<td>86</td>
<td>44</td>
<td>76</td>
<td>92</td>
<td>67</td>
</tr>
<tr>
<td>( I_{test}/I_{ref,1\text{sun}} )</td>
<td>0.640</td>
<td>0.610</td>
<td>0.635</td>
<td>0.642</td>
<td>0.630</td>
</tr>
<tr>
<td>Effective lifetime, ( \tau_{eff} ) (µs)</td>
<td>10.8</td>
<td>18.3</td>
<td>13.8</td>
<td>8.5</td>
<td>15.8</td>
</tr>
<tr>
<td>Microwave – PCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Effective lifetime, ( \tau_{eff} ) (µs)</td>
<td>10.8</td>
<td>8.5</td>
<td>10.6</td>
<td>12.6</td>
<td>17.6</td>
</tr>
<tr>
<td>QSS – PCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4.1: The effective minority carrier lifetimes \( \tau_{eff} \) measured by transient PCD and QSS–PCD.
Columns 1 to 3 show the results for epitaxial layers grown at various cooling rates, while column 4 shows the result from a layer grown on a substrate which had only been chemically etched. The surface morphology of the epitaxial layer prior to polishing was therefore similar to that shown in fig. 4.11 (b). The last column is for an epitaxial layer grown on a single crystal substrate. Despite the very different measurement conditions, the lifetime values obtained by the two techniques are in reasonable agreement with each other, except in the case of K176. A possible explanation for the much longer lifetime measured by transient PCD in this case is that minority carrier traps present in the multicrystalline material may not have been completely saturated by the bias light [16]. The trapping and de-trapping of minority carriers may thus have led to a slower decay curve and an erroneously large effective lifetime. The use of transient PCD for the measurement of the minority carrier lifetime in spatially inhomogeneous material such as multicrystalline silicon may also introduce errors due to the likely coexistence of regions with different lifetimes [17]. Thus the excess carriers recombine and decay away more rapidly in low lifetime regions, such as in the vicinity of grain boundaries, for example. Once the majority of excess carriers in these regions have recombined, excess carriers only remain in the high lifetime regions, resulting in a long tail in the decay curve. Extraction of the lifetime from this tail can thus result in a value that is representative of only the high quality regions of the material. In contrast, measurements using the QSS–PCD method result in a lifetime that is averaged over the whole of the sample area sensed by the detector.

As for the case of the single crystal epitaxial layers, no clear trend of change of lifetime with cooling rate is discernible. Under all growth conditions, high quality material could be grown. The corresponding diffusion lengths are in excess of 100µm, indicating that high cell efficiencies are possible in this material. The result of column 4 indicates that the roughness of an unpolished substrate, and the increased roughness of the resulting epitaxial layers, have no adverse effect on the material quality. Comparison of the effective lifetimes measured in the single crystal layer with the results of columns 1 to 4, as well as with the results of section 3.6.2.3, shows that i) the lifetimes in single crystal layers are significantly higher than those in multicrystalline layers, as expected, and ii) the effective lifetimes in section 3.6.2.3 are significantly lower than the actual lifetimes, due to the influence of surface recombination.

### 4.4.2 Electron beam induced current (EBIC) measurements

The growth of multicrystalline epitaxial layers on multicrystalline substrates produces a change in the grain boundary direction at the substrate–epi interface. It is likely that the grain boundary reorients itself in such a way as to minimise its total energy. Small angle grain boundaries in LPE layers have been observed to exhibit dislocation networks which have a simpler structure with a reduced number of dislocations, compared with their structure in the substrate [18]. Further, the purity of the epitaxial layer can be different (in most cases higher) from that of the substrate. Thus it is possible that the recombination activity of grain boundaries in epitaxial layers differs from their activity in the substrate.
In order to compare the grain boundary recombination activity in the substrate with that in the epitaxial layer, layers about 30µm in thickness were grown on 0.3Ω-cm, boron doped Wacker SILSO substrates. The substrate doping was chosen to be approximately the same as the doping in the epitaxial layer. Following growth, the layers were planarized and grooves of 0.8mm width, 70µm depth and spaced 1.6mm apart were cut with a dicing saw. This was followed by a short chemical etch to remove defects introduced by the sawing step. Solar cells were made using a low temperature process with a maximum process temperature of 900°C, in order to prevent fast diffusion of phosphorus down grain boundaries [19,20]. Electron beam induced current (EBIC) measurements were carried out using a Hitachi 2000 scanning electron microscope operating at 25kV and a Keithley 485 picoammeter. Grain boundaries which straddled the grooves cut into the wafer were selected and the EBIC response was measured at and away from the grain boundary, in the substrate as well as in the epitaxial layer. The results for four representative grain boundaries are displayed in table 3, where \( C = (I_{\text{background}}-I_{\text{GB}})/I_{\text{background}} \). In all cases, the EBIC response in the substrate and in the epilayer were found to be nearly identical, i.e. \( I_{\text{background,sub}} = I_{\text{background,epi}} \). No significant difference in the EBIC signal between the substrate and the epilayer was observed, either at or away from the grain boundaries.

The above results are in contrast with those of Albrecht et al. [21] who reported a significantly reduced electrical activity of grain boundaries in LPE grown material, as well as improved current collection in intragrain regions (higher \( I_{\text{background}} \)). There are several possible reasons for the different results:

- The substrate material used may have been of different quality
- The epitaxial layers for the results reported here were grown from Ga doped melts, while the layers used by Albrecht et al. were grown from pure In. The use of Ga may have led to a deterioration in the electronic quality of the epitaxial layer.
- For the layers used by Albrecht et al., Schottky contacts were used to enable carrier collection, while for the results reported here, a phosphorus diffusion was made. The diffusion may have had a gettering effect, thus improving the quality of the substrate.

<table>
<thead>
<tr>
<th>Grain boundary number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{sub}} )</td>
<td>0.38</td>
<td>0.24</td>
<td>0.13</td>
<td>0.19</td>
</tr>
<tr>
<td>( C_{\text{epi}} )</td>
<td>0.40</td>
<td>0.24</td>
<td>0.11</td>
<td>0.20</td>
</tr>
</tbody>
</table>

*Table 4.2*: Measured EBIC contrast at several representative grain boundaries, in the substrate and the epitaxial layer.
4.5 Fabrication of solar cells on multicrystalline epitaxial layers

4.5.1 The standard cell process

Many of the multicrystalline epitaxial layers required mechanical polishing in order to create a surface smooth enough for solar cell fabrication. Solar cells were then processed in a similar way as on single crystal layers (section 3.7). However, since multicrystalline silicon often degrades following high temperature treatments [22], and in order to minimize diffusion of impurities from the substrate into the epitaxial layer, it is desirable to avoid high process temperatures. Oxidation was therefore generally carried out at 900°C. Steam oxidation is necessary to grow an oxide sufficiently thick to mask against the phosphorus diffusion and therefore enable definition of the cell diffusion area. Table 4.3 lists the standard process for multicrystalline epitaxial cells.

<table>
<thead>
<tr>
<th>Step</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Steam oxidation</td>
<td>900°C, 2 hrs O$_2$+H$_2$O, then 30 min Ar. (150nm oxide)</td>
</tr>
<tr>
<td>Oxide patterning</td>
<td>Cell area, 2 × 2cm$^2$</td>
</tr>
<tr>
<td>n$^+$ phosphorus diffusion</td>
<td>860°C, 30min, N$_2$ (120Ω/cm)</td>
</tr>
<tr>
<td>Oxide removal</td>
<td>BHF</td>
</tr>
<tr>
<td>Rear aluminium deposition</td>
<td>500 – 1000nm Al</td>
</tr>
<tr>
<td>Oxide growth</td>
<td>900°C, 30min, O$_2$ then 30min Ar</td>
</tr>
<tr>
<td>Oxide patterning</td>
<td>Finger pattern in the front active area</td>
</tr>
<tr>
<td>Metallization</td>
<td>Front: 25nm Cr + 25nm Pd Rear: 500nm Al</td>
</tr>
<tr>
<td>Silver Electroplating</td>
<td>Finger width after plating approx. 24µm</td>
</tr>
<tr>
<td>Sintering</td>
<td>200 – 400°C, 10 – 30min, 4% H$_2$ / 96% Ar</td>
</tr>
</tbody>
</table>

Table 4.3: The standard solar cell process for cells on multicrystalline epitaxial layers

A problem that was occasionally encountered was shunting of the cells. In order to establish whether the diffusion of phosphorus down grain boundaries into a heavily doped substrate could create n$^+$/p$^+$ junctions and result in shunts due to trap assisted tunneling, some cells were made directly on heavily doped (0.015Ω·cm) Wacker SILSO substrates, as well as on heavily doped, 0.015Ω·cm, Cz wafers. The process is the same as that of table 3.6, with the following differences: no heavy diffusions were made under the contact fingers, and the wafers were not textured. Table 4.4 summarizes the parameters of the cells. In both cases, the cells were not shunted. This eliminates the creation of an n$^+$/p$^+$ junction as a possible cause of shunting, for epitaxial layers grown on the Wacker SILSO material.
<table>
<thead>
<tr>
<th>Substrate</th>
<th>Open circuit voltage (mV)</th>
<th>Short circuit current (mA)</th>
<th>Fill factor</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cz 0.015 Ω-cm</td>
<td>641</td>
<td>19.0</td>
<td>0.79</td>
<td>9.6</td>
</tr>
<tr>
<td>Wacker SILSO 0.015 Ω-cm</td>
<td>620</td>
<td>18.2</td>
<td>0.74</td>
<td>8.4</td>
</tr>
</tbody>
</table>

**Table 4.4**: The electrical parameters of cells fabricated on heavily doped substrates, at 25°C.

It was found that shunting of the cells could be avoided by careful attention to the cell process steps. The origins of the shunts were found to be a result of processing problems caused by the rough surface of the epitaxial layers. In particular, care had to be taken to ensure continuous coating of the epilayer surface, including all grain boundaries, with photoresist prior to front metal deposition, and to ensure complete exposure, development and oxide etching of the bottom of grain boundary grooves, prior to the phosphorus diffusion. Processing was also made significantly easier by mechanically polishing the epilayer surface prior to cell fabrication, or by employing periodic melt-back during epitaxial layer growth (section 4.2.4).

The results of solar cells on multicrystalline epitaxial layers made by the standard process are summarized in table 4.5. With the exception of G67c and 2K114, all the cells had a thin passivation oxide on the front, grown at 900°C in dry O₂. A very large spread in the values of the fill factor is apparent, pointing to a variety of processing problems as discussed above. Nevertheless, solar cells with good parameters were fabricated. All the electrical parameters of the cells (Jsc, Voc and FF) are consistently lower than the corresponding parameters of single crystal epitaxial cells processed in the same way, as a result of the lower material quality of both the epitaxial layer and the substrate. Note that one of the first cells made on a multicrystalline epitaxial layer grown using periodic meltback (14) resulted in the best efficiency for a cell fabricated on a heavily doped substrate so far. The epitaxial layer was sufficiently smooth not to require any polishing prior to cell processing.

### 4.5.2 Process variations

Several process variations were attempted in order to simplify the process as much as possible. Fig. 4.21 illustrates two of these. In both cases, the phosphorus diffusion is made over the entire surface. Cell isolation is achieved either by etching or by mechanical dicing. Cells made using the mesa etch process were consistently shunted. This can be attributed to the rough surface of the epitaxial layers, which allows etchant to seep into the cell area during the mesa etching step and etch through the diffusion in some areas. Table 4.6 lists the results of cells made using mechanical dicing. This process minimizes the number of photolithography steps and yields results as good as those achieved by the standard process.
Figure 4.21: Two possible process sequences for cells on multicrystalline epitaxial layers. (a) Mesa etch process involving i) Phosphorus diffusion, ii) Cell area definition with photoresist and etching and iii) oxidation and metallisation, and (b) Mechanical cell isolation involving i) Phosphorus diffusion and oxidation, ii) cell area isolation, etching of the diced regions and oxide removal, and iii) Al deposition, oxidation and metallisation.
<table>
<thead>
<tr>
<th>Epi ID</th>
<th>Substrate</th>
<th>Epi thickness (µm)</th>
<th>Epi polished (Yes/No)</th>
<th>Oxidation Temperature (°C)</th>
<th>Rear contact hole coverage</th>
<th>J&lt;sub&gt;SC&lt;/sub&gt; (mA/cm²)</th>
<th>V&lt;sub&gt;OC&lt;/sub&gt; (mV)</th>
<th>FF</th>
<th>Efficiency (%)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>G67c</td>
<td>Wacker 1Ω–cm</td>
<td>30</td>
<td>Yes</td>
<td>1100</td>
<td>7% Ga/Pd</td>
<td>25.5</td>
<td>606</td>
<td>0.787</td>
<td>12.2</td>
<td>Blue oxide acts as antireflection coating</td>
</tr>
<tr>
<td>S53G</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>30</td>
<td>No</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>21.2</td>
<td>615</td>
<td>0.775</td>
<td>10.1</td>
<td>Phosphorus oxide served as passivation oxide</td>
</tr>
<tr>
<td>S53H</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>20</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>19.1</td>
<td>625</td>
<td>0.786</td>
<td>9.4</td>
<td>Phosphorus oxide served as passivation oxide</td>
</tr>
<tr>
<td>S54F</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>25</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>21.1</td>
<td>600</td>
<td>0.683</td>
<td>8.6</td>
<td></td>
</tr>
<tr>
<td>S54G</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>25</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>21.3</td>
<td>612</td>
<td>0.576</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>S56I</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>25</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>20.4</td>
<td>605</td>
<td>0.611</td>
<td>7.5</td>
<td></td>
</tr>
<tr>
<td>G7</td>
<td>Eurosolare 1.5Ω–cm</td>
<td>45</td>
<td>No</td>
<td>900</td>
<td>100% Al (not alloyed)</td>
<td>21.3</td>
<td>602</td>
<td>0.725</td>
<td>9.3</td>
<td></td>
</tr>
<tr>
<td>3W3</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>25</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>21.1</td>
<td>622</td>
<td>0.738</td>
<td>9.7</td>
<td></td>
</tr>
<tr>
<td>3W4</td>
<td>Osaka Ti 0.9Ω–cm</td>
<td>30</td>
<td>Yes</td>
<td>900</td>
<td>100% Al (alloyed)</td>
<td>20.8</td>
<td>597</td>
<td>0.763</td>
<td>9.5</td>
<td></td>
</tr>
<tr>
<td>G4</td>
<td>Eurosolare 1.5Ω–cm</td>
<td>40</td>
<td>No</td>
<td>900</td>
<td>7% Ga/Pd</td>
<td>21.6</td>
<td>610</td>
<td>0.762</td>
<td>10.0</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.5: The electrical parameters of cells on multicrystalline epitaxial layers at 25°C, fabricated using the standard process
<table>
<thead>
<tr>
<th>Epi ID</th>
<th>Substrate</th>
<th>Epi thickness (µm)</th>
<th>Epi polished (Yes/No)</th>
<th>Oxidation Temperature (°C)</th>
<th>J_{sc} (mA/cm²)</th>
<th>V_{oc} (mV)</th>
<th>FF</th>
<th>Efficiency (%)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>G8</td>
<td>Eurosolare 0.2Ω-cm</td>
<td>50</td>
<td>No</td>
<td>900</td>
<td>100% Al</td>
<td>23.2</td>
<td>629</td>
<td>0.739</td>
<td>10.8</td>
</tr>
<tr>
<td>G6</td>
<td>Eurosolare 1.5Ω-cm</td>
<td>45</td>
<td>Yes</td>
<td>900</td>
<td>7% Ga/Pd</td>
<td>20.2</td>
<td>599</td>
<td>0.52</td>
<td>6.3</td>
</tr>
<tr>
<td>4F</td>
<td>Wacker SILSO 0.015Ω-cm</td>
<td>30</td>
<td>Yes</td>
<td>900</td>
<td>100% Al</td>
<td>20.8</td>
<td>621</td>
<td>0.64</td>
<td>8.3</td>
</tr>
<tr>
<td>11</td>
<td>Wacker SILSO 0.015Ω-cm</td>
<td>35</td>
<td>Yes</td>
<td>900</td>
<td>100% Al</td>
<td>18.0</td>
<td>612</td>
<td>0.656</td>
<td>7.2</td>
</tr>
<tr>
<td>2K114</td>
<td>Wacker SILSO 0.015Ω-cm</td>
<td>25</td>
<td>No</td>
<td>1000</td>
<td>100% Al</td>
<td>26.4</td>
<td>622</td>
<td>0.550</td>
<td>9.0</td>
</tr>
<tr>
<td>S19B</td>
<td>Wacker SILSO 1Ω-cm, B diff to 14 Ω/□</td>
<td>30</td>
<td>Yes</td>
<td>900</td>
<td>100% Al</td>
<td>20.6</td>
<td>614</td>
<td>0.790</td>
<td>10.0</td>
</tr>
<tr>
<td>S19C</td>
<td>Wacker SILSO 1Ω-cm, B diff to 8.2 Ω/□</td>
<td>25</td>
<td>Yes</td>
<td>900</td>
<td>100% Al</td>
<td>19.9</td>
<td>596</td>
<td>0.788</td>
<td>9.3</td>
</tr>
<tr>
<td>14</td>
<td>Wacker SILSO 0.015Ω-cm</td>
<td>25</td>
<td>No</td>
<td>900</td>
<td>100% Al</td>
<td>20.8</td>
<td>630</td>
<td>0.793</td>
<td>10.4</td>
</tr>
</tbody>
</table>

Table 4.5 continued: The electrical parameters of cells on multicrystalline epitaxial layers at 25°C, fabricated using the standard process.
<table>
<thead>
<tr>
<th>Epi ID</th>
<th>Substrate</th>
<th>Epi thickness (µm)</th>
<th>Epi polished (Yes/No)</th>
<th>Oxidation Temperature (°C)</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>$V_{oc}$ (mV)</th>
<th>FF</th>
<th>Efficiency (%)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>7W5/K232</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>40</td>
<td>No</td>
<td>1000</td>
<td>25.6</td>
<td>627</td>
<td>0.787</td>
<td>12.6</td>
<td>Thick oxide; thickness not optimal for AR properties</td>
</tr>
<tr>
<td>8W4/K192</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>40</td>
<td>Yes</td>
<td>1000</td>
<td>21.5</td>
<td>614</td>
<td>0.77</td>
<td>10.2</td>
<td>Final oxide on front was a thin oxide grown at 900°C</td>
</tr>
<tr>
<td>8W2/2019</td>
<td>Wacker SILSO 0.015Ω–cm</td>
<td>20</td>
<td>No</td>
<td>1000</td>
<td>26.5</td>
<td>607</td>
<td>0.73</td>
<td>11.8</td>
<td>Thick oxide, thickness not optimal for AR properties</td>
</tr>
</tbody>
</table>

Table 4.6: The parameters of cells on multicrystalline epitaxial layers at 25°C, fabricated using mechanical cell isolation
4.5.3 Addition of TiO₂ antireflection coatings and cell encapsulation

The addition of TiO₂ antireflection coatings together with cell encapsulation under low iron glass results in significant increases in cell performance. The TiO₂ layers were thermally evaporated onto the cells at a temperature of 200–220°C. Table 4.7 lists some of the results obtained. TiO₂ evaporation and encapsulation result in an improvement of over 40% in the short circuit current of the cells, while \( V_{oc} \) improves marginally as a result of the higher \( J_{sc} \). The high efficiency of 15.4% on G8 was achieved despite the poor fill factor of this cell, a result of a high series resistance. A better fill factor of 0.78 would have resulted in an efficiency of nearly 17%. The substrate of this cell would have contributed to \( J_{sc} \) due to the low substrate doping and therefore a high potential minority carrier lifetime. However, modelling results indicate that the current originating from the substrate for a lifetime of 2µs, expected for this type of substrate following processing, is only about 0.5mA/cm². The efficiency of cell I4 is limited by the relatively low short circuit current. Increasing the epitaxial layer thickness to 50µm is expected to increase efficiencies to at least 16%. Due to the high substrate doping, the contribution of the substrate to the photocurrent is negligible.

<table>
<thead>
<tr>
<th>Cell ID</th>
<th>( J_{sc} )</th>
<th>( V_{oc} )</th>
<th>Fill Factor</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>G7</td>
<td>30.9</td>
<td>610</td>
<td>0.728</td>
<td>13.7</td>
</tr>
<tr>
<td>G8</td>
<td>33.8</td>
<td>639</td>
<td>0.708</td>
<td>15.4</td>
</tr>
<tr>
<td>I4</td>
<td>30.0</td>
<td>639</td>
<td>0.790</td>
<td>15.2</td>
</tr>
</tbody>
</table>

Table 4.7: The electrical parameters of cells following TiO₂ deposition and encapsulation, at 25°C.

4.6 References


[16] A. Stephens, private communication


[22] M. Stocks, private communication
Chapter 5

Numerical Modelling of Drift Fields in Thin Film Silicon Solar Cells

5.1 Introduction

The efficiency of thin film silicon cells is dependent on several parameters such as the minority carrier lifetime and diffusion length, the surface recombination velocities, the thicknesses of the various device regions, the doping concentrations and the degree of light trapping in the cell structure. Some of these parameters, such as the doping concentrations and the thicknesses of the device regions, can be chosen relatively freely while others, such as the degree of light trapping and the minority carrier lifetimes are dependent on the particular process being used. Thus, the deposition of silicon on glass will yield very low minority carrier lifetimes but good light trapping, while the epitaxial growth on multicrystalline silicon substrates results in good material quality but a loss of light trapping. The choice of a suitable solar cell process and the optimal choice of the design variables therefore require the evaluation of the efficiency potential of a range of solar cell structures. In addition, thin film silicon deposition techniques such as LPE or CVD enable a variation of the doping level in the deposited film during the growth process [1], leading to a dopant gradient in the absorber layer of the cell. Such a dopant gradient cannot easily be achieved by any of the other silicon growth techniques. Since the electric 'drift' field resulting from nonuniform base doping is potentially beneficial to solar cell performance, evaluation of its effect is of practical importance. The classical solar cell theory [2] was developed assuming uniform base doping and therefore does not strictly apply to these cells.

Various analytical models for the transport and recombination of current carriers in semiconductor regions with non-uniform dopant densities have been developed and used to explore the performance of drift field cells [3–13]. These models have been steadily refined in an attempt to take into account the variations of mobility and lifetime with doping, and to include important effects such as bandgap narrowing. Lindholm and Chen [7] derived expressions for the dark saturation current $J_0$, taking into account a power law dependence of lifetime on doping density, but neglecting mobility variations with doping. Instead they employed average values of the minority carrier mobility $\mu$ and diffusion coefficient $D$. Verhoef and Sinke [13] obtained closed form solutions for the dark saturation current for the cases of power law or exponential doping profiles, approximating experimentally observed variations of mobility and minority carrier lifetime by power–law dependencies. Their solutions, in the form of second–class Bessel functions, were free of integrals of the minority carrier transport parameters over the semiconductor region being analyzed. However, while the approximations for mobility are accurate in the doping range $10^{17}$ to $10^{19}$cm$^{-3}$, a greater range in doping densities is difficult to model accurately by a simple power law.
dependence and the calculations are restricted to these fairly high doping levels. Short circuit current expressions were not obtained.

Elnahway et al. [12] expanded on the work of Kuivalainen [8] to obtain expressions for both the dark saturation current as well as the short circuit current \( J_{sc} (\lambda) \) for monochromatic light. Integration of \( J_{sc} (\lambda) \) over the solar spectrum gives the short circuit current in the base of the solar cell. A major problem with this work is the unrealistic variation of mobility with doping: \( \mu_n(0) \) is adjusted to give an excellent fit at low doping levels, but at higher doping levels the approximation is gravely in error. For example, at a doping level of \( 10^{18} \text{cm}^{-3} \), the above model would give \( \mu_n = 1.73 \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \), while experimentally \( \mu_n \) is around 250 \( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) for high quality single crystal silicon.

The application of quasi-analytical solutions for both \( J_0 \) and \( J_{sc}(\lambda) \) initially developed for emitter regions by Park et al. [14] to the case of non-uniformly doped base regions is straightforward [15]. While these improved models can properly account for the Si transport parameters, it is not easy to include such effects as light trapping and high injection. A numerical approach is frequently a better option in order to account for these effects. Some numerical models have been developed and used to obtain more accurate values for the cell parameters. Lindholm et al. [9] used several different lifetime models to determine the cell parameters for \( p^+/n(n(x)) \) structures. However, neither the base doping nor the cell thickness were optimized with respect to cell efficiency.

The purpose of the modelling presented in this chapter was to determine the efficiency potential of a range of cell structures and to make a realistic assessment of base drift field (BDF) cells, by comparing the performance of such cells with that of cells having constant base doping. The modelling program PC-1D [16] was used in order to allow the material properties to be modelled accurately and all the cell parameters to be determined. PC-1D was chosen because it is a relatively mature program, which allows one to place more confidence in the modelling results.

### 5.2 Modelling of drift fields

#### 5.2.1 Cell structure

Fig. 5.1 illustrates the basic solar cell structure that was assumed. Only the base region of the cell is shown for clarity. The modelling was restricted to \( n+/p(x)/p+ \) cells throughout. An exponential doping profile is assumed in the base region, with doping levels at the front and rear of the lightly doped region of the base of \( N_r \) and \( N_n \), respectively. This is representative of silicon films grown by LPE, which have displayed approximately exponential doping profiles [1]. The exponential doping gradient results in an electric field of constant magnitude that pushes the minority carriers (electrons) towards the \( p-n \) junction. In some cells, the base region is terminated by a heavily doped \( p \) type layer. For the case \( N_r \ll N_n \), the high–low junction created at the interface results in a strong electric field which reflects minority carriers back into the base of the cell and thus reduces recombination at the rear surface. This 'back surface field' (BSF) can be formed in practice in a

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variety of ways, such as by depositing the thin base layer on a heavily doped silicon substrate. At the rear of the cell a surface of reflectivity $R$ and surface recombination velocity $S$ is assumed.

\[ \log(N_a) \]

\[ N_h \]

\[ N_r \]

\[ N_f \]

\[ W_b \]

\[ W_h \]

**Figure 5.1**: The base region of the solar cell that was modelled. An electric field exists in the base when $N_r > N_f$, creating a force on minority carrier electrons directed towards the p–n junction.

A reasonable quality front n$^+$ emitter is modelled with a sheet resistance of 150$\Omega/$$\square$, and a thickness of approximately 500nm. The saturation current density of the front surface is $5 \times 10^{-14}$Acm$^{-2}$ (corresponding to an open circuit voltage cap of 705mV). This emitter allows for effects in the base region to be clearly observable. Antireflection control is included by assuming zero front reflectivity. The internal reflectivity at the front surface of the cell is set to 92%, the lambertian limit for randomized light. The cell is illuminated with 100 mAcm$^{-2}$ of light of AM 1.5 spectrum (global) at 25°C. It should be noted that in the model, light traverses the cell perpendicular to the front surface, whereas in practice texturization techniques result in the light being coupled into the cell at a range of angles, and therefore in increased optical path lengths. Thus, real devices would absorb light more efficiently than the devices modelled here, and would have slightly larger values of the short circuit current, all other parameters being equal.

### 5.2.2 Material parameters

The values for the Auger recombination coefficient and for the intrinsic carrier density are taken as $C_p = 9.9 \times 10^{-32}$cm$^6$/sec and $n_i = 1.0 \times 10^{10}$cm$^{-3}$ at 300K [17, 18]. Electrical bandgap narrowing is modelled as

\[ p_{eq}n_{eq}=n_f^2(T)e^{(\Delta E_g)/kT}, \text{with } \Delta E_g=C_a \ln(N_d/N_{a0}) \] (5.1)
where $p_{\text{eq}}$ and $n_{\text{eq}}$ are the electron and hole concentrations at thermal equilibrium, $N_{a0} = 2.3 \times 10^{17}\text{cm}^{-3}$, and $C_a = 17.8\text{mV}$ for p-type silicon [19].

The default PC-1D parameters are used to account for the variation of electron and hole mobilities with doping. The minority carrier mobilities are taken from the data of del Alamo et al. [20] and Swirhun et al. [21].

### 5.3 Case studies

Two different lifetime models are considered. For low-level injection conditions the dependence of lifetime on doping is:

$$\frac{1}{\tau} = \frac{1}{\tau_{\text{SRH}}} + C_P p^2$$  \hspace{1cm} (5.2)

with

$$\tau_{\text{SRH}} = 5000, \ 500 \text{ or } 50\text{ns}$$  \hspace{1cm} (model (1))

$$\tau_{\text{SRH}} = \frac{\tau_0}{1 + N_a/N_{\text{ref}}}, \ \tau_0 = 5000\text{ns}, \ N_{\text{ref}} = 2 \times 10^{16}\text{cm}^{-3}$$  \hspace{1cm} (model (2))

where $\tau_{\text{SRH}}$ is the Schottky–Read–Hall lifetime and the term $C_P p^2$ represents the fundamental Auger recombination process. Radiative recombination is neglected. In model (1) $\tau_{\text{SRH}}$ is independent of doping, while in model (2) $\tau_{\text{SRH}}$ depends inversely on doping at high dopant concentrations. A significant decrease in the minority carrier lifetime of cast multicrystalline silicon at higher dopant levels, consistent with the form of model (2), has been observed by several workers for various types of silicon, including cast polycrystalline silicon, ribbon grown silicon and irradiated silicon [22–24].

Three different cell designs are modelled. These are chosen to span the range of most practical devices found in the literature. Both high and low recombination rates at the rear surface are analyzed, as is the presence or absence of a BSF. Light trapping quality ranging from excellent to nil is modelled.

### 5.3.1 Cells with a moderately passivated, high reflectivity rear surface

The first case considered is that of cells having both a BDF and a BSF. The BSF is incorporated by assuming a $p^+$ region at the rear of the cell with $W_h = 3\mu\text{m}, N_h = 5 \times 10^{18}\text{cm}^{-3}$. The reason for selecting this relatively moderate value for the dopant density of the heavily doped region is that at doping levels significantly higher than $5 \times 10^{18}$, lattice strain and the introduction of misfit dislocations during the growth of the more lightly doped base often have detrimental effects on the electronic quality of the base region. The value of the rear surface recombination velocity $S$ is set to $D_h/L_h$, where $D_h$ and $L_h$ are the values of the electron diffusion coefficient and the diffusion length in the heavily doped region of the base, respectively. Inspection of eqs. (1.8) and (1.10)
shows that in this case, the thickness of the heavily doped rear only influences slightly the collection of photogenerated carriers but has no influence on the dark saturation current. The rear reflectivity is set to 99%. For each lifetime model, optimization of the cell is carried out by evaluating the cell efficiency at many points on a three-dimensional grid, with $N_f$, $N_r$ and $W_b$ as the three variables.

As an example of the optimization procedure, fig. 5.2 shows contour plots for cells with a 5µs minority carrier lifetime in the base at low doping levels, with lifetime depending on doping only through Auger recombination (model (1)). Table 5.1 summarizes the results by comparing the efficiencies of the optimized BDF cells (having $N_f \neq N_r$) with the efficiencies of cells having the classical BSF cell structure with uniform base doping. Since the classical BSF cells are a special case of the BDF cells modelled here, the efficiency of the BDF cells will always be greater than or equal to that of the BSF cells, $\eta_{BDF} \geq \eta_{BSF}$. It can be seen from Table 5.1 that the improvements achieved through the incorporation of drift fields are small. Due to the assumption of excellent light trapping, even very thin devices are still efficient at capturing light and so the optimum cell thickness shifts towards very low values around 3µm for low quality material. Due to the difficulty in defining realistic boundaries on the values that the base thickness may assume, no attempt was made to limit the modelling to a certain range of thicknesses. Very thin (<10µm) c-Si solar cells have been considered by several workers and appear to be feasible [25]. For a thicker than optimum base, a drift field offers a larger advantage than that shown in Table 1.

5.3.2 Cells with high recombination velocity, high reflectivity rear surface

In the second class of cells, the recombination velocity at the rear is set to $S = 1 \times 10^7$ cm/s. This would correspond to a full area metallization at the rear surface. Usually the reflectivity of such a structure is lower than when a dielectric material is placed in between the metal and Si. Nevertheless, to facilitate comparison with the previous case, $R = 99\%$ is assumed. Cells incorporating a drift field only but no BSF are modelled using $W_b = 0$. Optimization again involves evaluating the cell efficiencies at many points on the 3-dimensional grid with variables $N_f$, $N_r$ and $W_b$. These results are compared with the results of cells with a BSF only but no BDF, that is $N_f = N_r = N_a$. In this case, the three variables consist of $W_b$, $W_h$ and $N_a$. As a final case, cells incorporating both a drift field and a high–low junction are considered (as in section 5.3.1, except for the different value of $S$).

A major function of the BDF in this class of cells is to provide some shielding effect from the high recombination velocity rear surface. The results of Table 5.2 indicate that this requires large changes in doping concentrations over more than two orders of magnitude. The efficiency differences between cells incorporating either a BSF, a BDF or both are modest in all the cases modelled. The most significant effect of a BDF is a significant increase in the optimum base thickness, due to the fact that the BDF results in an improved collection efficiency of photogenerated minority
carriers. This may be of practical interest particularly in the case of material with low lifetimes, where the optimum cell thickness decreases below 10µm.

The results of Table 5.2 also indicate that a high surface recombination velocity is not an insurmountable problem for thin silicon cells, since both a BDF and a BSF are capable of producing creditable efficiencies.

5.3.3 Cells with no light trapping

As a third structure we consider the case of a thin film deposited on a thick and highly doped silicon substrate. The rear reflectivity is set to zero and the thickness of the highly doped region, \( W_h \), is set to infinity, with \( N_h = 5 \times 10^{18} \text{ cm}^{-3} \). This represents the worst possible optical design since no light is reflected back from the rear surface of the cell at all, and since light traverses the cell perpendicular to the front surface. The variables to be optimized are \( N_r \), \( N_f \) and \( W_b \). As in the first class of cells, the classical BSF only case can be obtained by making \( N_f = N_r \).

Table 5.3 shows that a drift field now offers a more significant efficiency advantage over BSF cells. This can be attributed to the fact that the absence of any light trapping favours much thicker devices. Since the rear surface is reasonably well passivated by the high-low junction at the substrate–epi interface, the main challenge is the efficient collection of photogenerated minority carriers in the bulk. A BDF provides a moderate advantage due to improved carrier collection efficiency. This is again reflected in the larger values for the optimal base thickness, as well as in the larger values for the short circuit current, compared to the BSF only case. For example, for the case of a 500ns base lifetime, \( J_{sc,BDF} = 34.3 \text{ mA cm}^{-2} \) while \( J_{sc,No BDF} = 32.3 \text{ mA cm}^{-2} \). However, variations in dopant density of more than two orders of magnitude are required in some cases.
Figure 5.2: Contour plots of cell efficiency as a function of the front and rear dopant concentrations, for the case of the lifetime model (1) with $\tau_0 = 5\mu$s and (a) $W_b=15\mu$m, (b) $W_b=25\mu$m and (c) $W_b=35\mu$m. The straight line indicates the zero BDF case.
### Table 5.1:

The efficiencies of optimized cells incorporating both a base drift field and a back surface field, or only a back surface field, for the case of excellent light trapping and a moderately well passivated rear surface.

<table>
<thead>
<tr>
<th>Lifetime model</th>
<th>Model (1)</th>
<th>Model (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\tau_0=5\mu s$</td>
<td>$\tau_0=500\text{ns}$</td>
</tr>
<tr>
<td>Electric field type</td>
<td>BDF + BSF</td>
<td>BSF only</td>
</tr>
<tr>
<td>$\eta_{\text{max}}, %$</td>
<td>22.7</td>
<td>22.6</td>
</tr>
<tr>
<td>$N, \text{cm}^{-3}$</td>
<td>$3 \times 10^{16}$</td>
<td>$1 \times 10^{17}$</td>
</tr>
<tr>
<td>$W_b, \mu m$ (optimum)</td>
<td>35</td>
<td>25</td>
</tr>
</tbody>
</table>

### Table 5.2:

The efficiencies of optimized cells incorporating either a base drift field, a back surface field or both, for the case of excellent light trapping and a high rear surface recombination velocity.

<table>
<thead>
<tr>
<th>Lifetime model</th>
<th>Model (1)</th>
<th>Model (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\tau_0=5\mu s$</td>
<td>$\tau_0=500\text{ns}$</td>
</tr>
<tr>
<td>Electric field type</td>
<td>BDF</td>
<td>BSF</td>
</tr>
<tr>
<td>$\eta_{\text{max}}, %$</td>
<td>22.0</td>
<td>21.6</td>
</tr>
<tr>
<td>$N, \text{cm}^{-3}$</td>
<td>$3 \times 10^{16}$</td>
<td>$5 \times 10^{18}$</td>
</tr>
<tr>
<td>$W_b, \mu m$ (optimum)</td>
<td>80</td>
<td>40</td>
</tr>
<tr>
<td>Lifetime model</td>
<td>Model (1)</td>
<td>Model (2)</td>
</tr>
<tr>
<td>----------------</td>
<td>-----------</td>
<td>-----------</td>
</tr>
<tr>
<td></td>
<td>$\tau_0=5\mu s$</td>
<td>$\tau_0=500\text{ns}$</td>
</tr>
<tr>
<td>Electric field type</td>
<td>BDF + BSF</td>
<td>BSF</td>
</tr>
<tr>
<td>$\eta_{\text{max}}, %$</td>
<td>20.6</td>
<td>19.9</td>
</tr>
<tr>
<td>$N, \text{cm}^{-3}$</td>
<td>$3 \times 10^{16}$</td>
<td>$1 \times 10^{17}$</td>
</tr>
<tr>
<td>$W_b, \mu\text{m (optimum)}$</td>
<td>100</td>
<td>75</td>
</tr>
</tbody>
</table>

**Table 5.3:**

The efficiencies of optimized cells incorporating both a base drift field and a back surface field, or only a back surface field, for the case of no light trapping.
5.4 The effective diffusion length $L_{\text{eff}}$

The concept of an effective diffusion length has been developed by several authors [26,27]: under the assumptions of constant values of $E$, $\tau$ and $D$, the transport equation for minority carriers can be solved to give a solution for the minority carrier concentration profile, similar to the solution in the case of zero electric field. By analogy with the zero field case, an effective diffusion length can be defined:

$$\frac{1}{L_{\text{eff}}} = \frac{1}{2L} \left( \sqrt{\frac{(E/E_c)^2 + 4 - E/E_c}{E/E_c}} \right)$$  \hspace{1cm} (5.3)$$

with

$$E = \frac{kT}{qW_b} \ln\left(\frac{N_r}{N_f}\right)$$  \hspace{1cm} (5.4)$$

where $L$ is the minority carrier diffusion length in the absence of an electric field and $E_c = kT/qL$ [26]. According to eq. (5.3), the effective diffusion length $L_{\text{eff}}$ is significantly larger than $L$ whenever $E \geq E_c$. Evaluating $L_{\text{eff}}$ for the optimized drift fields in Tables 5.1 to 5.3 by using the value of the diffusion length $L$ at a dopant concentration intermediate between the front and rear values, one finds that the values of $L_{\text{eff}}$ are between 3 and 10 times the value of $L$. However, this diffusion length enhancement does not translate into significant increases in solar cell efficiency in most cases. In fact, the largest efficiency increases (for the cases of 50ns and 500ns base lifetimes in Table 5.3) actually correspond to the smallest calculated ratios of $L_{\text{eff}}/L$. This points out that a calculation of $L_{\text{eff}}$ by itself does not reveal the real significance of the incorporation of a drift field. Other important factors, such as the degree of light trapping in the device and recombination at the surfaces, must be considered.

5.5 The costs and benefits of light trapping in thin film cells incorporating drift fields

Fig. 5.3 compares the maximum efficiencies that were obtained by modelling each of the three device structures. It can be seen that the efficiency gain that can be obtained by incorporating light trapping into the device structure, assuming that the material quality is not altered, increases with decreasing minority carrier lifetime and varies from 2% for a 5µs lifetime to over 4% for a 50ns lifetime. However, if the rear surface recombination velocity is high, this difference is reduced. Also, if the optical path length of light through the cell is increased by texturization, or if the light trapping scheme is less ideal than the one that was modelled, the efficiency differences will be reduced. Since in practice the achievement of light trapping comes at the expense of either reduced material quality (e.g. deposition of silicon on a foreign substrate) or increased complexity and cost (e.g. the use of ZMR), cell structures which sacrifice the benefit of light trapping may still be attractive from a commercial point of view, particularly if the minority carrier lifetimes of the silicon films are relatively large ($\tau \geq 1\mu$s).
![Diagram showing cell efficiencies for different models and parameters](image)

**Figure 5.3**: The maximum cell efficiencies for each of the three cell structures modelled. i) to iii): model (1) with $\tau_0 = 5000, 50, 50$ ns; iv): $\tau \propto 1/N$

## 5.6 Conclusions

The results of the modelling carried out indicate that the benefits of a base drift field are rather small and depend on the degree of light trapping incorporated into the device structure, on limitations on the base thickness of the solar cell and on the magnitude of the dopant variations that can be practically achieved. The potential benefit of a BDF is to increase the collection probability of photogenerated minority carriers, resulting in a greater optimum base thickness. The benefit is realized in devices with poor light trapping, due to the obvious advantage in increasing the base thickness in these devices, or in poor lifetime material where practical considerations may restrict the base thickness to larger than optimal values. However, in all the cases studied, the advantage of a drift field is so small that its incorporation would probably only make sense if it arose naturally as part of the silicon growth process.

## 5.7 References


Chapter 6

Summary and Directions for Future Work

6.1 Summary

In this work, thin crystalline silicon films were grown by the LPE technique on single crystal and multicrystalline silicon substrates, with the aim of evaluating and demonstrating the potential of such films for the fabrication of high efficiency solar cells.

The epitaxial layers were grown by the tipping boat method. A very simple LPE system was designed and constructed that did not require evacuation of the LPE tube prior to growth in order to achieve an oxide free silicon surface. Good quality epitaxial layers could be grown in a H₂ ambient when the growth was initiated above 900°C. It was shown that In can catalyze the oxidation of silicon. For example, a 4 hour oxidation at 960°C in a hydrogen ambient containing less than 1 part per thousand by weight of H₂O, resulted in an oxide up to 3.5µm thick.

Smooth and specular layers were grown on single crystal substrates from In and In/Ga solutions. The layers were found to be essentially free of extended defects. DLTS measurements did not reveal any deep level traps, indicating that the layers are of high purity. Spreading resistance analysis of layers grown from In solution showed the parts of the layers grown below 900°C to be n doped due to the presence of phosphorus in the melt, as shown by SIMS analysis. Achievement of p doped epitaxial layers therefore required the addition of small amounts of Ga to the melt.

Photoconductivity measurements on single crystal epitaxial layers showed the material to be of good quality for all the cooling rates investigated. In all cases, the diffusion length was well in excess of 100µm, or more than twice the thickness of the films. Solar cells fabricated on single crystalline epitaxial layers grown on heavily doped substrates reached efficiencies up to 17% with an SiO₂ antireflection coating. Cells fabricated on single crystalline epitaxial layers grown on lightly doped substrates displayed efficiencies of nearly 18% after the substrate had been completely removed. These efficiencies could be further improved through the use of better single or double layer antireflection coatings. Analysis of the open circuit voltages of these cells confirmed that the minority carrier lifetime in the films was in excess of 10µs.

Epitaxial layers grown on large grained, cast multicrystalline silicon substrates displayed good grain-to-grain thickness uniformity with maximum thickness variation of 15% of the layer thickness, despite the essentially random orientation of the grains in the substrates. At the grain boundaries, grooves of various depths were observed following epitaxial layer growth, and the grain boundary direction was seen to change abruptly at the substrate-epi interface. These observations could be explained by considering the energy required for atomic attachment at a grain boundary, and by the fact that the LPE method is a near equilibrium growth process, so that growth proceeds in such a way as to minimize the free energy of the epitaxial layer.
The influence of surface preparation and the cooling rate on the surface morphology and the growth at the grain boundaries was investigated. It was found that constitutional supercooling plays an important role in determining the surface morphology. The use of the periodic meltback technique, which consists of alternating growth and meltback cycles, resulted in significantly smoother layers, which were easier to process into solar cells.

Epitaxial layers deposited on small grained multicrystalline silicon substrates showed a gradual roughening, as the length of grain boundaries per unit area increased. When the grain size was of the order of, or smaller than the film thickness, facetting of the individual grains occurred and the layers were too rough for processing into solar cells. In this case, the use of periodic meltback did not result in a significant improvement of the surface morphology, because the surface morphology is determined by the lack of growth at the grain boundaries.

Photoconductivity measurements on multicrystalline epitaxial layers grown from In/Ga solutions again yielded high minority carrier lifetimes of around 10µs for all the growth conditions investigated. Importantly, growth on a rough substrate surface was not found to result in a degradation of material quality, compared to layers grown on polished surfaces. The high minority carrier lifetimes indicate the potential for cells with efficiencies in excess of 16% to be fabricated on these layers.

Solar cells on multicrystalline epitaxial layers displayed a large spread in the electrical parameters, particularly the fill factor FF. However, by paying careful attention to the cell process and through the use of sufficiently planar epitaxial layers, high cell efficiencies were achieved. To date, an efficiency of 15.4% has been realized, and there exists a clear potential for even higher efficiencies up to 17%.

Thin film silicon cells incorporating electric drift fields in the base of the cell were modelled using PC-1D in order to determine the optimum cell parameters (cell thickness and doping profile) for three different cell designs. It was found that, in most cases, the presence of drift fields does not result in a significant improvement in cell performance. The results also indicated that even thin film cells not incorporating any light trapping can achieve efficiencies sufficiently high to be commercially interesting, provided minority carrier lifetimes of approximately 1µs or higher can be maintained in the active layer.

6.2 Future directions

Work on liquid phase epitaxy of silicon to date has confirmed the ability of this approach to produce thin silicon films of sufficient quality for the fabrication of high efficiency solar cells. In order for the LPE process to become economically viable for large scale solar cell production, several interrelated issues have to be addressed. These include the question of the best solvent to carry out the LPE process, the choice of a suitable solar cell structure and the development of an LPE system capable of high throughput rates at low cost.
6.2.1 Optimal solvent for the LPE process

The results of this thesis, as well as those of other authors have shown that In is a good solvent for the LPE process, capable of producing high quality silicon layers. However, on multicrystalline silicon substrates, the roughness of the layers, resulting chiefly from the development of grain boundary grooves, makes solar cell processing difficult, although the use of periodic meltback improves the surface morphology to some extent. On the other hand, in layers grown from In/Cu solvents the development of these grooves is less pronounced and thus their morphology can be more suitable for solar cell processing. Such alloys also offer the advantages of higher growth rates and the ease of growing thick (>50µm) epilayers. Another solvent which has a high silicon solubility and which has to date not been investigated is Ag. From an economic viewpoint, solvents such as Cu and Sn may be preferable to solvents such as In and Ag, due to their greater abundance and lower cost.

The further investigation of the solvents In, Cu, Ag and Sn and their alloys for LPE on multicrystalline silicon substrates is therefore a possible subject of further research. Of particular interest would be the determination of the electrical parameters (mobility and minority carrier lifetime) and the fabrication of solar cells as diagnostic tools to assess the suitability of the solvents. From the results obtained so far, the system In/Cu is a promising candidate to be studied in more detail.

6.2.2 Choice of a suitable solar cell structure

Several possibilities exist for fabricating cost-effective solar cells by growing epitaxial layers on pre-existing multicrystalline silicon substrates. One approach is to grow the epitaxial layer on a sufficiently low cost silicon ribbon and then tolerate the efficiency losses resulting from the absence of light trapping. Another approach would be to remove most of the substrate following cell processing and bonding of the cell to a rigid superstrate. Removal of the substrate could be achieved, for example, by mechanical grinding, but the approach presents obvious difficulties since the grinding process must be cheap and since, in the absence of any low temperature surface passivation techniques, a few microns of the heavily doped substrate would have to be left untouched by the thinning process, so that the rear high–low junction can provide a degree of surface passivation. A third possibility involves the recrystallization of a thin amorphous silicon film by ZMR, as described in chapter 1. Fig. 6.1 illustrates a possible solar cell structure obtained using ZMR, for the case where a multicrystalline silicon substrate is used. The ZMR approach has the advantage that light trapping can be incorporated in the cell structure, as a result of the different refractive indices of the dielectric layer (SiO₂ in fig. 6.1) and silicon. The investigation of these different options is a further possible subject for future research.
6.2.3 Development of a high-throughput LPE technique

The LPE technique as was used for the experiments described in this thesis is useful only for laboratory-scale experiments. For LPE to become cost effective, an alternative method is required which is capable of much higher throughput rates. For example, typical LPE growth rates are 1 µm/min or less, while for the growth of multicrystalline silicon wafers by casting, for example, typical growth rates are 1–3 mm/min [1]. Even taking into account the much reduced thickness of LPE layers compared to cast silicon wafers and kerf losses, it is clear that the throughput rate of such a system is much too low to be commercially attractive.

One way of achieving higher throughput rates is to increase the growth rate, thus reducing the amount of time required to grow a single layer. This can be achieved with the temperature gradient growth technique, as outlined in section 2.5. Initial work on this technique has shown that it is capable of producing layers of sufficiently high quality, with lifetimes of several µs [2]. Significant work is still required in order to achieve the required thickness homogeneity. On the other hand, the use of a dipping LPE system as employed by Wang and Ciszek [3], permits the batch processing of LPE substrates. This approach should in principle be capable of even higher throughput rates, by enabling the growth of many LPE layers at the same time. However, the system used by Wang and Ciszek was not capable of removal of the native silicon oxide, which required the use of Al in the melt. Consequently, the epitaxial layers were more heavily doped than optimal. The development of a dipping system capable of in-situ oxide removal and its use to grow many layers at the same time could be an important step towards the realization of a commercial LPE process.

6.3 References


[2] P. Heidborn, G. Müller and H. Wawra, "Results of Large Area Liquid Phase Epitaxy of Silicon by Use of the Temperature Difference Method", private communication

Figure 6.1: A possible cell structure incorporating a degree of light trapping
Publications list for K.J. Weber as of 6/97

Journal Papers


6) **K.J. Weber**, K. Catchpole and A.W. Blakers, "Epitaxial Lateral Overgrowth of Si on (100) Si Substrates by Liquid Phase Epitaxy", submitted to J. Crystal Growth

Conference Papers


