

Message from the PDSEC-16 Workshop Chairs

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Welcome to the 17th IEEE International Workshop on Parallel and Distributed Scientific and Engineering Computing (PDSEC-16), held on May 27, 2016 in Chicago, USA, in conjunction with the 30th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2016).

The field of high performance computing has earned prominence through advances in electronic and integrated technologies. Current times are very exciting and the years to come will witness a proliferation in the use of parallel and distributed systems. Again, we saw a continuation in the increase in the use of board-level massively parallel processors for scientific applications, with one third of the papers of the workshop utilizing GP-GPUs and manycore processors for this purpose. We also saw an extent stronger emphasis on the orientation to Exascale computing and related concerns from previous, with several papers dealing with the issue of resilience. The scientific and engineering application domains have a key role in shaping future research and development activities in academia and industry, especially when the solution of large and complex problems must cope with tight timing schedules.

One of the most challenging issues facing scientific and engineering computing today is designing the infrastructure required to support massively parallel applications to the meet ever-evolving systems expected over the coming decades. This year we were especially delighted to have **Dr. George Bosilca from University of Tennessee, Knoxville, and Dr. Jeremiah Wilke from Sandia National Laboratories, California deliver the two PDSEC-16 keynote talks on parallel programming models, and their research challenges and future.**

For this year's workshop we have received many high-quality submissions from Australia, Asia Pacific, Europe, North Africa and North America. In a peer-reviewing phase with at least 3 reviews per paper, the submissions were judged by originality, relevance, technical quality, and clarity of presentation. Based on the reviews, we decided to accept 7 high-quality papers for presentation in the technical program of PDSEC-16 out of 14 papers submitted.

The annual PDSEC workshop brings together researchers from computer science, applied mathematics and other application areas of high-performance computing to present, discuss

and exchange ideas, results, work in progress and experiences in the area of parallel and distributed computing for problems in science and engineering applications.

For the contributed papers, there is one application paper on electron dynamics simulation. Two papers focus on task parallelism, one on a CFD code and the other one on radiative heat transport with many GPUs. Two papers are oriented on the area of resilience, both are illustrated with linear algebra applications. Finally two papers are oriented on performance: the former on linear algebra performance using CPUs and GPUs and the latter on an application profiler and emulator.

The program for this workshop is the result of hard and excellent work of many others. We would like to express our sincere appreciation to all authors for their valuable contributions and to all program committee members and external reviewers for their cooperation and diligent work in completing the workshop program under a very tight schedule. Last but not least, we thank Bora Uçar (CNRS and ENS Lyon, France) and Ramachandran Vaidyanathan (Louisiana State University, USA) the IPDPS 2016 Workshops Chair and Proceedings chair, for helping and encouraging the inclusion of the PDSEC-16 in IPDPS 2016.

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